

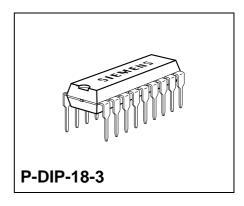
1-A DC Motor Driver

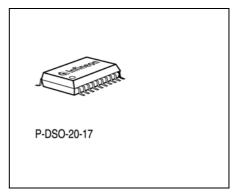
TLE 4205

Overview Bipolar IC

Features

- Max. driver current 1 A
- Integrated free-wheeling diodes
- Short-circuit proof to ground
- Inhibit
- ESD protected inputs
- Temperature range 40 °C $\leq T_{\rm j} \leq$ 150 °C





Туре	Ordering Code	Package
TLE 4205	Q67000-A9025	P-DIP-18-3
TLE 4205 G	Q67006-A9114	P-DSO-20-17

Description

TLE 4205 is an integrated power full-bridge DC-motor driver for a wide temperature range, as required in automotive applications for example. The circuit contains two power comparators that can be combined to a full-bridge circuit. For inductive loads there are integrated free-wheeling diodes to + $V_{\rm S}$ and ground. The outputs are short-circuit proof up to 18 V supply voltage to ground and turn off when overtemperature occurs. This IC is especially suitable for headlight-beam adjustment in automobiles.



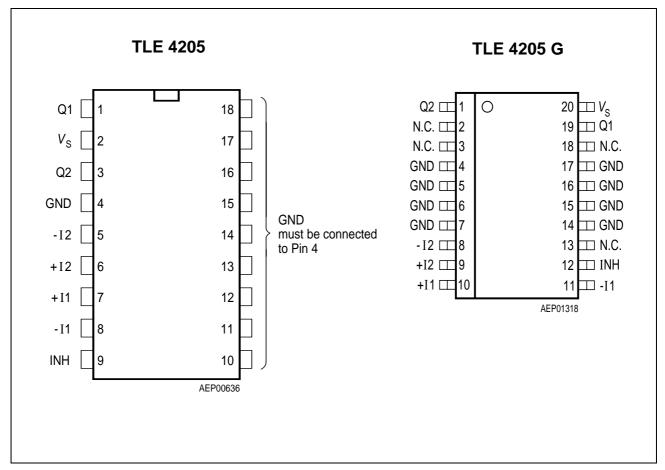


Figure 1 Pin Configuration (top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	Q1	Output Q1 of channel 1; push-pull B output with DC short-circuit protection to ground. Integrated free-wheeling diodes to ground and the supply voltage.
2	$V_{\mathbb{S}}$	Supply voltage V_s ; must be blocked to ground with a ceramic capacitor of at least 100 nF directly on the pins of the IC.
3	Q2	Output Q2 of channel 2; see pin 1.
4	GND	Ground
5	- I2	Inverting input channel 2 ; to be wired according to general rules.
6	+ 12	Non-inverting input channel 2; to be wired according to general rules.
7	+ I1	Non-inverting input channel 1; see pin 6.
8	- I1	Inverting input channel 1; see pin 5.
9	INH	Inhibit ; the IC is passive when this pin is open or connected to ground.
10-18	GND	Ground; must be connected to pin 4.



Pin Definitions and Functions (TLE 4205 G)

Pin No.	Symbol	Function
1	Q2	Output 2 of channel 2; push-pull B output with DC short-circuit protection to ground. Integrated free-wheeling diodes to ground and the supply voltage.
2	N.C.	Not connected
3	N.C.	Not connected
4-7	GND	Ground
8	- I2	Inverting input channel 2 ; to be wired according to general rules.
9	+ 12	Non-inverting input channel 2; to be wired according to general rules.
10	+ I1	Non-inverting input channel 1; see pin 9.
11	- I1	Inverting input channel 1; see pin 8.
12	INH	Inhibit ; the IC is passive when this pin is open or connected to ground.
13	N.C.	Not connected
14-17	GND	Ground
18	N.C.	Not connected
19	Q1	Output Q1 of channel 1, see pin 1.
20	V_{S}	Supply voltage $V_{\rm s}$; must be blocked with a ceramic capacitor of at least 100 nF directly on the pins of the IC.



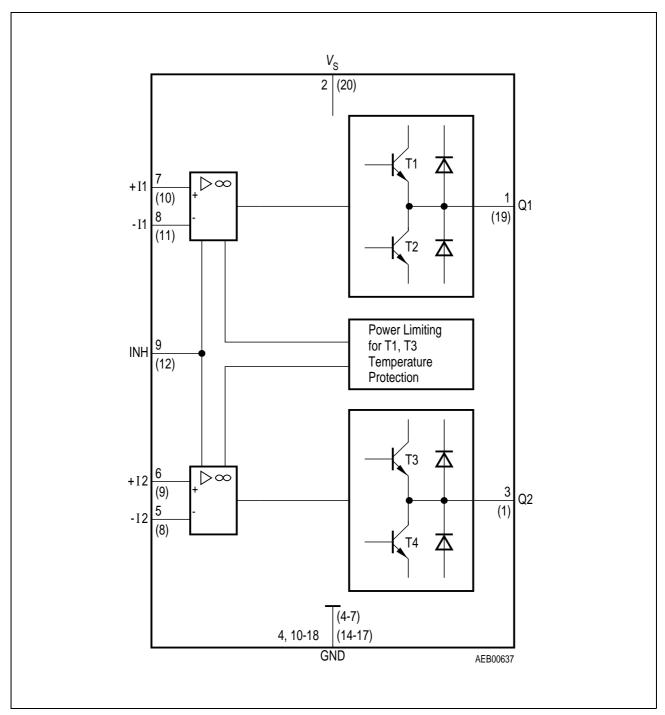


Figure 2 Block Diagram



Circuit Description

The IC contains two amplifiers with typical open-loop gain of 80 dB at 500 Hz.

The input stages consist of PNP-differential amplifiers. This produces a common-mode input range of 0 V to nearly $V_{\rm S}$ and a maximum differential input voltage of $V_{\rm S}$. The IC is guarded against ground shorts by an SOA-protective circuit. The output transistors are turned off if the chip temperature exceeds approx. 160 °C. The IC can be turned off by an inhibit input, which very much reduces current consumption.

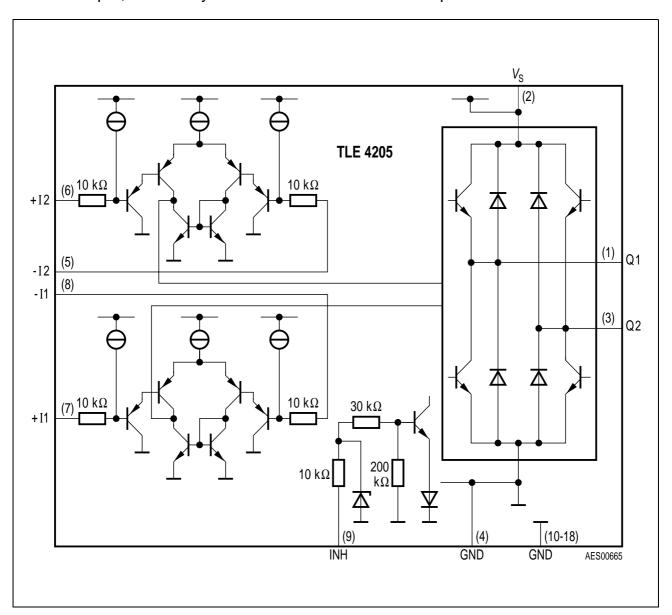


Figure 3 Circuit Diagram



Absolute Maximum Ratings

 $T_{\rm j}$ = - 40 to 150 °C

Parameter	Symbol	Limi	t Values	Unit	Remarks
		min.	max.		
Supply voltage	V_{S}	- 0.3	45	V	_
Differential input voltage	V_{ID}	_	± V _S	V	$\Delta V_{6\text{-}5}$ or $\Delta V_{7\text{-}8}$ TLE 4205 $\Delta V_{8\text{-}9}$ or $\Delta V_{10\text{-}11}$ TLE 4205 G
Output current	I_{Q}	– 1	1	Α	_
Supply current	$I_{\mathbb{S}}$	2.5	3	Α	_
Ground current	I_{GND}	-3	2.5	Α	12
Input voltage	V _I	– 15	V_{S}	V	V_5 ; V_6 ; V_7 ; V_8 TLE 4205 V_8 ; V_9 ; V_{10} ; V_{11} TLE 4205 G
Inhibit input	V_{Inh}	– 15	$V_{\mathtt{S}}$	V	V_{9} TLE 4205 V_{12} TLE 4205G
Junction temperature	T_{j}	_	150	°C	_
Storage temperature	$T_{ m stg}$	- 50	150	°C	_

Operating Range

<u> </u>					
Supply voltage	$V_{\mathtt{S}}$	6	32	V	_
Case temperature	T_{C}	- 40	105	°C	$P_{Dmax} = 3 \; W; \; DIP$
Case temperature	T_{C}	- 40	95	°C	$P_{Dmax} = 3 \; W; \; SO$
Thermal resistance junction - ambient junction - case	$R_{th\ JA} \ R_{th\ JC}$	_ _	60 15	K/W K/W	TLE 4205 TLE 4205
Thermal resistance junction - ambient junction - case	$R_{th\ JA} \ R_{th\ JC}$	_ _	65 20	K/W K/W	TLE 4205 G TLE 4205 G

Outputs pin 1 (19) and pin 3 (1) short-circuit proof to GND at $V_{\rm S} \le$ 18 V for TLE 4205 (TLE 4205G)



Characteristics

 $6 \text{ V} < V_{\text{S}} < 18 \text{ V}; -40 \text{ }^{\circ}\text{C} < T_{\text{j}} < 150 \text{ }^{\circ}\text{C}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General						
Open-circuit current consumption	$I_{\mathbb{S}}$	_	10	30	mA	active, both outputs
Open-circuit current consumption	$I_{\mathbb{S}}$	_	10	100	μΑ	inhibit
Turn-ON dead time ref. to $V_{9 {\rm OFF/ON}}$	t _{d ON}	-	10	20	μS	$ I_{1,3} < 1 \text{ A}$ TLE 4205 $ I_{1,19} < 1 \text{ A}$ TLE 4205 G
Turn-OFF dead time ref. to $V_{9 {\rm OFF/ON}}$	t _{d OFF}	_	10	20	μS	I _{1,3} < 1 A TLE 4205 I _{1,19} < 1 A TLE 4205 G
Open-loop gain	G_{VO}	50	80	_	dB	f = 500 Hz
Inputs						
Input zero voltage	V_{IO}	- 7.5	_	7.5	mV	$R_{\rm S}$ = 10 k Ω ;
Input-voltage drift	$\Delta V_{IO} / \Delta T$	_	20	30	μV/K	_
Input zero current	I_{IO}	- 75	_	75	mA	_
Input current	I_{I}	- 300	_	300	nA	_
Input-current drift	$\Delta I_{\rm I}/\Delta T$	_	_	5	nA/K	_
Input common-mode range, positive	V_{IC}	_	_	V _S - 2	V	_
Input common-mode range, negative	V_{IC}	-	_	- 0.5	V	-
Power-supply rejection ratio	PSSR	_	_	200	μV/V	$R_{\rm S}$ = 10 k Ω ;
Common-mode rejection ratio	CMRR	70	80	_	dB	_



Characteristics (cont'd)

6 V < $V_{\rm S}$ < 18 V; - 40 °C < $T_{\rm j}$ < 150 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Outputs						
Saturation voltage	V_{SatU}	_	1.35	1.5	V	$I_{\rm Q} = -0.6 \; {\rm A}$
Saturation voltage	V_{SatL}	_	0.8	1.2	V	$I_{\rm Q} = 0.6 \; {\rm A}$
Forward voltage of free-wheeling diode	$V_{\sf FU}$	_	1	1.5	V	$I_{\rm F} = 0.6 \; {\rm A}$
Forward voltage of free-wheeling diode	$V_{\sf FL}$	_	1	1.5	V	$I_{\rm F} = 0.6 \text{ A};$
Slew rate of V_{Q}	$dV_{q}dt_{r}$	_	0.5	_	V/µs	_
Inhibit Input			·			
Switching threshold high	V_{IH}	2	_	_	V	_
Switching threshold low	V_{IL}	_	_	0.8	V	_
H-input current	I_{IH}	_	100	_	μΑ	$V_9 = 5 \text{ V}$
L-input current	I_{IH}	-	0	 -	μΑ	$V_9 = 0 \text{ V}$

Note: $V_{\text{Sat U}} = \text{upper}$ $V_{\text{Sat L}} = \text{lower}$



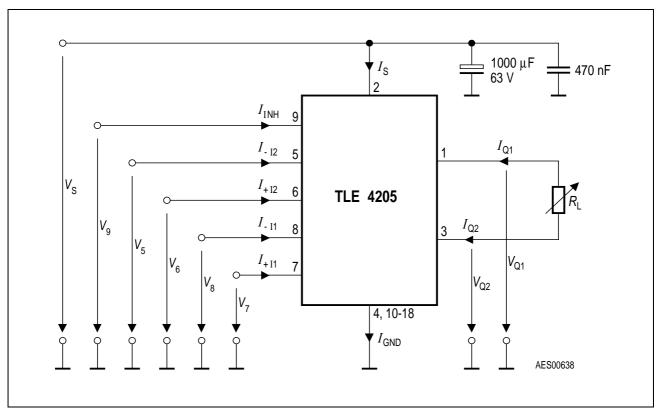


Figure 4 Test Circuit

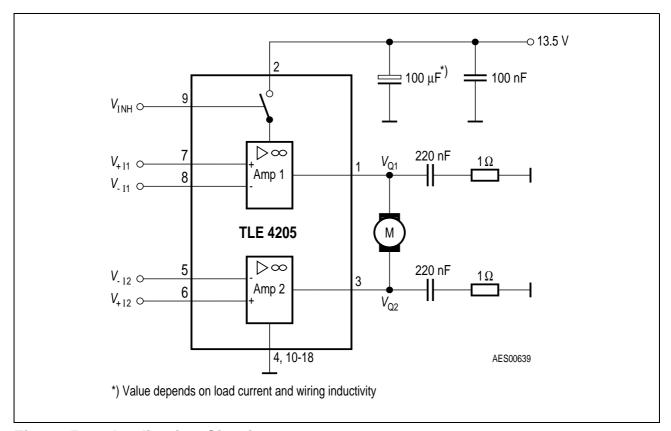
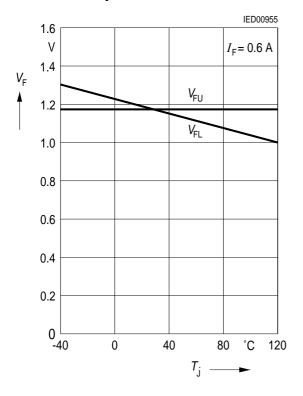


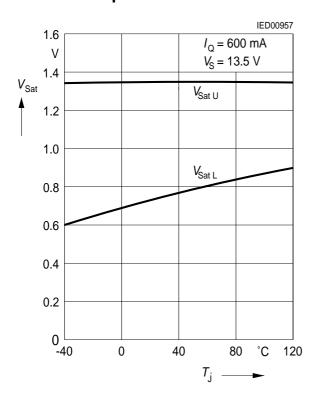
Figure 5 Application Circuit



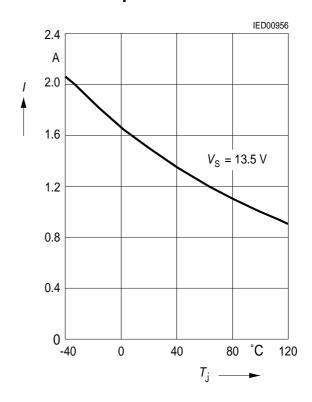
Forward Voltage of the Free-Wheeling Diodes versus Junction Temperature



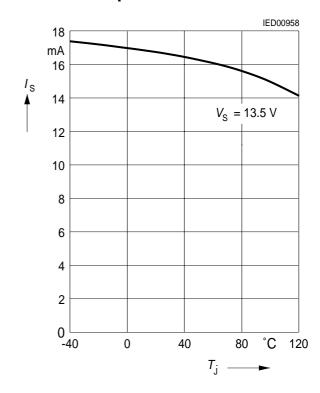
Saturation Voltage versus Junction Temperature



Start Point of the SOA-Protection Circuit versus Junction Temperature

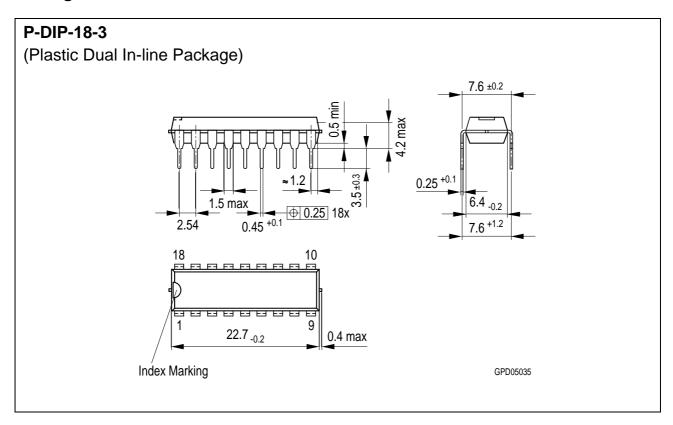


Current Consumption versus Junction Temperature





Package Outlines



Sorts of Packing

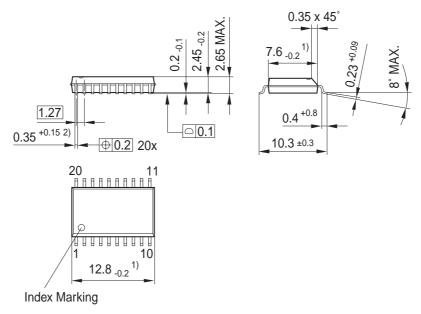
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm



P-DSO-20-17

(Plastic Dual Small Outline Package)



¹⁾ Does not include plastic or metal protrusion of 0.15 max. per side

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

²⁾ Does not include dambar protrusion of 0.05 max. per side