IR2130D

3-PHASE DRIVER

Features

- Hermetic
- Floating channel designed for bootstrap operation
  Fully operational to +400V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Under voltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent half-bridge drivers
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

V_{OFFSET}	400V max.
$I_{O+/-}$	100mA / 100mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	675ns & 425ns
Dead time (typ.)	0.9µs

Description

The IR2130D is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with 5V CMOS or LSTTL outputs. A ground-referenced operational amplifier provides analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also

An open drain $\overline{FAULT}$ signal indicates if an over current or under voltage shutdown has occurred. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use at high frequencies. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 400 volts.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to Vso. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Absolute Voltage	-0.3	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High Side Floating Supply Offset Voltage	V_{SO} - 5	V_{SO} + 400	
$V_{HO1,2,3}$	High Side Output Voltage	$V_{S1,2,3}$ - 0.3	$V_{S1,2,3}$ + 0.3	
V_{CC}	Low Side Fixed Supply Voltage	-0.3	20	
V_{SO}	Low Side Driver Return	-5	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low Side Output Voltage	V_{SO} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage (H_{IN}, L_{IN} & S_D)	-0.3	V_{CC} + 0.3	
V_{FLT}	Fault Output Voltage	-0.3	V_{CC} + 0.3	
V_{CAO}	Operational Amplifier Output Voltage	-0.3	V_{CC} + 0.3	
V_{CA}^-	Operational amplifier Inverting Input Voltage	-0.3	V_{CC} + 0.3	
dVS/dt	Allowable Offset Supply Voltage Transient (Fig. 16)	——	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq 25°C$ (Fig. 19)	——	1.5	W
$R_{th}JA$	Thermal Resistance, Junction to Ambient	——	70	°C/W
T_j	Junction Temperature	-55	125	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	——	300	
	Weight	6.1 (typical)		g

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{S0}. The V_S offset rating is tested with all supplies biased at 15V differential.

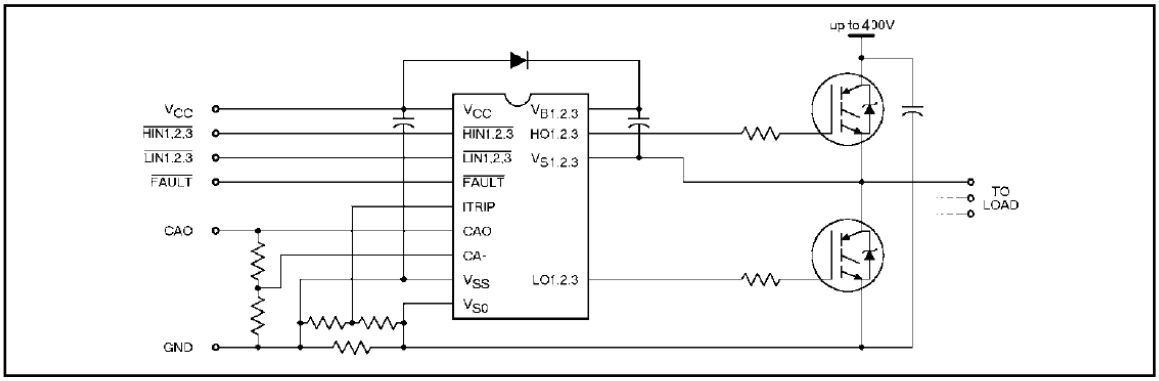
Symbol	Parameter	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Absolute Voltage	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High Side Floating Supply Offset Voltage	V_{SO} - 5	V_{SO} + 400	
$V_{HO1,2,3}$	High Side Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low Side Fixed Supply Voltage	10	20	
V_{SS}	Logic Ground	-5	5	
$V_{LO1,2,3}$	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage (H_{IN}, L_{IN} & S_D)	V_{SS}	V_{SS} + 5	
V_{FLT}	Fault Output Voltage	V_{SS}	V_{CC}	
V_{CAO}	Operational Amplifier Output Voltage	V_{SS}	5	
V_{CA}	Operational amplifier Inverting Input Voltage	V_{SS}	5	

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, V_{S0},1,2,3 = V_{SS}, C_L = 1000 pF unless otherwise specified.

		T_J = 25°C			T_J = - 55°C to 125°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Max.	Units	Test Conditions
$t_{d(on)}$	Turn-On Propagation Delay (all six channels)	500	675	850	—	850	ns	C_L= 1000pF $V_{S1,2,3}$ = 0 to 400 V V_{IN} = 0 & 5 V
tr	Turn-On Rise Time (all six channels)	—	80	125	—	175		
$t_{d(off)}$	Turn-Off Propagation Delay (all six channels)	300	425	550	—	675		
t_f	Turn-Off Fall Time (all six channels)	—	35	55	—	85		
D_T	Dead time (LS Turn-off to HS Turn-on & HS Turn-off to LS Turn-on)	0.4	0.9	1.3	0.25	1.5	µs	C_L = 1000pF, V_{IN} = 0 & 5V
t_{itrip}	ITRIP to Output Shutdown Prop. Delay	400	660	920	—	1100	ns	C_L = 1000pF, V_{IN}, V_{ITRIP} = 0 & 5V
t_{flt}	ITRIP to FAULT Indication Delay	335	590	845	—	1000	ns	
t_{fltclr}	LIN1, 2, 3 To FAULT Clear Time	5.5	10	12.5	—	—	µs	
$t_{flt,in}$	Input Filter Time (all six inputs)	—	310	—	—	—	ns	V_{IN} = 0 & 5V
t_{bl}	ITRIP Blanking Time	—	400	—	—	—	ns	V_{ITRIP} = 1V
SR+	Amplifier Slew Rate (+)	3.75	5.0	—	2.7	—	V/µs	
SR-	Amplifier Slew Rate (-)	2.4	3.2	—	1.5	—	V/µs	

Typical Connection



Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{SO1,2,3}$ = V_{SS} unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: HIN1, 2, 3 & LIN1, 2, 3. The V_O and I_O parameters are referenced to $V_{SO1,2,3}$.

		T_J = 25°C			T_J = - 55°C to 125°C			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
I_{LK}	Offset Supply Leakage Currents	—	—	50	—	500	µA	V_B = V_S = 400V
I_{QBS}	Quiescent VBS Supply Current	—	15	30	—	200		V_{IN} = 0V or 5V
I_{QCC}	Quiescent VCC Supply Current	—	3.0	4.0	—	6.0	mA	V_{IN} = 0V or 5V
I_{IN}+	Logic "1" Input Bias Current (OUT = HI)	—	450	650	—	1050		V_{IN} = 0V
I_{IN}-	Logic "0" Input Bias Current (OUT = LO)	—	225	400	—	—	µA	V_{IN} = 5V
I_{ITRIP}+	"High" ITRIP Bias Current	—	75	150	—	—		I_{TRIP} = 5V
I_{ITRIP}-	"Low" ITRIP Bias Current	—	—	100	—	170	nA	I_{TRIP} = 0V
V_{IN}-IH	Logic "0" Input Voltage (OUT = LO)	—	—	—	2.2	—	V	
V_{IN}-IL	Logic "1" Input Voltage (OUT = HI)	—	—	—	—	0.8		
V_{IT},TH+	ITRIP Input Positive Going Threshold	400	490	580	350	580	mV	V_{SO} = CA- = 0.2V
V_{OS}	Amplifier Input Offset Voltage	—	—	30	—	—		
R_{ON},FLT	FAULT- Low On Resistance	—	55	75	—	150	Ω	
I_{CA}-	CA- Input Bias Current	—	0.5	4.0	—	4.0	nA	CA- = 2.5V
V_{CCUV}+	VCC Supply Under voltage Positive Going Threshold	8.3	9.0	10.6	8.0	10.7	V	
V_{CCUV}-	VCC Supply Under voltage Negative Going Threshold	8.0	8.7	10.5	7.7	10.5		
V_{BSUV}+	VBS Supply Under voltage Positive Going Threshold	7.5	8.4	9.5	—	—	V	
V_{BSUV}-	VBS Supply Under voltage Negative Going Threshold	7.1	8.0	9.3	—	—		
I_O+	Output High Short Circuit Pulsed Current	100	500	—	—	—	mA	V_{OUT} = V_{IN}- = 0V PW <= 10µS
I_O-	Output Low Short Circuit Pulsed Current	100	500	—	—	—	mA	V_{OUT} = 15V, V_{IN}- = 5V PW <= 10µS
V_{OH} Amp	Amplifier High Level Output Voltage	5.0	5.2	5.4	4.9	5.6	V	CA- = 0V, V_{SO} = 1V
V_{OL}Amp	Amplifier Low Level Output Voltage	—	2.5	20	—	20	mV	CA- = 1V, V_{SO} = 0V
I_{SRC}Amp	Amplifier Output Source Current	2.3	4.0	—	1.5	—	mA	CA- = 0V, V_{SO} = 1V, C_{AO}=4V
I_{SNK}Amp	Amplifier Output Sink Current	1.0	2.1	—	0.5	—		CA- = 1V, V_{SO} = 0V, C_{AO} = 2V
CMRR	Amplifier Common Mode Rejection Ratio	60	80	—	—	—	dB	CA- =V_{SO} =0.1V & 5V
PSRR	Amplifier Power Supply Rejection Ratio	55	75	—	—	—		CA- = V_{SO} = 0.2V V_{CC} = 10V & 20V
V_{OH}	High Level Output Voltage	—	—	100	—	100	mV	V_{IN}- = 0V, I_O = 0A
V_{OL}	Low Level Output Voltage	—	—	100	—	100		V_{IN}- = 5V, I_O = 0A
I_O+Amp	Amplifier Output High Short Circuit Circuit	—	4.5	6.5	—	8.0		CA- = 0V, V_{SO} = 5V V_{CAO} = 0V
I_O+Amp	Amplifier Output High Short Circuit Circuit	—	3.2	5.2	—	7.0		CA- = 5V, V_{SO} = 0V V_{CAO} = 5V

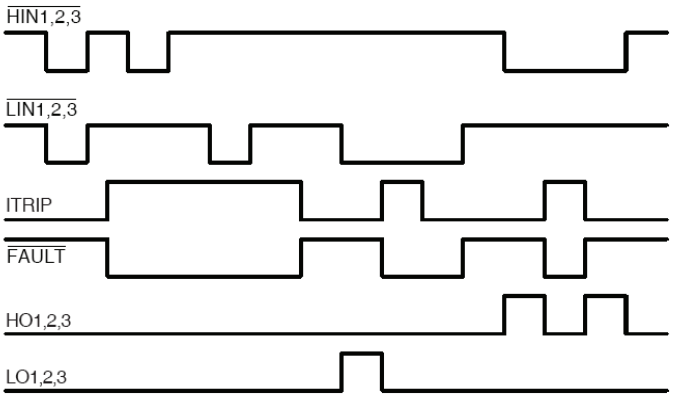


Fig 1. Input/Output Timing Diagram

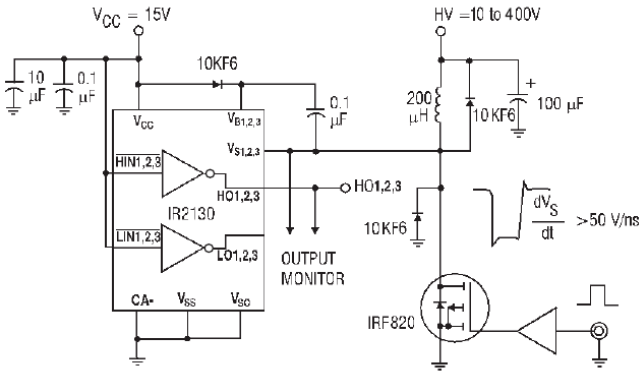


Fig 2. Floating Supply Voltage Transient Test

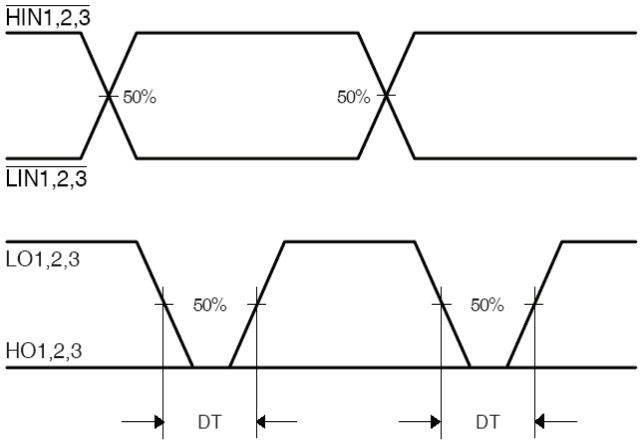


Fig 3. Dead time Waveform Definitions

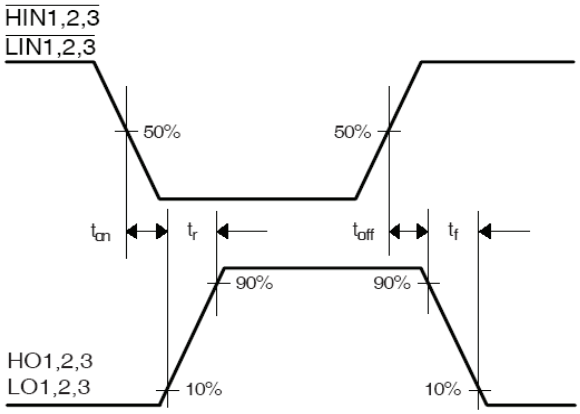


Fig 4. Input/Output Switching Time Waveform Definitions

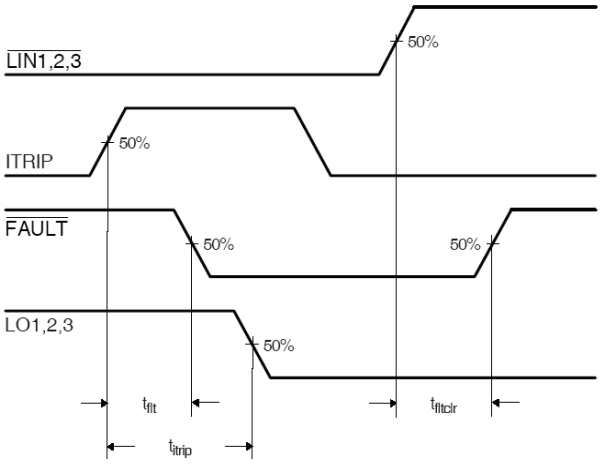


Fig 5. Overcurrent Shutdown Switching Time Waveform Definitions

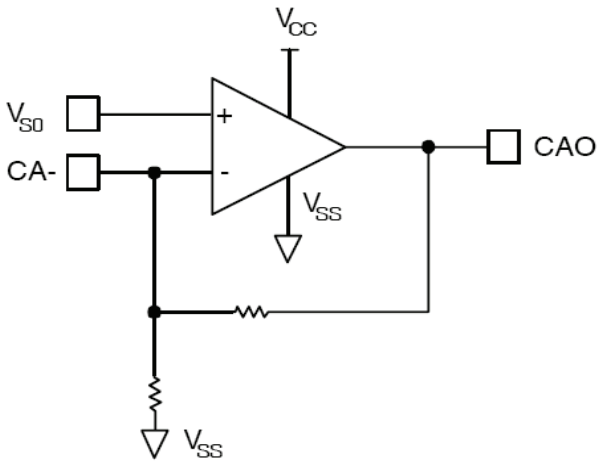


Fig 6. Diagnostic Feedback Operational Amplifier Circuit

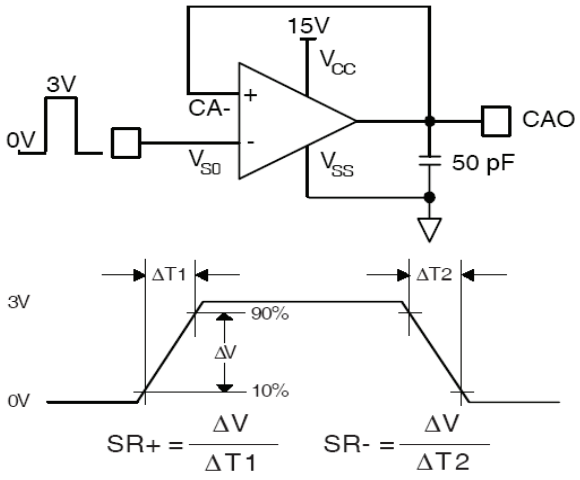


Fig 7. Operational Amplifier Slew Rate Measurement

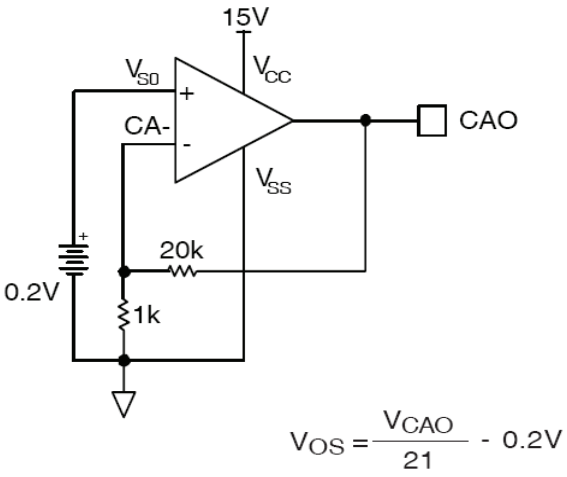
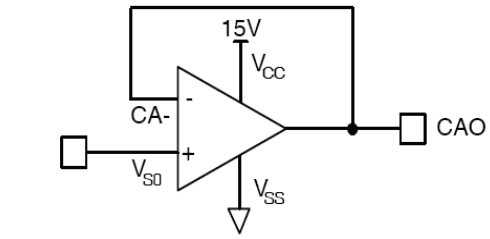


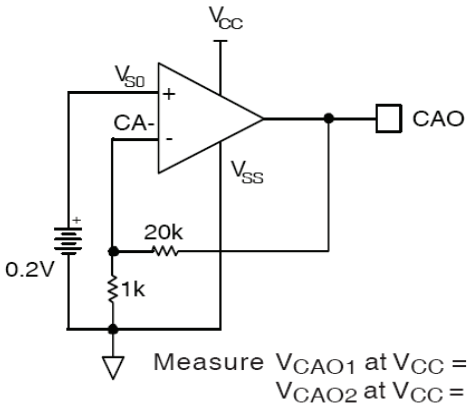
Fig 8. Operational Amplifier Input Offset Voltage Measurement



Measure V_{CAO1} at V_{SO} = 0.1V
V_{CAO2} at V_{SO} = 5V

$$CMRR = -20*LOG\left|\frac{(V_{CAO1}-0.1V) - (V_{CAO2}-5V)}{4.9V}\right| (dB)$$

Fig 9. Operational Amplifier Common Mode Rejection Ratio Measurements



Measure V_{CAO1} at V_{CC} = 10V
V_{CAO2} at V_{CC} = 20V

$$PSRR = -20*LOG\left|\frac{V_{CAO1} - V_{CAO2}}{(10V)\ (21)}\right|$$

Fig 10. Operational Amplifier Power Supply Rejection Ratio Measurements

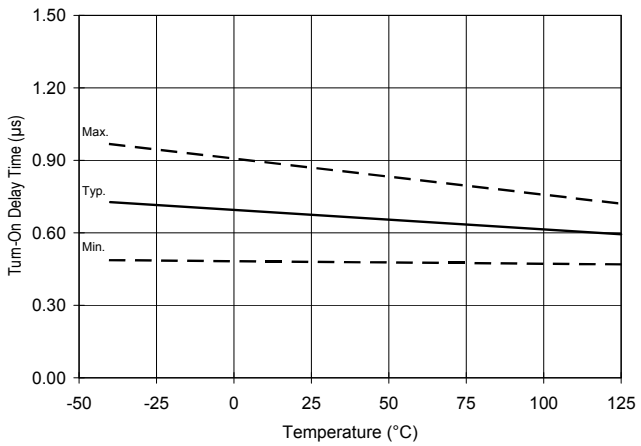


Fig 11A. Turn-On Time Vs. Temperature

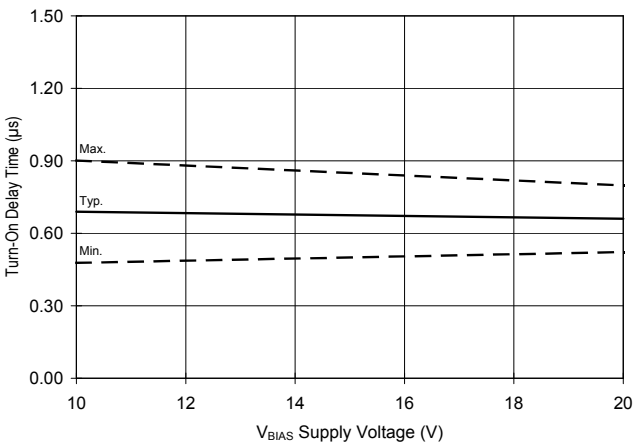


Fig 11B. Turn-On Time Vs. Voltage

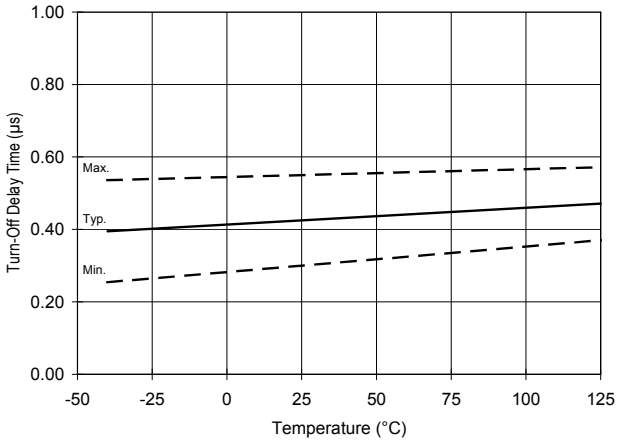


Fig 12a. Turn-Off Time Vs. Temperature

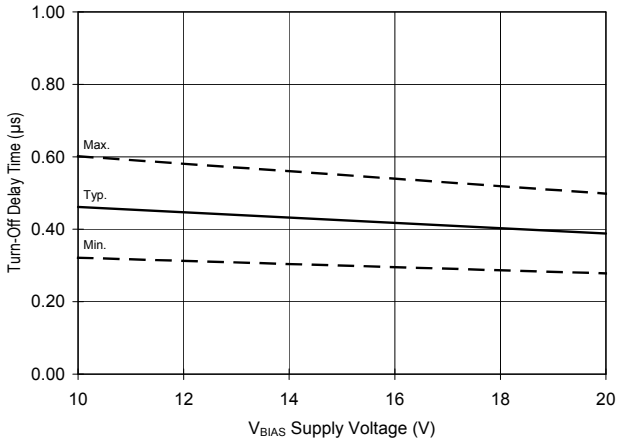


Fig 12b. Turn-Off Time Vs. Voltage

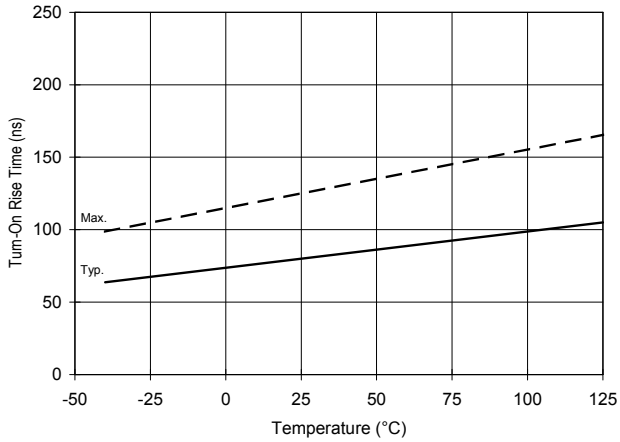


Fig 13a. Turn-On Rise Time Vs. Temperature

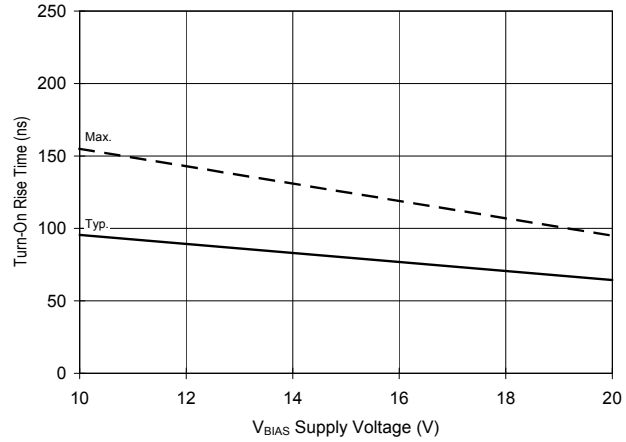


Fig 13b. Turn-On Rise Time Vs. Voltage

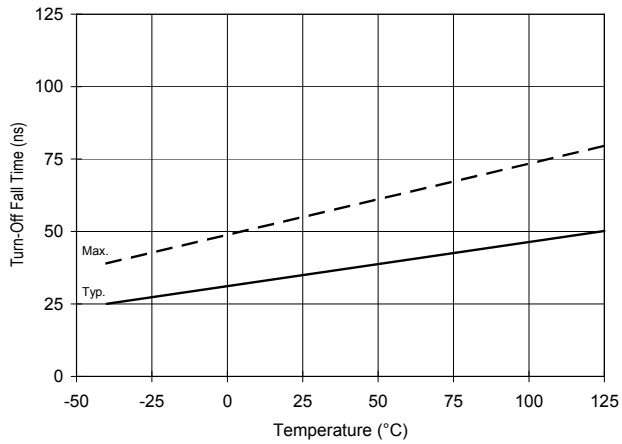


Fig 14a. Turn-Off Fall Time Vs. Temperature

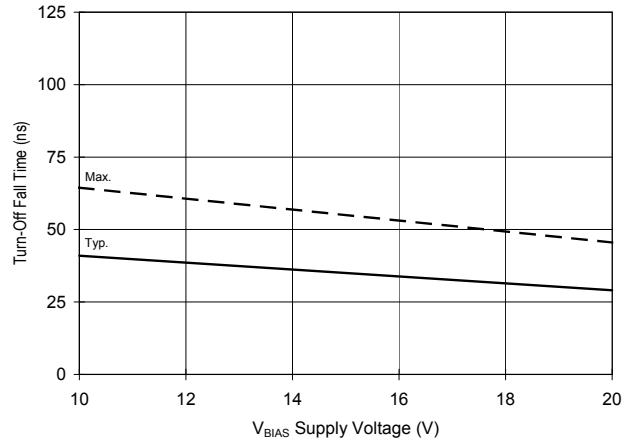


Fig 14b. Turn-Off Fall Time Vs. Voltage

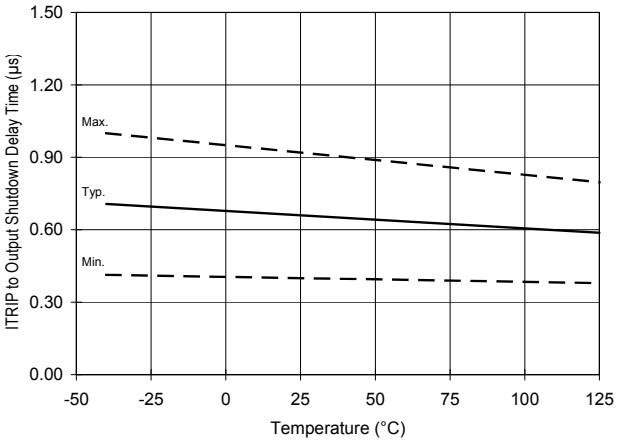


Fig 15a. ITRIP to Output Shutdown Time Vs. Temperature

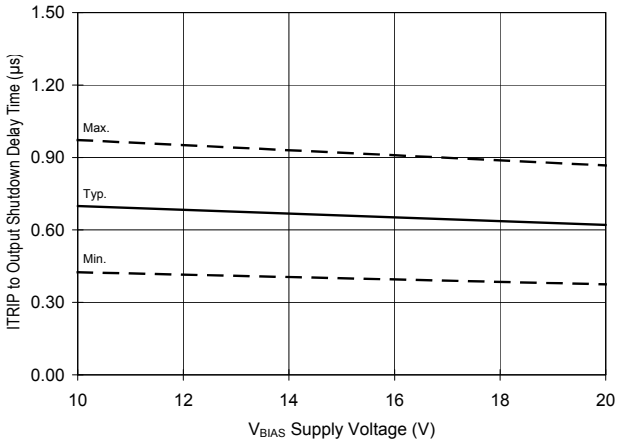


Fig 15b. ITRIP to Output Shutdown Time Vs. Voltage

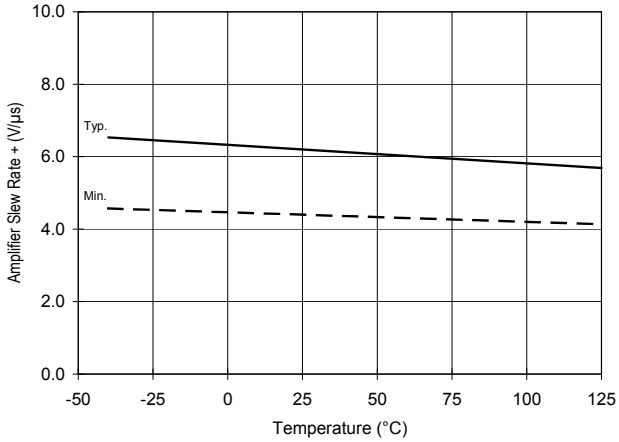


Fig 16a. ITRIP to **FAULT** Indication Time Vs. Temperature

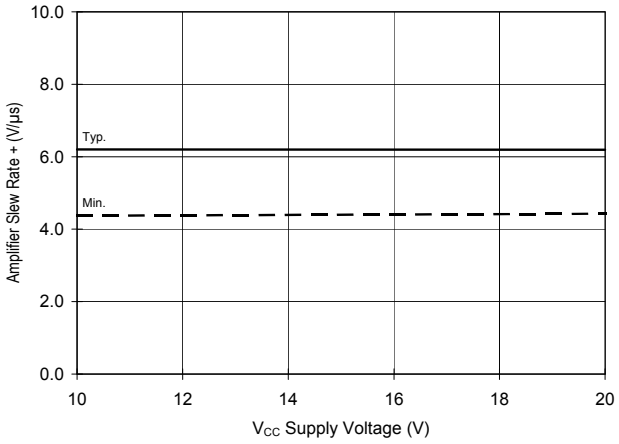


Fig 16b. ITRIP to **FAULT** Indication Time Vs. Voltage

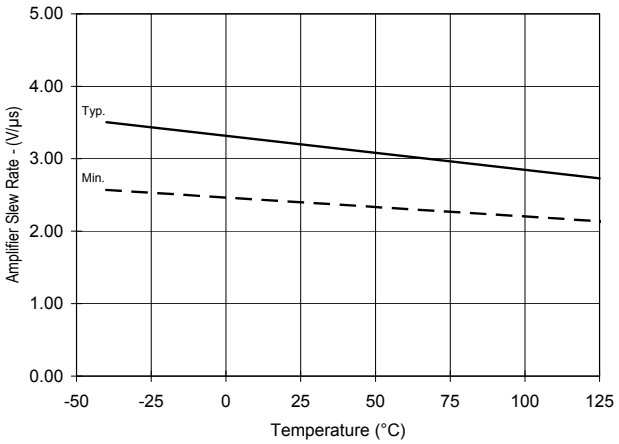


Fig 17a. **LIN 1,2,3** to **FAULT** Clear Time Vs. Temperature

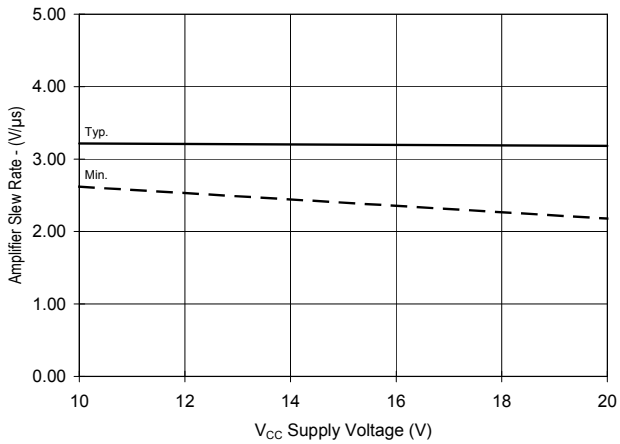


Fig 17b. **LIN 1,2,3** to **FAULT** Clear Time Vs. Voltage

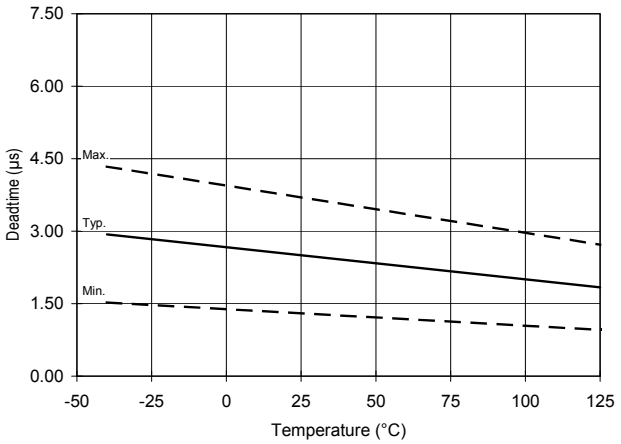


Fig 18a. Deadtime Vs. Temperature

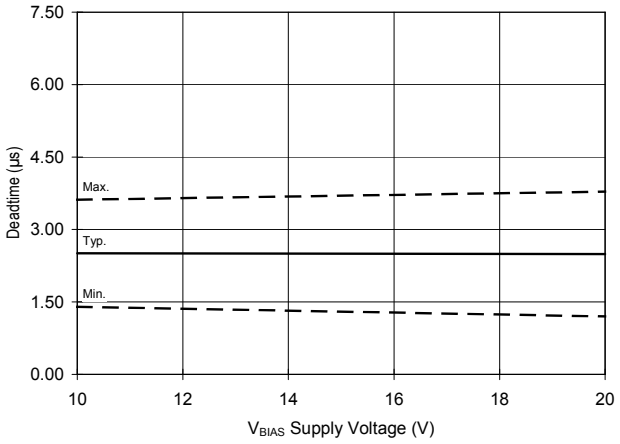


Fig 18b. Deadtime Vs. Voltage

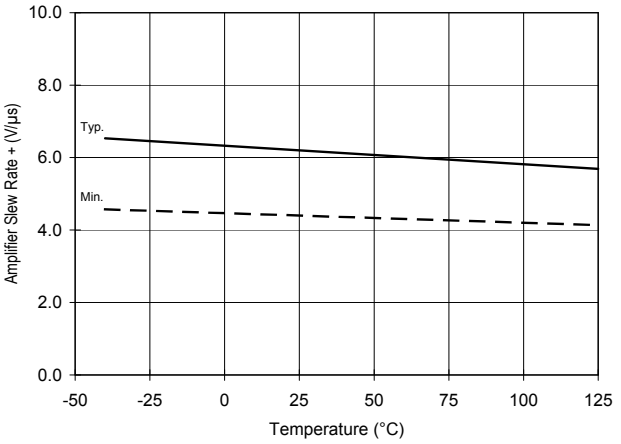


Fig 19a. Amplifier Slew Rate (+) Vs. Temperature

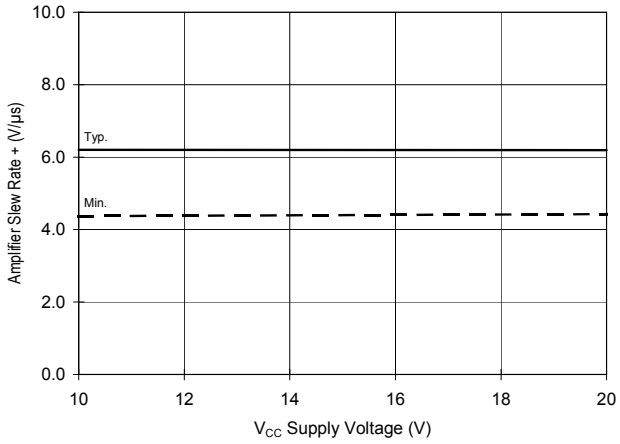


Fig 19b. Amplifier Slew Rate (+) Vs. Voltage

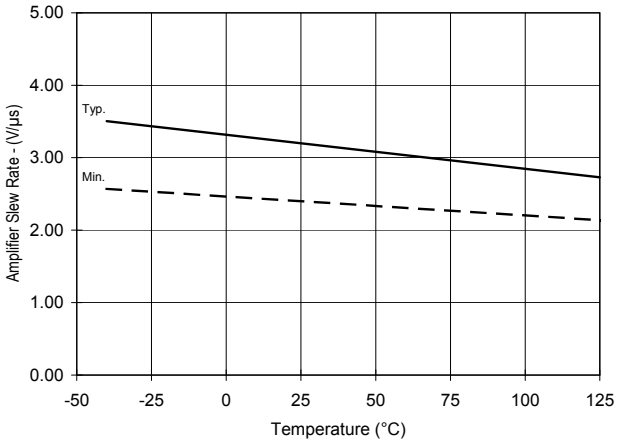


Fig 20a. Amplifier Slew Rate (-) Vs. Temperature

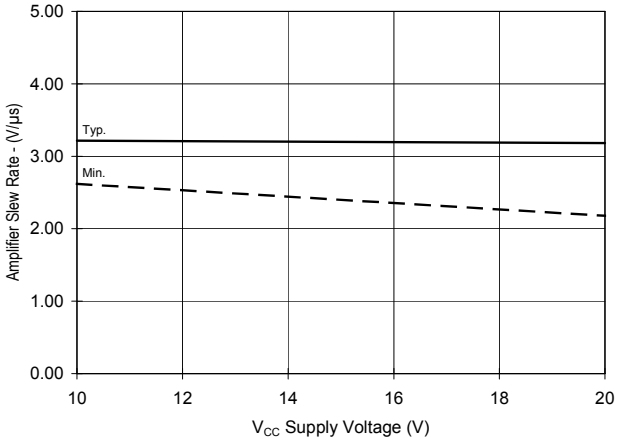


Fig 20b. Amplifier Slew Rate (-) Vs. Voltage

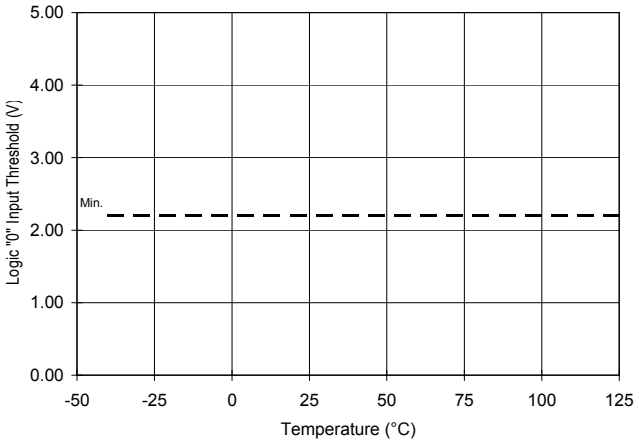


Fig 21a. Logic “0” Input Threshold Vs. Temperature

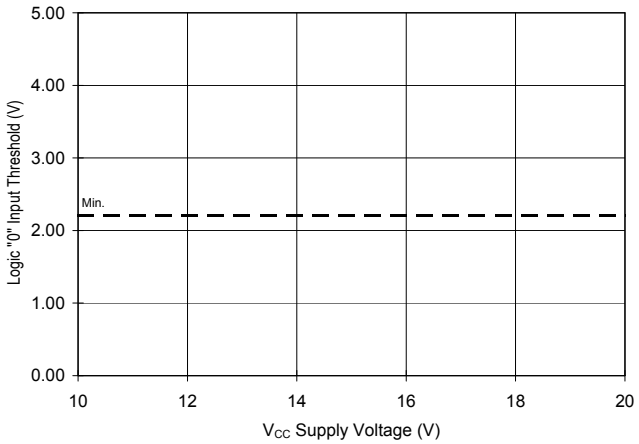


Fig 21b. Logic “0” Input Threshold Vs. Voltage

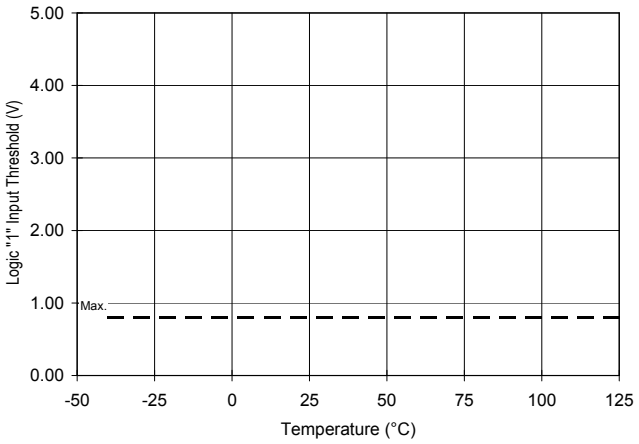


Fig 22a. Logic “1” Input Threshold Vs. Temperature

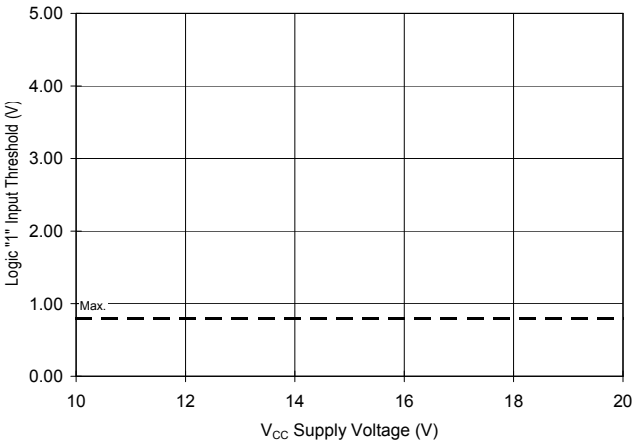


Fig 22b. Logic “1” Input Threshold Vs. Voltage

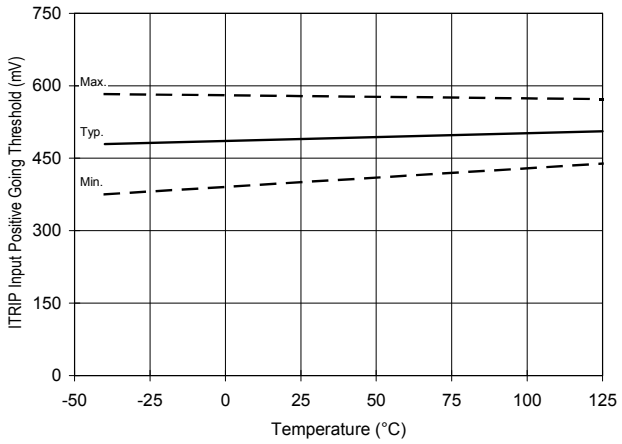


Fig 23a. ITRIP Input Positive Going Threshold Vs. Temperature

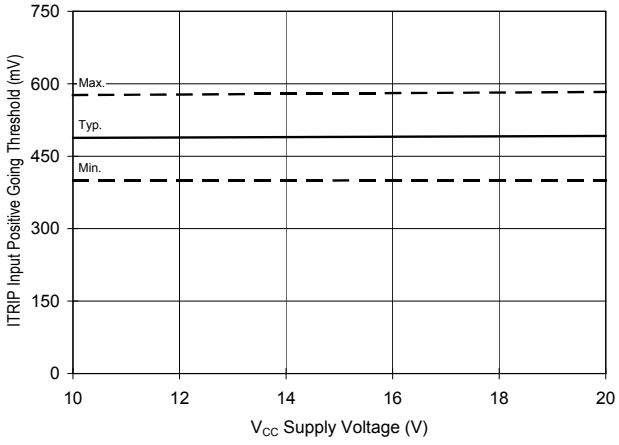


Fig 23b. ITRIP Input Positive Going Threshold

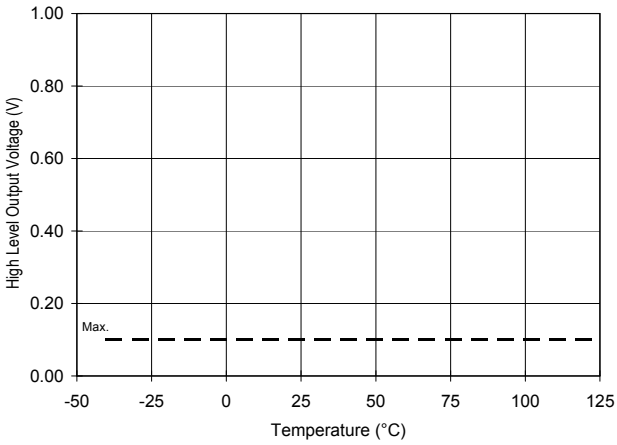


Fig 24a. High Level Output Vs. Temperature

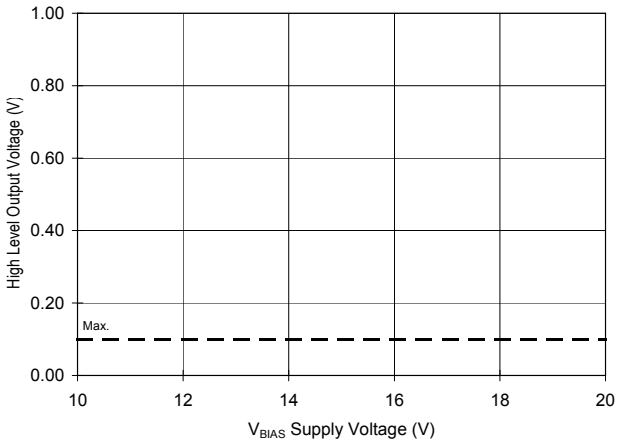


Fig 24b. High Level Output Vs. Voltage

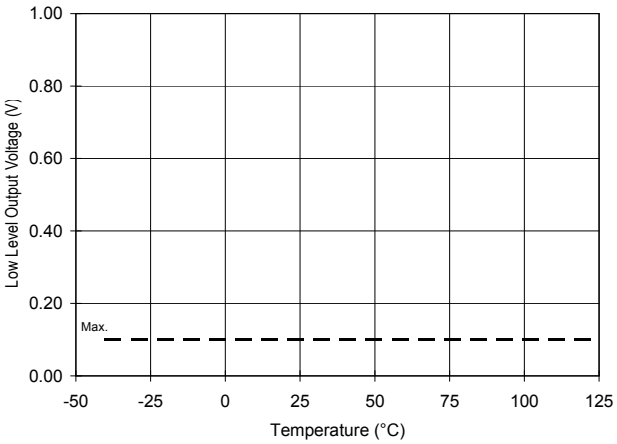


Fig 25a. Low Level Output Vs. Temperature

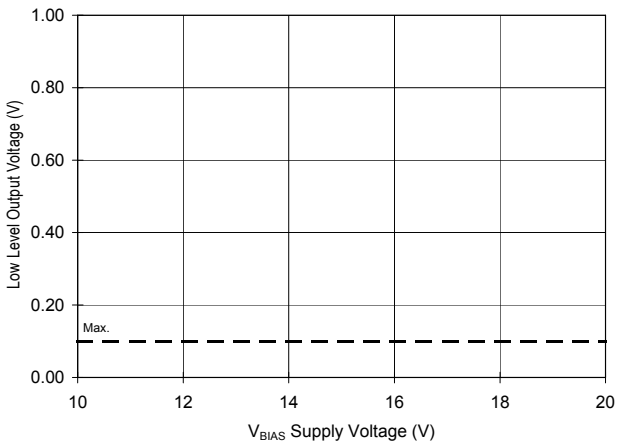


Fig 25b. Low Level Output Vs. Voltage

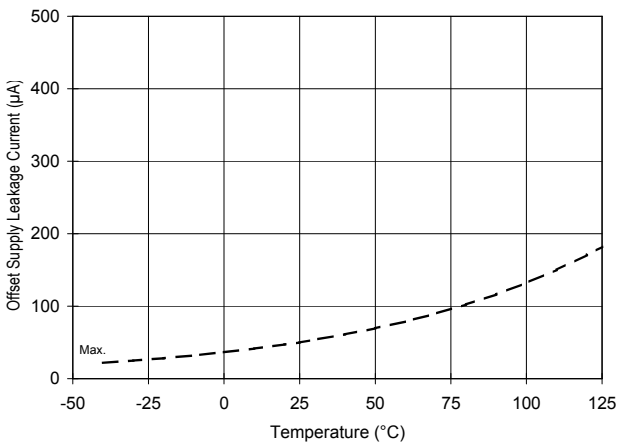


Fig 26a. Offset Supply Leakage Current Vs. Temperature

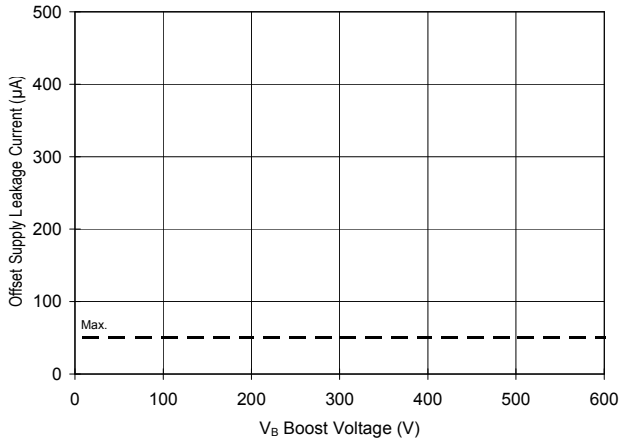


Fig 26b. Offset Supply Leakage Current Vs. Voltage

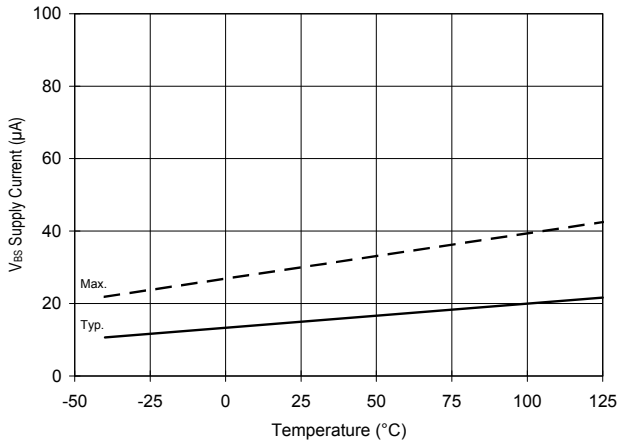


Fig 27a. V_{BS} Supply Current Vs. Temperature

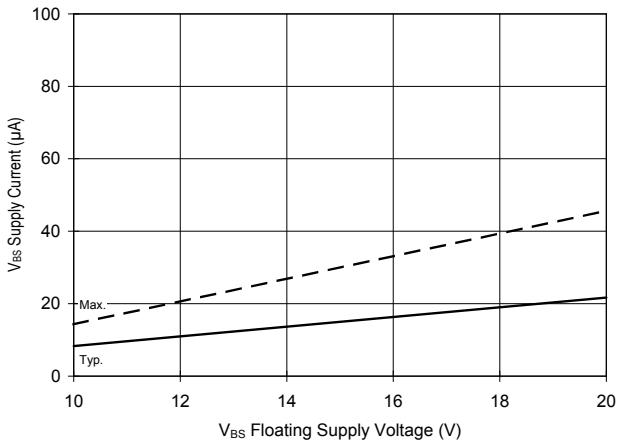


Fig 27b. V_{BS} Supply Current Vs. Voltage

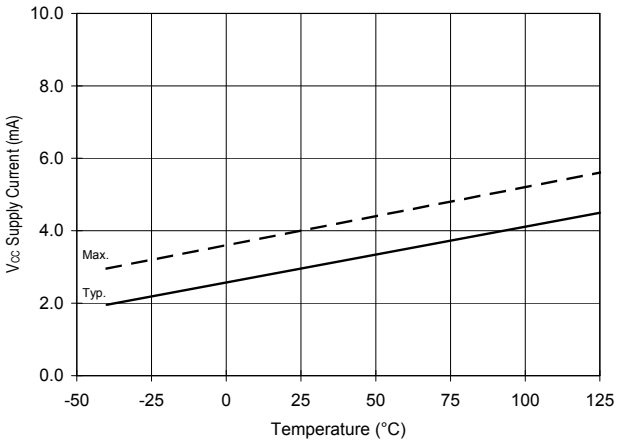


Fig 28a. V_{CC} Supply Current Vs. Temperature

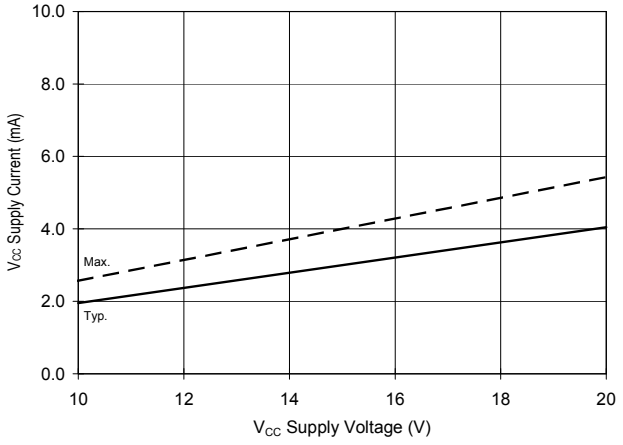


Fig 28b. V_{CC} Supply Current Vs. Voltage

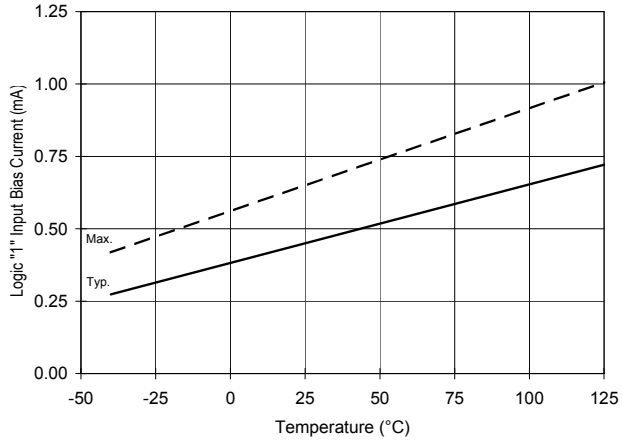


Fig 29a. Logic “1” Input Current Vs. Temperature

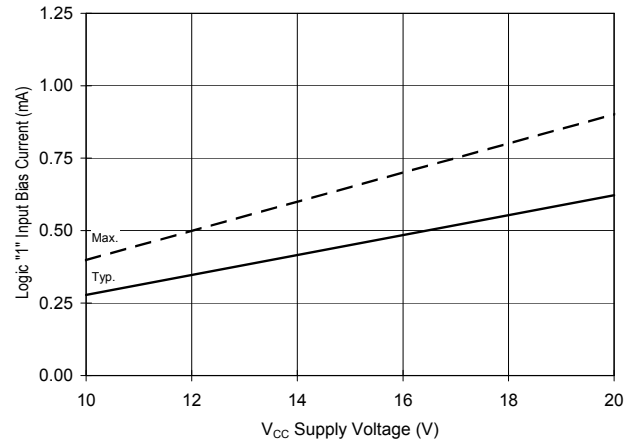


Fig 29b. Logic “1” Input Current Vs. Voltage

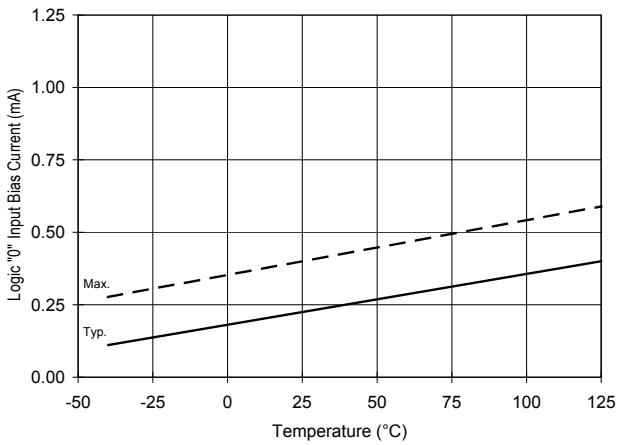


Fig 30a. Logic “0” Input Current Vs. Temperature

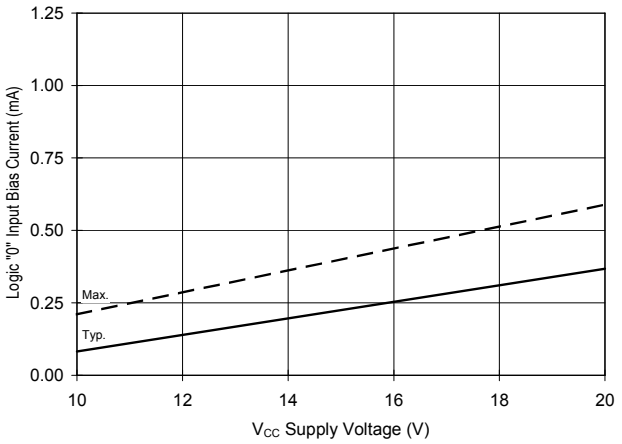


Fig 30b. Logic “0” Input Current Vs. Voltage

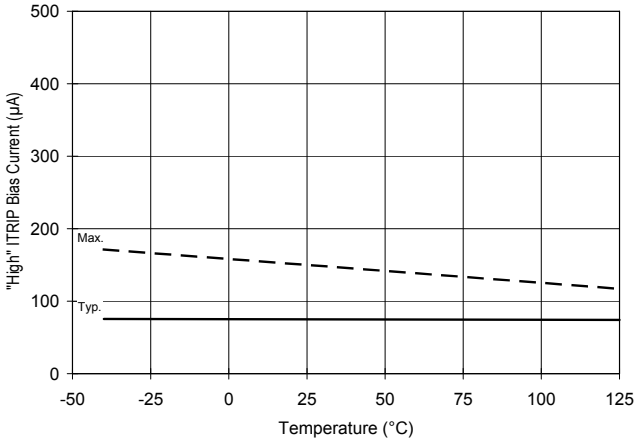


Fig 31a. “High” ITRIP Current Vs. Temperature

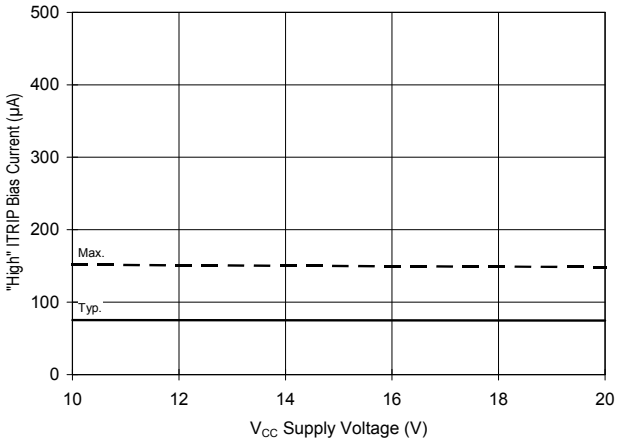


Fig 31b. “High” ITRIP Current Vs. Voltage

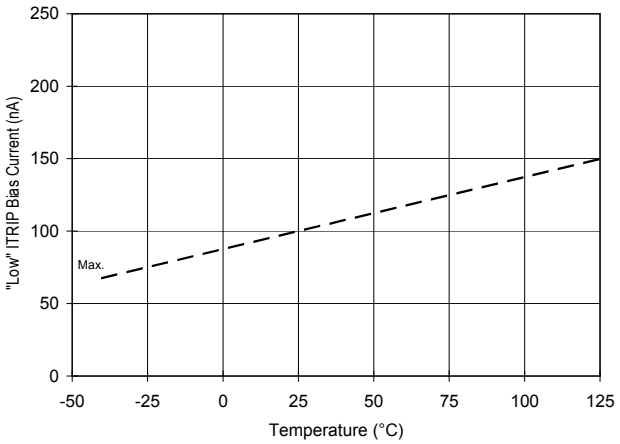


Fig 32a. “Low” ITRIP Current Vs. Temperature

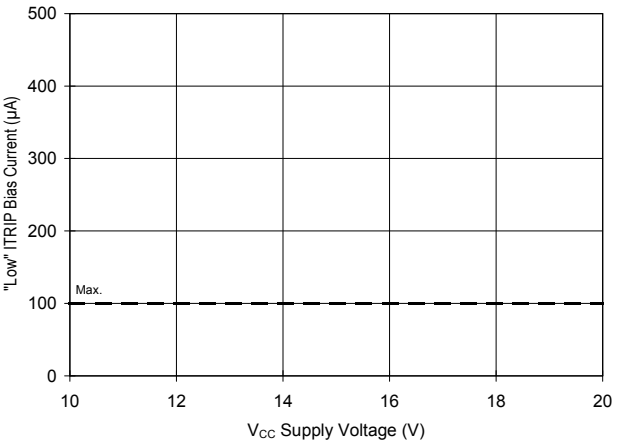


Fig 32b. “Low” ITRIP Current Vs. Voltage

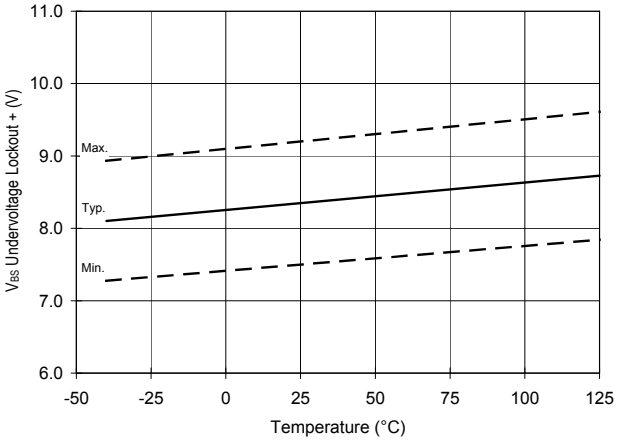


Fig 33. V_{BS} Under voltage (+) Vs. Temperature

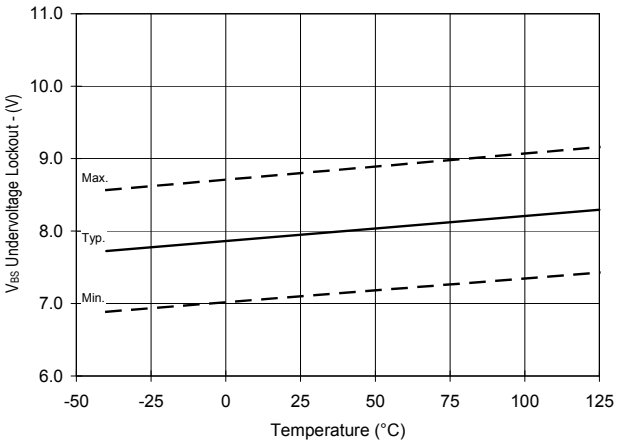


Fig 34. V_{BS} Under voltage (-) Vs. Temperature

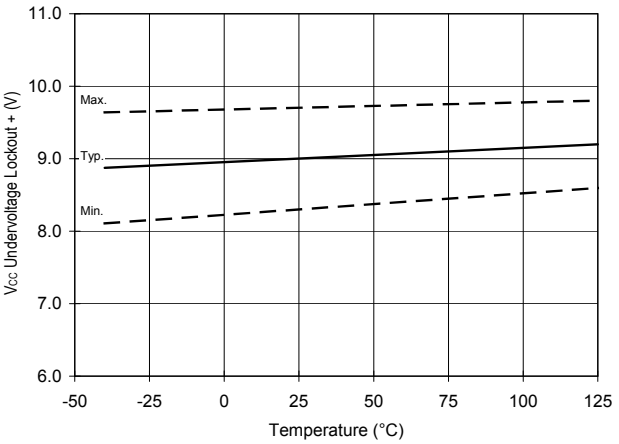


Fig 35. V_{CC} Under voltage (+) Vs. Temperature

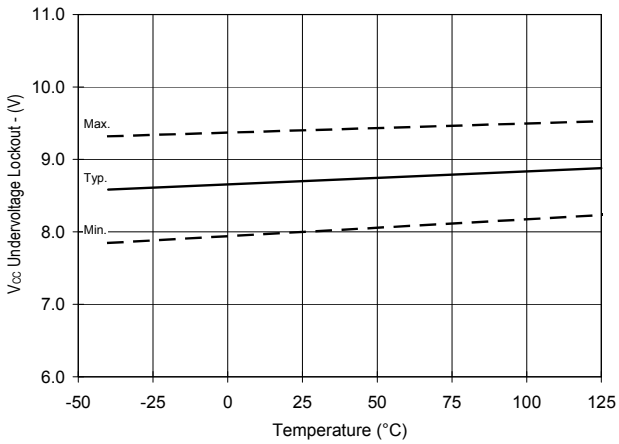


Fig 36. V_{CC} Under voltage (-) Vs. Temperature

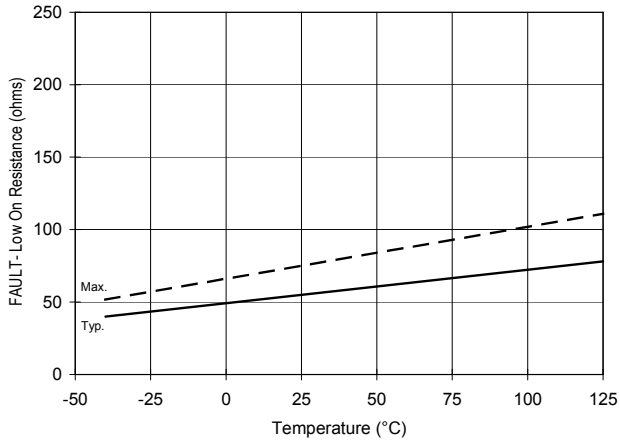


Fig 37a. $\overline{\textbf{FAULT}}$ Low On Resistance Vs. Temperature

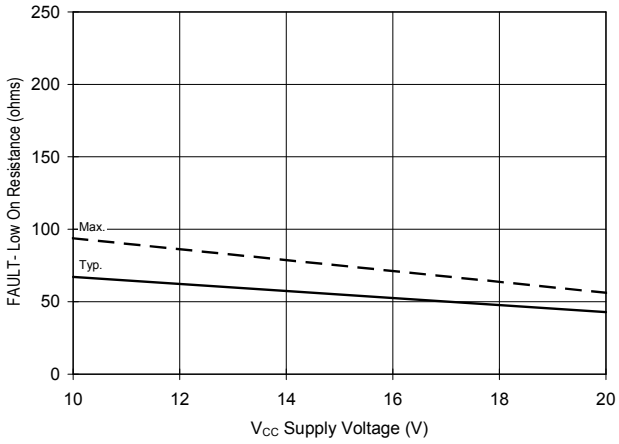


Fig 37b. $\overline{\textbf{FAULT}}$ Low On Resistance Vs. Voltage

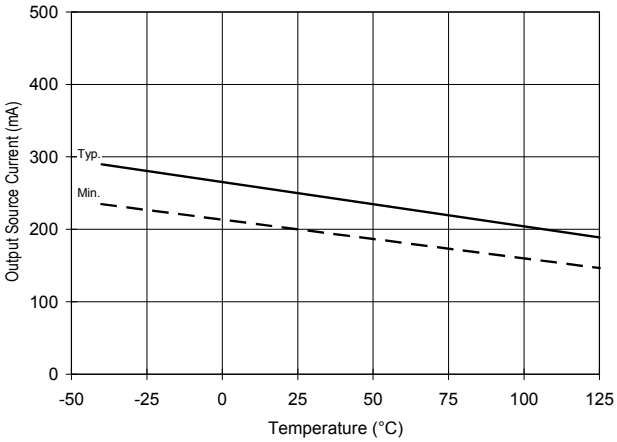


Fig 38a. Output Source Current Vs. Temperature

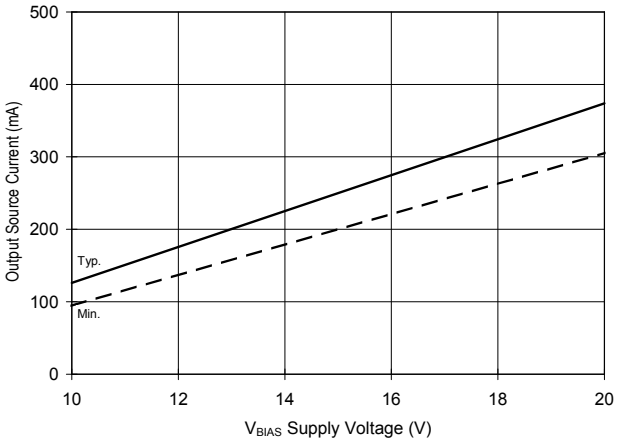


Fig 38b. Output Source Current Vs. Voltage

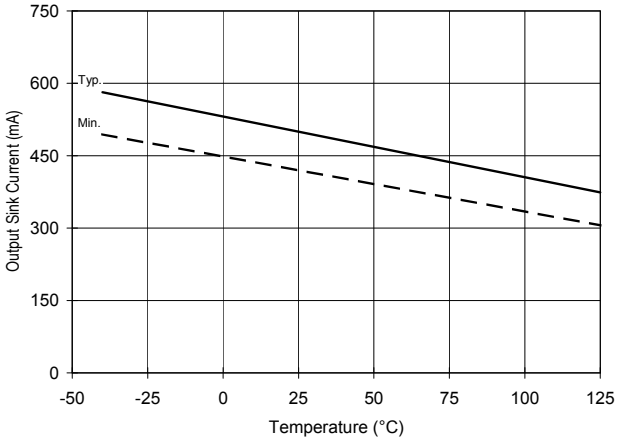


Fig 39a. Output Sink Current Vs. Temperature

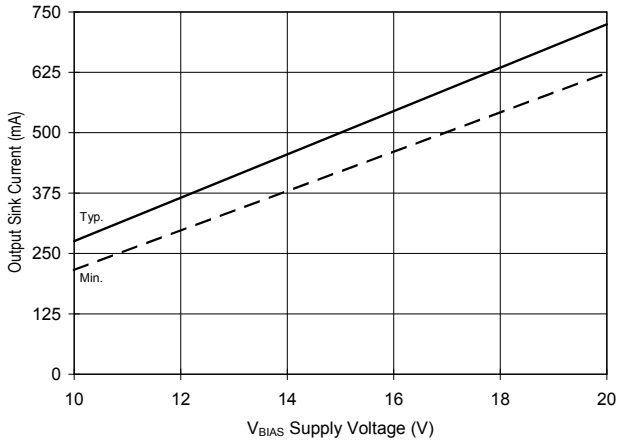


Fig 39b. Output Sink Current Vs. Voltage

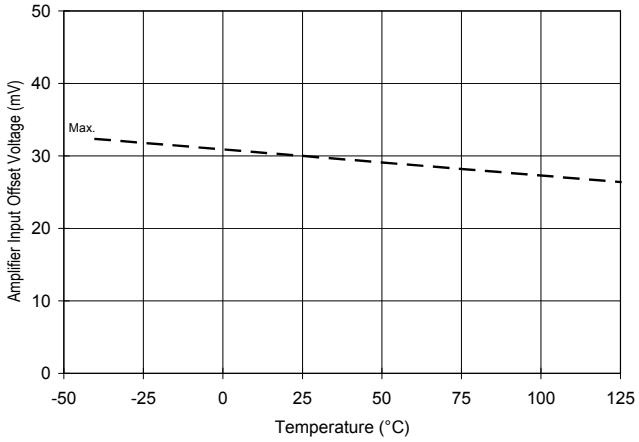


Fig 40a. Amplifier Input Offset Vs. Temperature

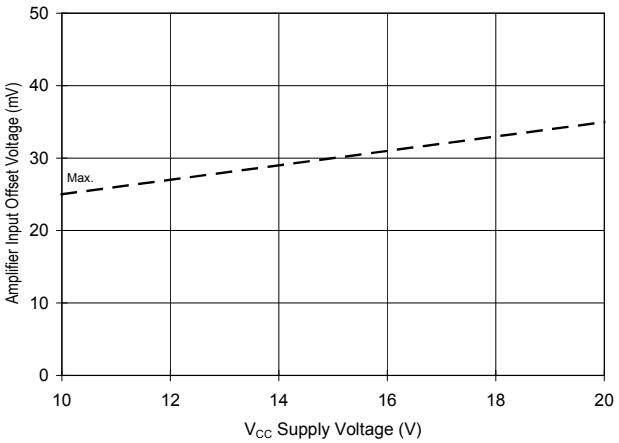


Fig 40b. Amplifier Input Offset Vs. Voltage

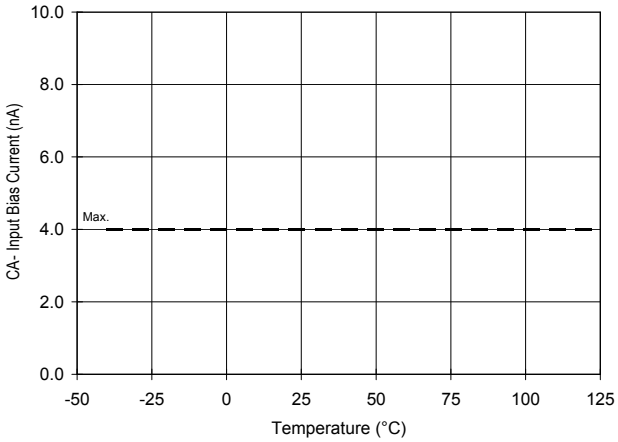


Fig 41a. CA- Input Current Vs. Temperature

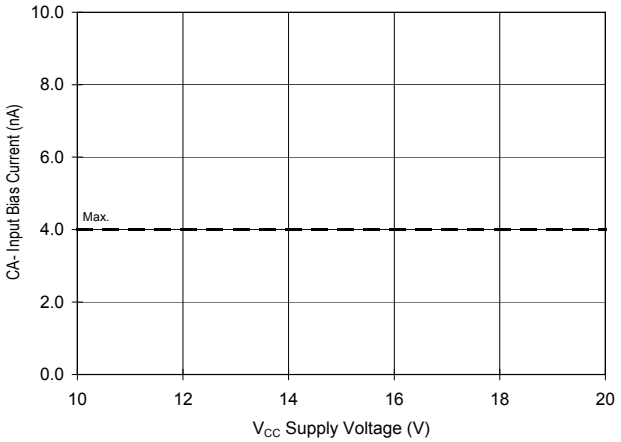


Fig 41b. CA- Input Current Vs. Voltage

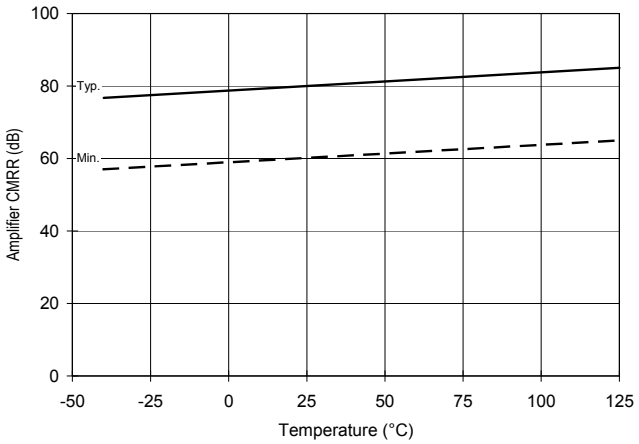


Fig 42a. Amplifier CMRR Vs. Temperature

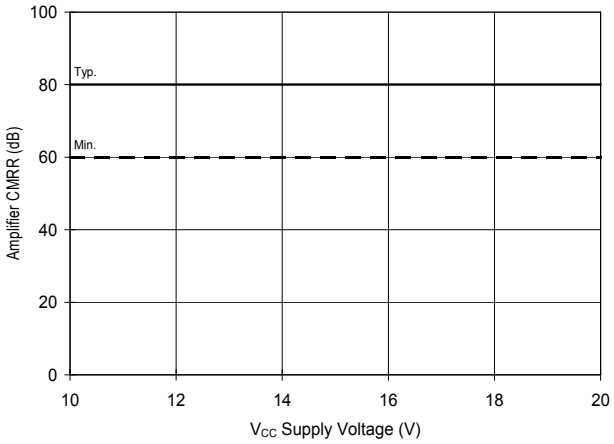


Fig 42b. Amplifier CMRR Vs. Voltage

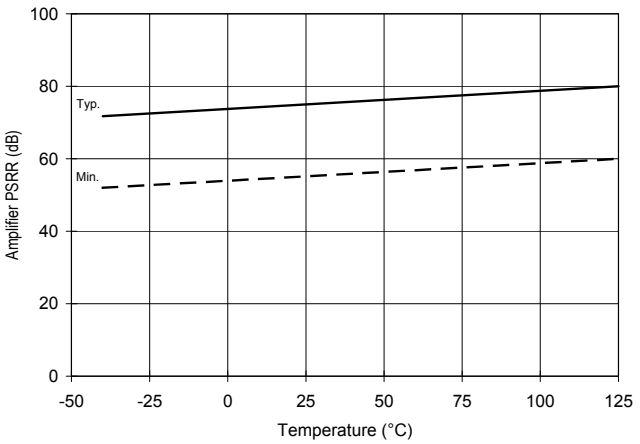


Fig 43a. Amplifier PSRR Vs. Temperature

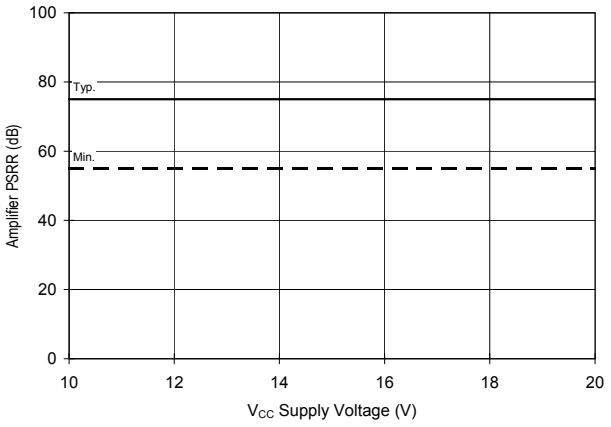


Fig 43b. Amplifier PSRR Vs. Voltage

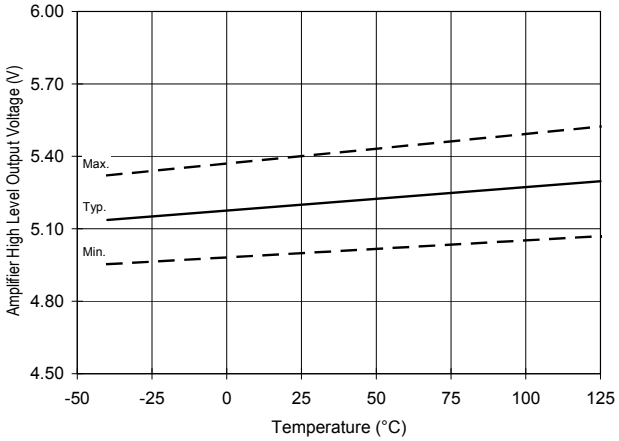


Fig 44a. Amplifier High Level Output Vs. Temperature

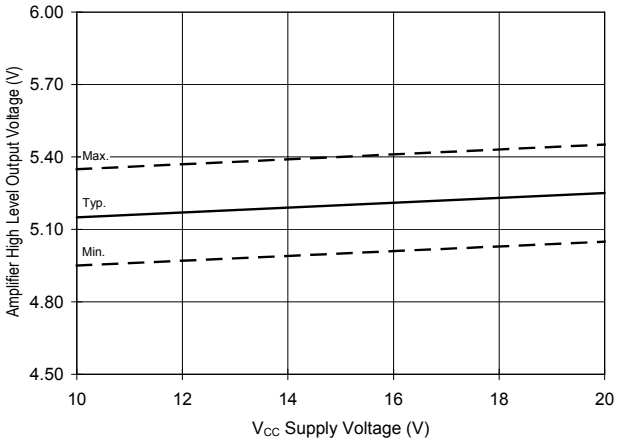


Fig 44b. Amplifier High Level Output Vs. Voltage

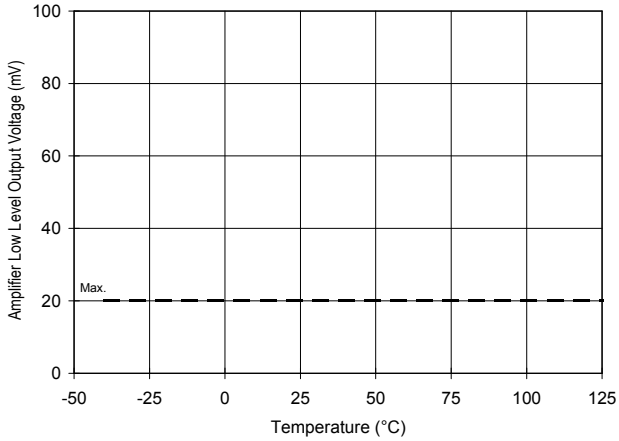


Fig 45a. Amplifier Low Level Output Vs. Temperature

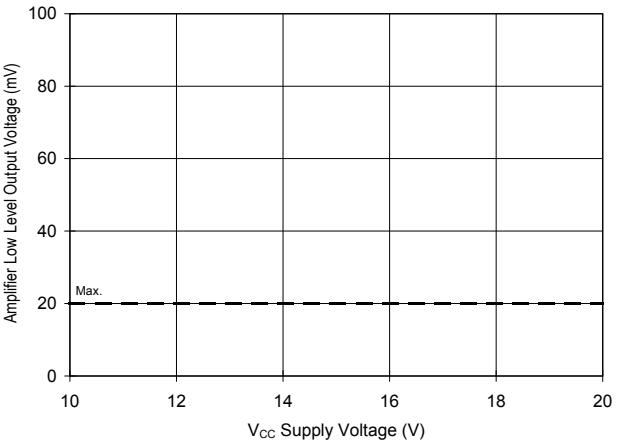


Fig 45b. Amplifier Low Level Output Vs. Voltage

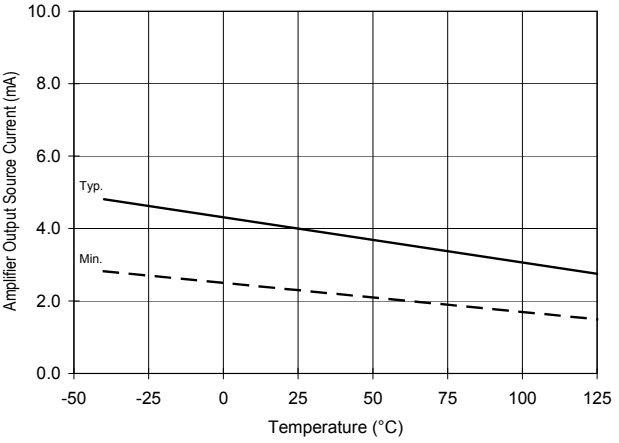


Fig 46a. Amplifier Output Source Current Vs. Temperature

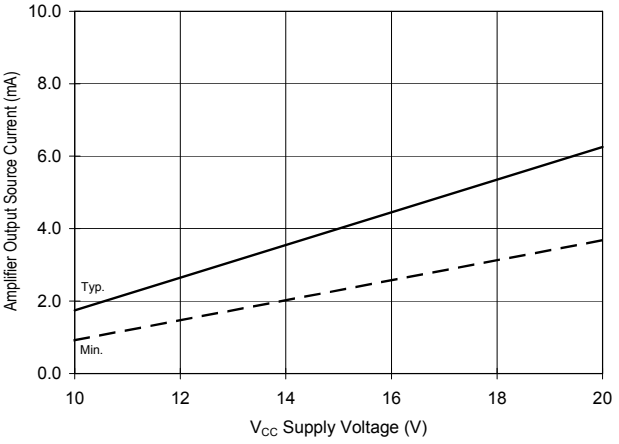


Fig 46b. Amplifier Output Source Current Vs. Voltage

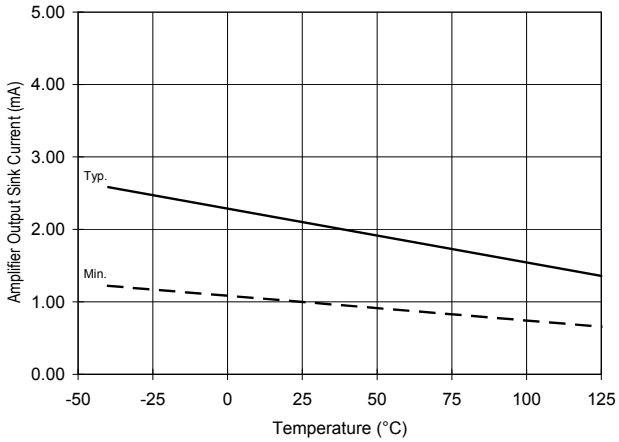


Fig 47a. Amplifier Output Sink Current Vs. Temperature

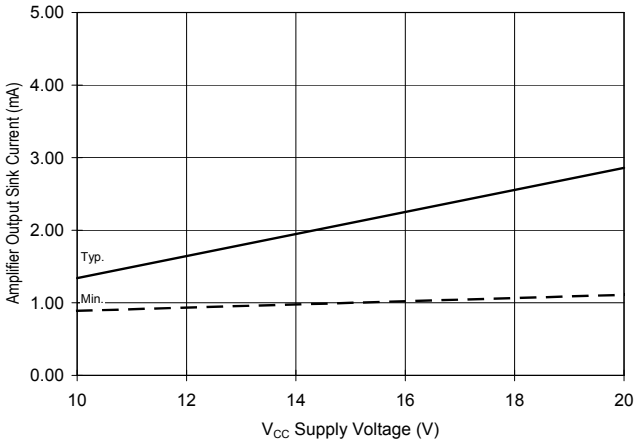


Fig 47b. Amplifier Output Sink Current Vs. Voltage

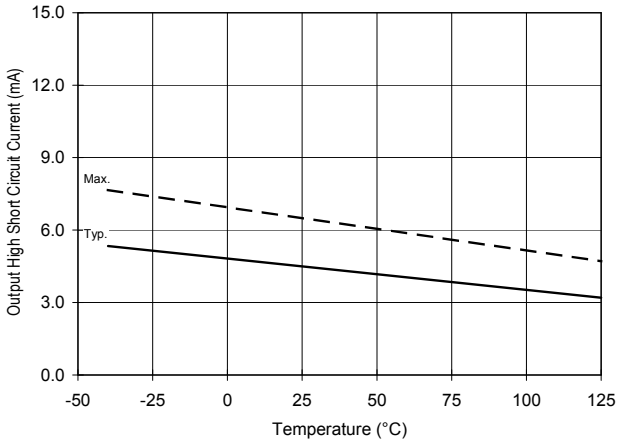


Fig 48a. Amplifier Output High Short Circuit Current Vs. Temperature

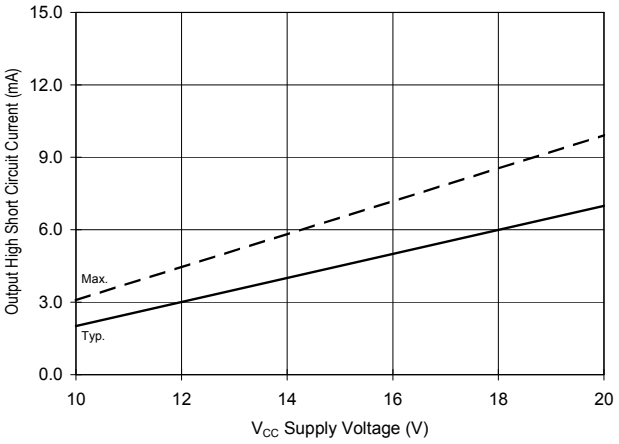


Fig 48b. Amplifier Output High Short Circuit Current Vs. Voltage

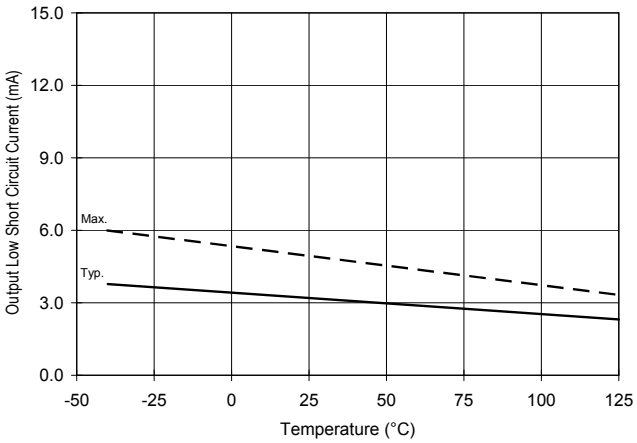


Fig 49a. Amplifier Output Low Short Circuit Current Vs. Temperature

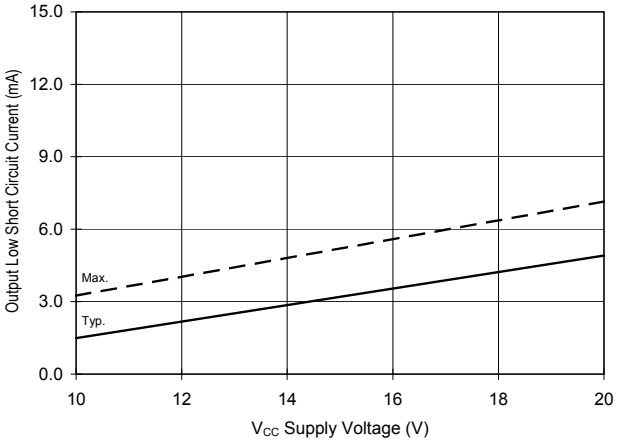


Fig 49b. Amplifier Output Low Short Circuit Current Vs. Voltage

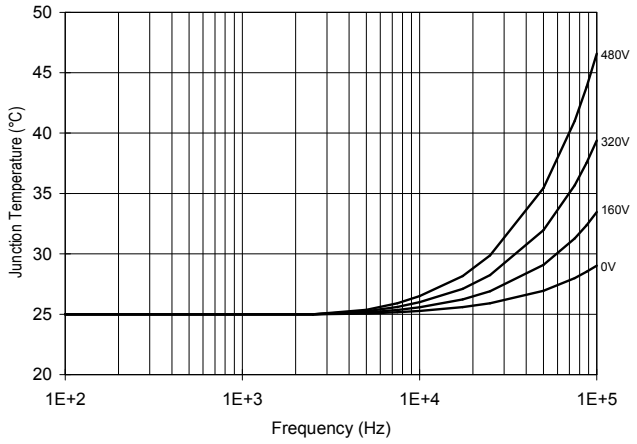


Fig 50. IR2130 T_J Vs. Frequency (IRF820)
R_{GATE} = 33Ω, V_{CC} = 15V

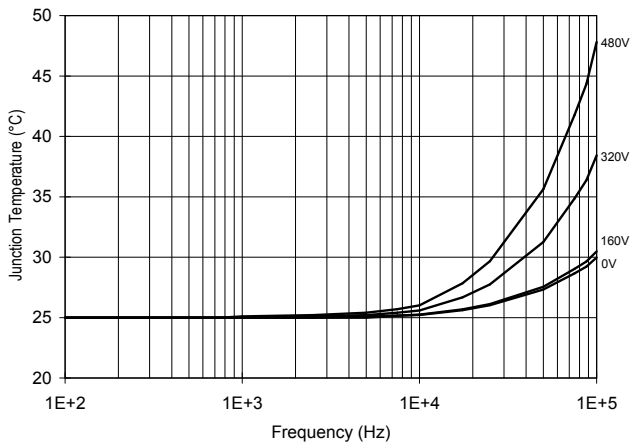


Fig 51. IR2130 T_J Vs. Frequency (IRF830)
R_{GATE} = 20Ω, V_{CC} = 15V

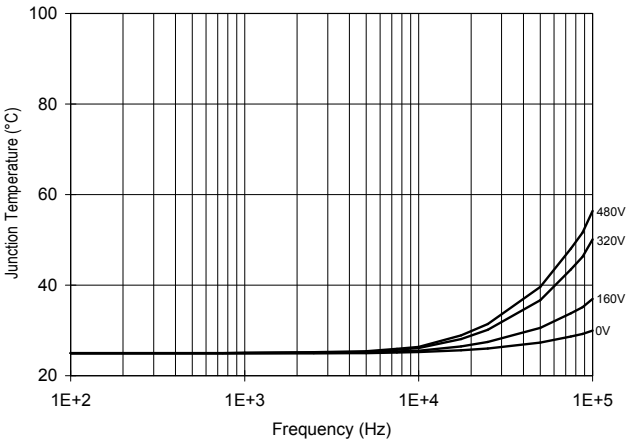


Fig 52. IR2130 T_J Vs. Frequency (IRF840)
R_{GATE} = 15Ω, V_{CC} = 15V

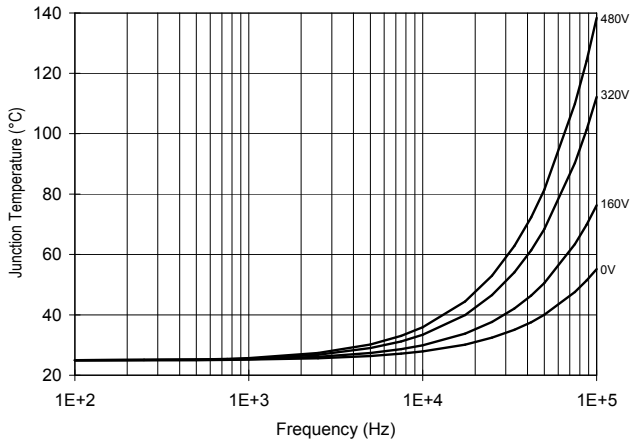


Fig 53. IR2130 T_J Vs. Frequency (IRF450)
R_{GATE} = 10Ω, V_{CC} = 15V

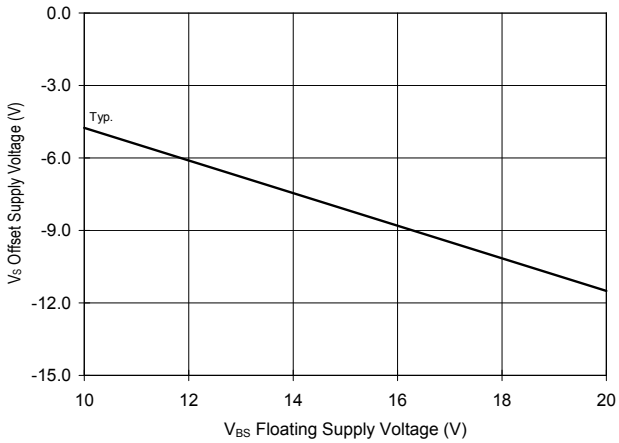
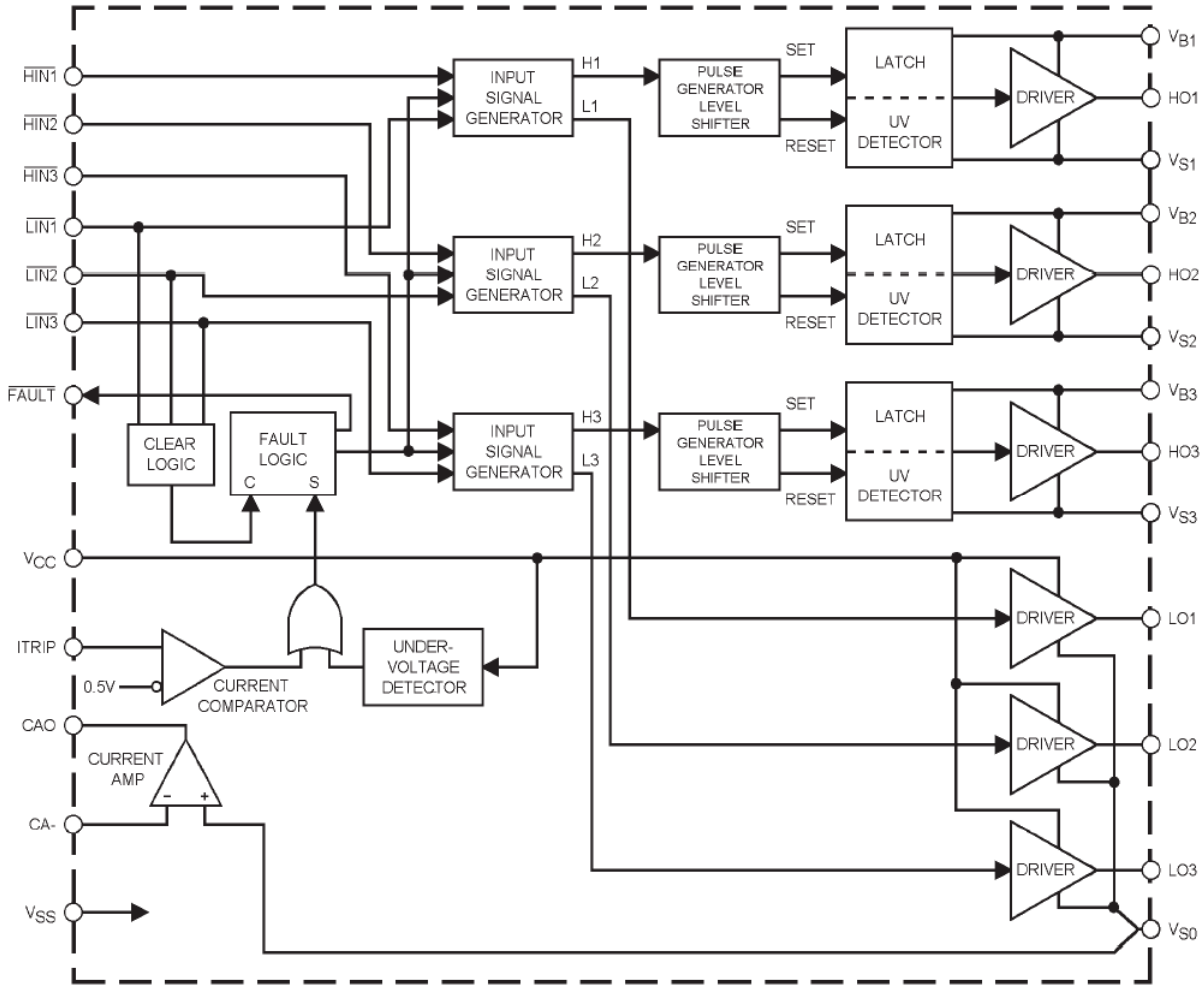


Fig 54. Maximum Vs Negative Offset Vs. V_{BS} Supply Voltage

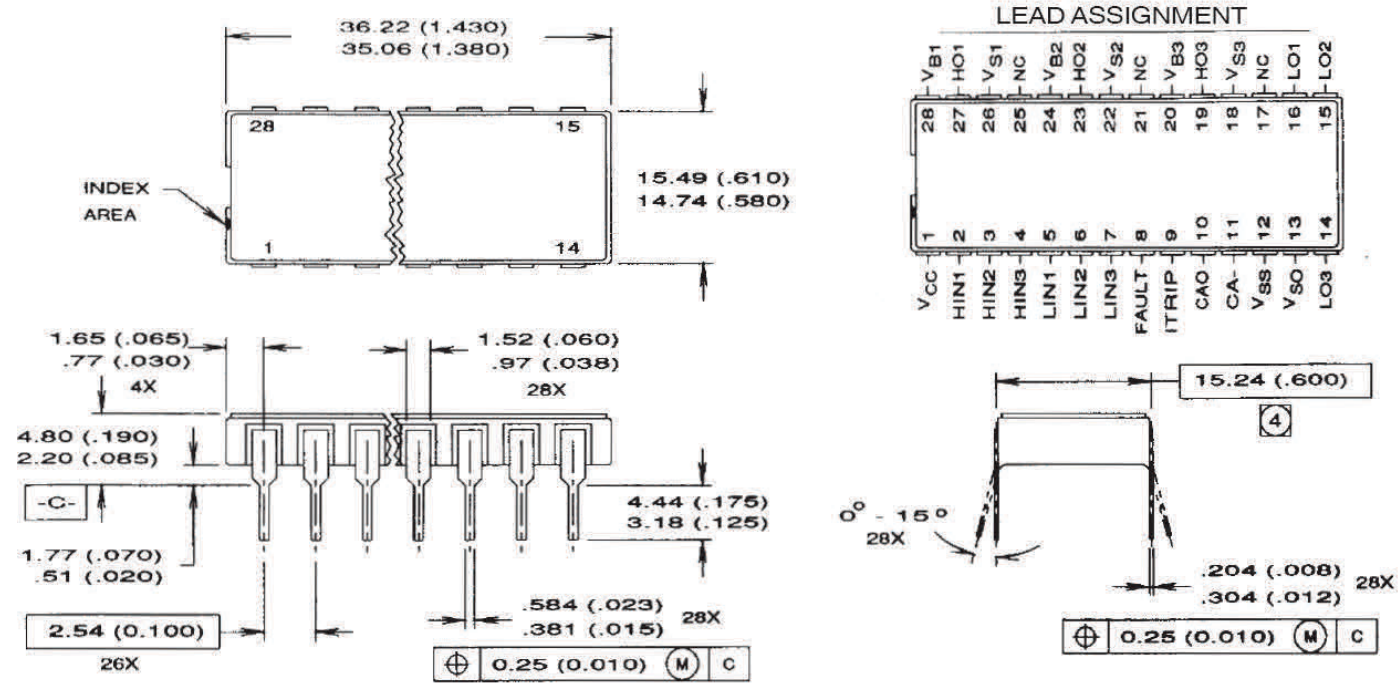
Functional Block Diagram



Lead Definitions

Symbol	Description
$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver output (LO1,2,3), out of phase
$\overline{FAULT}$	Indicates over-current or under voltage lockout (low side) has occurred, negative logic
V_{CC}	Low side and logic fixed supply
ITRIP	Input for over-current shutdown
CAO	Output of current amplifier
CA-	Negative input of current amplifier
V_{SS}	Logic ground
$V_{B1,2,3}$	High side floating supplies
$H_{O1,2,3}$	High side gate drive outputs
$V_{S1,2,3}$	High side floating supply returns
$L_{O1,2,3}$	Low side gate drive outputs
V_{SO}	Low side return and positive input of current amplifier

Case Outline and dimensions - MO-038AB



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

2 CONTROLLING DIMENSION : INCH.

3 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

4 DIMENSION IS TO CENTER OF LEADS WHEN FORMED PARALLEL.

5 OUTLINE CONFORMS TO JEDEC OUTLINE MO-038AB.

An Infineon Technologies Company

www.infineon.com/irhirel

Infineon Technologies Service Center: USA Tel: +1 (866) 951-9519 and International Tel: +49 89 234 65555
Leominster, Massachusetts 01453, USA Tel: +1 (978) 534-5776
San Jose, California 95134, USA Tel: +1 (408) 434-5000

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