EiceDRIVER™ 1EDI Compact

Single channel IGBT gate driver IC with clamp in wide body package

Features

- Single channel isolated gate driver
- For 600 V/650 V/1200 V IGBTs, MOSFETs, and SiC MOSFETs
- Up to 6 A typical peak current at rail-to-rail output
- Active Miller clamp
- Galvanically isolated coreless transformer driver
- Wide input voltage operating range
- Suitable for operation at high ambient temperature and in fast switching applications

Potential applications

- AC and brushless DC motor drives
- High voltage DC/DC-converter and DC/AC-inverter
- Induction heating resonant application
- UPS-systems
- Welding
- Solar

Product type	Minimum output current and configuration	Package
1EDI10I12MH	±1.0 A with 1.0 A Miller clamp	PG-DSO-8-59
1EDI20I12MH	±2.0 A with 2.0 A Miller clamp	PG-DSO-8-59
1EDI30I12MH	±3.0 A with 3.0 A Miller clamp	PG-DSO-8-59

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

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Description

The 1EDIxxI12MH are galvanically isolated single channel IGBT driver in a PG-DSO-8-59 package that provide output currents up to 3 A and an integrated active Miller clamp circuit with the same current rating to protect against parasitic turn on.

The input logic pins operate on a wide input voltage range from 3 V to 15 V using scaled CMOS threshold levels to support even 3.3 V microcontrollers.

Data transfer across the isolation barrier is realized by the coreless transformer technology.

Every driver family member comes with logic input and driver output undervoltage lockout (UVLO) and active shutdown.

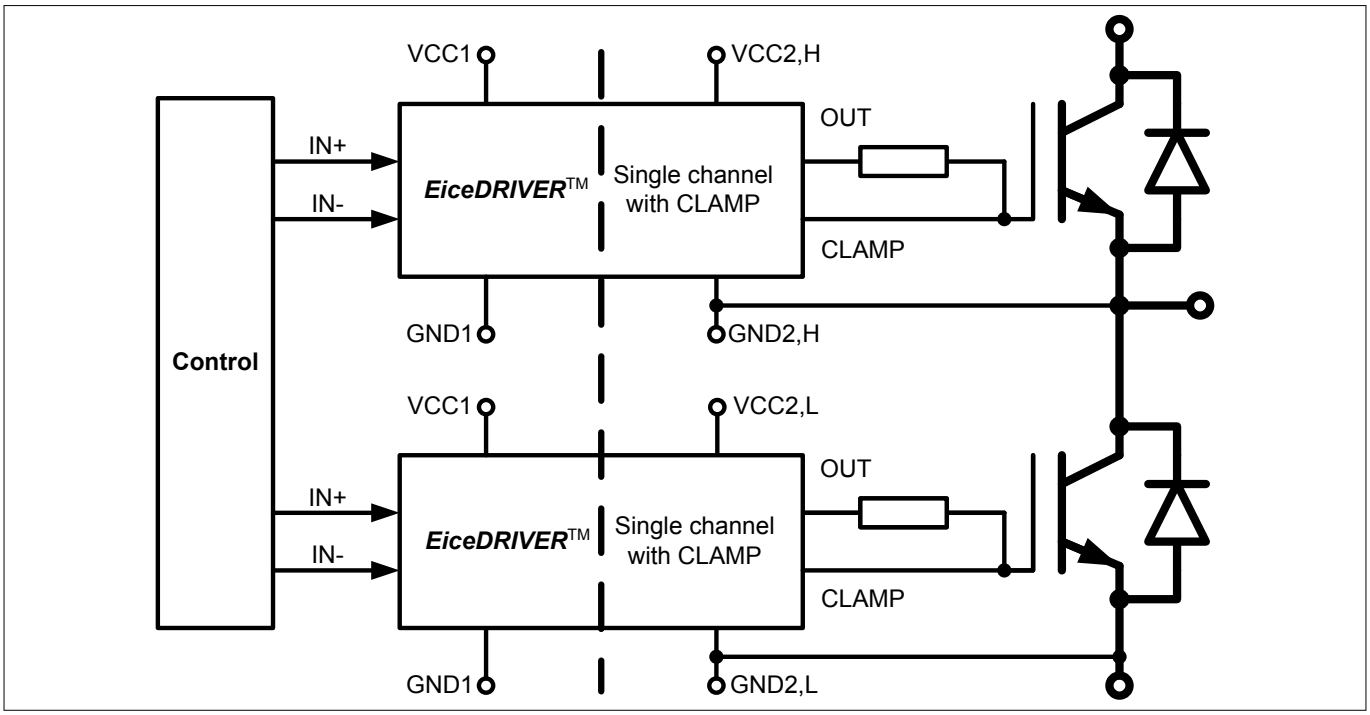

Figure 1 Typical application

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1 Block diagram

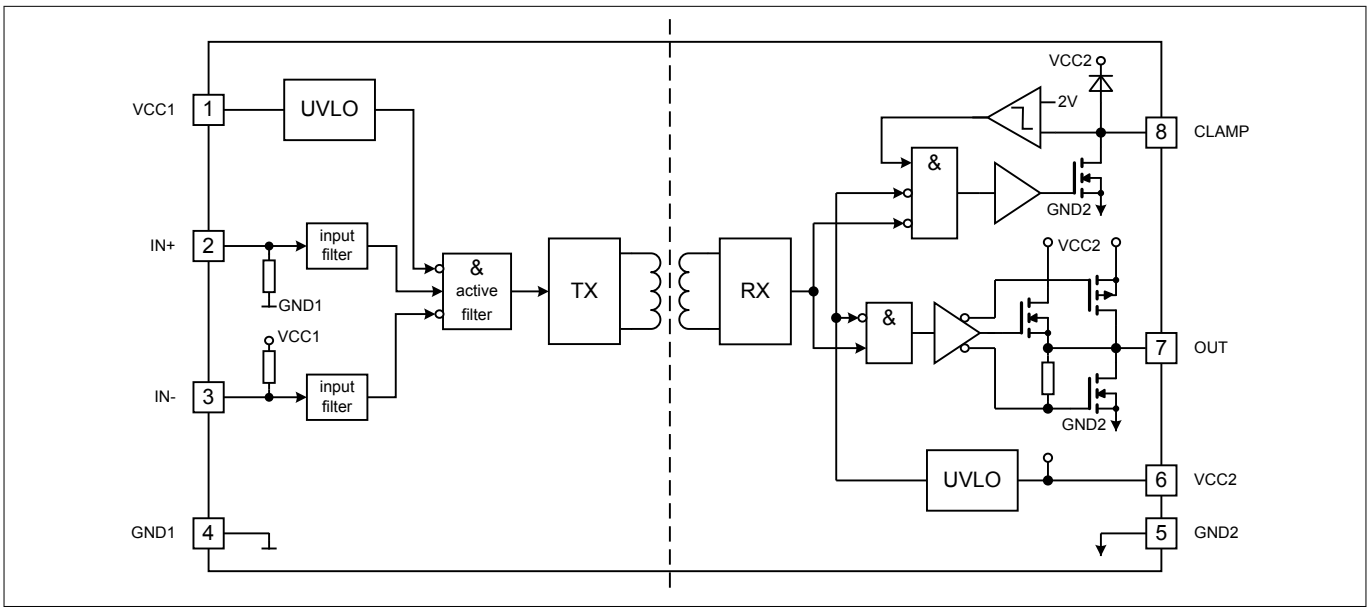

Figure 2 Block diagram

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2 Pin configuration and functionality

2.1 Pin configuration

Table 1 Pin configuration

Pin No.	Name	Function
1	*VCC1*	Positive logic supply
2	*IN+*	Non-inverted driver input (active high)
3	*IN-*	Inverted driver input (active low)
4	*GND1*	Logic ground
5	*GND2*	Power ground
6	*VCC2*	Positive power supply voltage
7	*OUT*	Driver output
8	*CLAMP*	Active Miller clamp

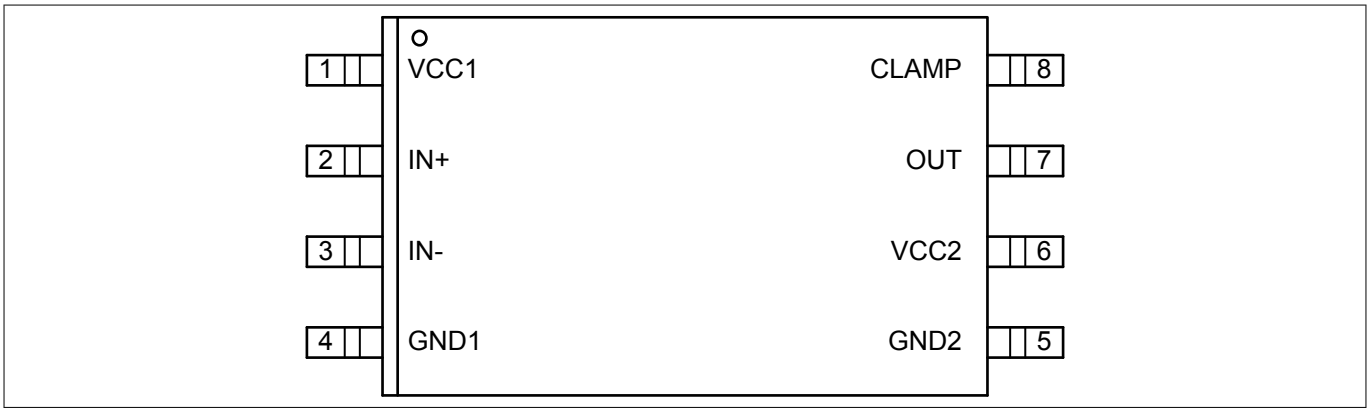

Figure 3 PG-DSO-8-59 (top view)

2.2 Pin functionality

VCC1

Logic input supply voltage of 3.3 V up to 15 V wide operating range.

IN+ non inverting driver input

IN+ non-inverted control signal for driver output if *IN-* is set to low. (Output sourcing active at *IN+* = high and *IN-* = low)

Due to internal filtering a minimum pulse width is defined to ensure robustness against noise at *IN+*. An internal weak pull-down-resistor favors off-state.

IN- inverting driver input

IN- inverted control signal for driver output if *IN+* is set to high. (Output sourcing active at *IN-* = low and *IN+* = high)

Due to internal filtering a minimum pulse width is defined to ensure robustness against noise at *IN-*. An internal weak pull-up-resistor favors off-state.

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GND1

Ground connection of input circuit.

GND2 reference ground

Reference ground of the output driving circuit.

VCC2

Positive power supply pin of output driving circuit. A proper blocking capacitor has to be placed close to this supply pin.

OUT driver output

Combined source and sink output pin to external IGBT. The output voltage will be switched between *VCC2* and *GND2* and is controlled by *IN+* and *IN-*. In case of an UVLO event this output will be switched off and an active shut down keeps the output voltage at a low level.

CLAMP active Miller clamp

Connect gate of external IGBT directly to this pin. As soon as the gate voltage has dropped below 2 V referred to *GND2* during turn off state the Miller clamp function ties its output to *GND2* to avoid parasitic turn on of the connected IGBT.

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3 Functional description

The 1EDIxxI12MH is a general purpose IGBT gate driver. Basic control and protection features support fast and easy design of highly reliable systems.

The integrated galvanic isolation between control input logic and driving output stage grants additional safety. Its wide input voltage supply range supports the direct connection of various signal sources like DSPs and microcontrollers.

With the rail-to-rail output and the additional active Miller clamp, dynamic turn on due to Miller capacitance is suppressed.

3.1 Supply

The driver can operate over a wide supply voltage range.

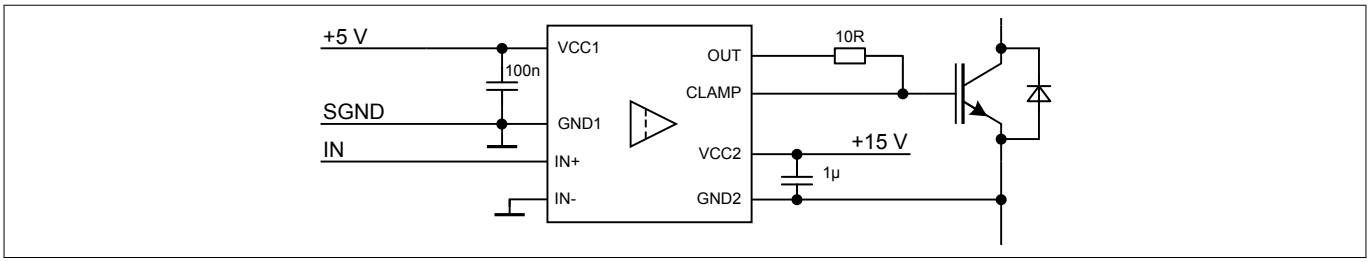

Figure 4 Application example

The typical positive supply voltage for the driver is 15 V at *VCC2*. Erratical dynamic turn on of the IGBT can be prevented with the active Miller clamp function, in which the *CLAMP* output is directly connected to the IGBT gate.

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3.2 Protection features

3.2.1 Undervoltage lockout (UVLO)

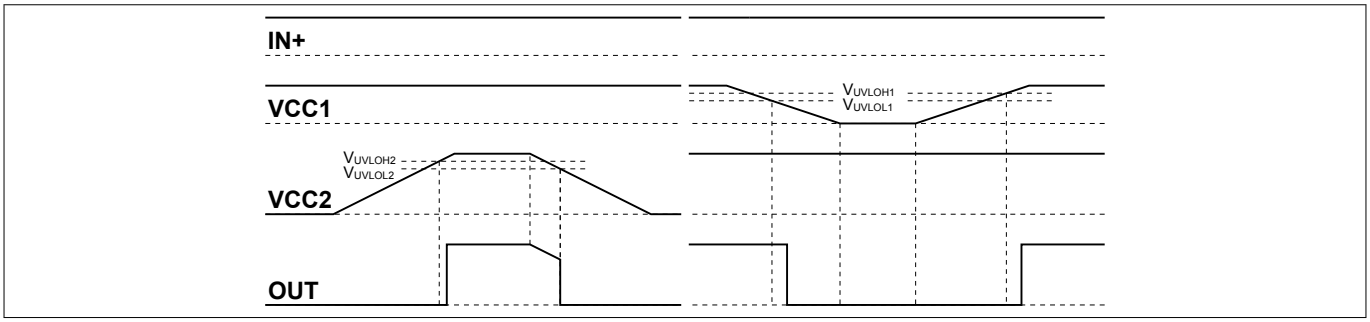

Figure 5 UVLO behavior

To ensure correct switching of IGBTs the device is equipped with an undervoltage lockout for input and output independently. Operation starts only after both VCC levels have increased beyond the respective V_{UVLOH} levels

If the power supply voltage V_{VCC1} of the input chip drops below V_{UVLOL1} a turn-off signal is sent to the output chip before power-down. The IGBT is switched off and the signals at *IN+* and *IN-* are ignored until V_{VCC1} reaches the power-up voltage V_{UVLOH1} again.

If the power supply voltage V_{VCC2} of the output chip goes down below V_{UVLOL2} the IGBT is switched off and signals from the input chip are ignored until V_{VCC2} reaches the power-up voltage V_{UVLOH2} again.

3.2.2 Active shut-down

The active shut-down feature ensures a safe IGBT off-state if the output chip is not connected to the power supply or an undervoltage lockout is in effect. The IGBT gate is clamped at *OUT* to *GND2*.

3.2.3 Short circuit clamping

During short circuit the IGBT's gate voltage tends to rise because of the feedback via the Miller capacitance. An additional protection circuit connected to *OUT* and *CLAMP* limits this voltage to a value slightly higher than the supply voltage. A maximum current of 500 mA may be fed back to the supply through one of these paths for 10 µs. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

3.2.4 Active Miller clamp

In a half bridge configuration the switched off IGBT tends to dynamically turn on during turn on phase of the opposite IGBT. A Miller clamp allows sinking the Miller current across a low impedance path in this high dV/dt situation. Therefore in many applications, the use of a negative supply voltage can be avoided. During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage drops below typical 2 V (referred to *GND2*). The clamp is designed for a Miller current in the same range as the nominal output current.

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3.3 Non-inverting and inverting inputs

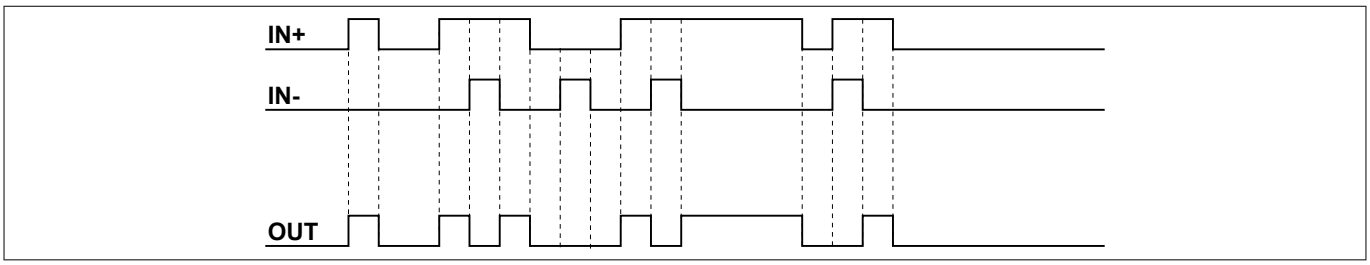

Figure 6 Logic input to output switching behavior

There are two possible input modes to control the IGBT. At non-inverting mode *IN+* controls the driver output while *IN-* is set to low. At inverting mode *IN-* controls the driver output while *IN+* is set to high. A minimum input pulse width is defined to filter occasional glitches.

3.4 Driver output

The output driver section uses MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the driver's supply is stable. Due to the low internal voltage drop, switching behavior of the IGBT is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated by the driver.

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4 Electrical parameters

4.1 Absolute maximum ratings

Note: *Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND1*

Table 2 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note or Test Condition
		Min.	Max.		
Power supply output side	V_{VCC2}	-0.3	20[1)]	V	[2)]
Gate driver output	V_{OUT}	V_{GND2}-0.3	V_{VCC2}+0.3	V	[2)]
Maximum short circuit clamping time	t_{CLP}	–	10	µs	$I_{CLAMP/OUT}$ = 500 mA
Positive power supply input side	V_{VCC1}	-0.3	18.0	V	–
Logic input voltages (IN+,IN-)	$V_{LogicIN}$	-0.3	18.0	V	–
Pin CLAMP voltage	V_{CLAMP}	-0.3	V_{VCC2} +0.3[1)]	V	[2)]
Input to output isolation voltage (GND2)	V_{GND2}	-1200	1200	V	*GND2 - GND1*
Junction temperature	T_J	-40	150	°C	–
Storage temperature	T_S	-55	150	°C	–
Comparative tracking index	*CTI*	400	–		IEC 60601-1: Material group II
Power dissipation (Input side)	$P_{D, IN}$	–	25	mW	[3)] @T_A = 25°C
Power dissipation (Output side)	$P_{D, OUT}$	–	400	mW	[3)] @T_A = 25°C
Thermal resistance (Input side)	$R_{THJA,IN}$	–	145	K/W	[3)] @T_A = 85°C
Thermal resistance (Output side)	$R_{THJA,OUT}$	–	165	K/W	[3)] @T_A = 85°C
ESD capability	$V_{ESD,HBM}$	–	2	kV	Human body model[4)]
	$V_{ESD,CDM}$	–	1	kV	Charged device model[5)]

1 May be exceeded during short circuit clamping.
2 With respect to *GND2*.
3 See ***Figure 10*** for reference layouts for these thermal data. Thermal performance may change significantly with layout and heat dissipation of components in close proximity.
4 According to EIA/JESD22-A114-C (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).
5 According to EIA/JESD22-C101 (specified waveform characteristics)

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4.2 Operating parameters

Note: *Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND1.*

Table 3 Operating parameters

Parameter	Symbol	Values		Unit	Note or Test Condition
		Min.	Max.		
Power supply output side	V_{VCC2}	13	18	V	6)
Power supply input side	V_{VCC1}	3.1	17	V	–
Logic input voltages (IN+,IN-)	$V_{LogicIN}$	-0.3	17	V	–
Pin CLAMP voltage	V_{CLAMP}	V_{GND2}-0.3	V_{VCC2} 7)	V	6)
Switching frequency	f_{sw}	–	1.0	MHz	8)9)
Ambient temperature	T_A	-40	125	°C	–
Thermal coefficient, junction-top	$\Psi_{th,jt}$	–	4.8	K/W	9)@T_A = 85°C
Common mode transient immunity	$\lvert dV_{ISO}/dt \rvert$	–	100	kV/µs	9) @ 1000 V

4.3 Electrical characteristics

Note: *The electrical characteristics include the spread of values in supply voltages, load and junction temperatures given below. Typical values represent the median values at T_A = 25°C. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 3, GND2 for pins 6 to 8).*

4.3.1 Voltage supply

Table 4 Voltage supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
UVLO threshold input chip	V_{UVLOH1}	–	2.85	3.1	V	–
	V_{UVLOL1}	2.55	2.75	–	V	–
UVLO hysteresis input chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS1}	0.09	0.10	–	V	–

6 With respect to *GND2*.
7 May be exceeded during short circuit clamping.
8 do not exceed max. power dissipation
9 Parameter is not subject to production test - verified by design/characterization

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Table 4 Voltage supply (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
UVLO threshold output chip (IGBT supply)	V_{UVLOH2}	–	11.9	12.7	V	*10)*
	V_{UVLOL2}	10.5	11.0	–	V	*10)*
UVLO hysteresis output chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS2}	0.7	0.85	–	V	–
Quiescent current input chip	I_{Q1}	–	0.6	1	mA	V_{VCC1} = 5 V *IN+* = High, *IN-* = Low =>*OUT* = High
Quiescent current output chip	I_{Q2}	–	1.2	2	mA	V_{VCC2} = 15 V *IN+* = High, *IN-* = Low =>*OUT* = High

4.3.2 Logic input

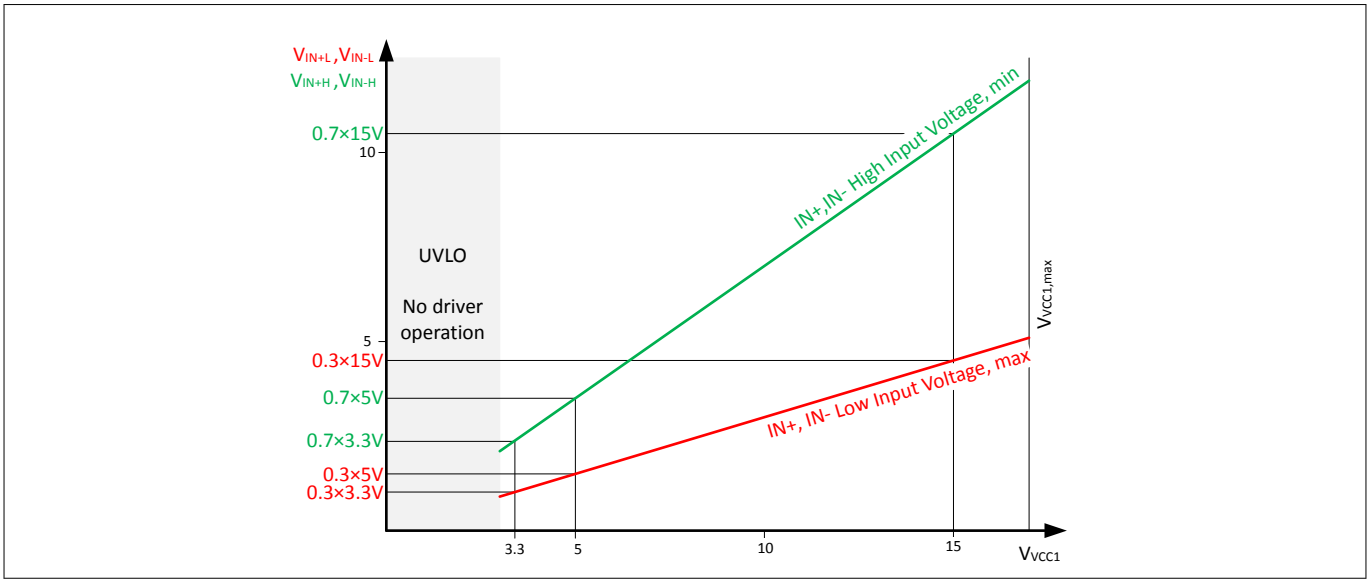

Figure 7 *VCC1* scaled input threshold voltage of *IN+* and *IN-*

Beginning from the input undervoltage lockout level, threshold levels for *IN+* and *IN-* are scaled to V_{VCC1}. The high input threshold is 70% of V_{VCC1} and the low input threshold is at 30% of V_{VCC1}.

10 With respect to *GND2*.

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Table 5 Logic input

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
IN+,*IN-* low input voltage	V_{IN+L}, V_{IN-L}	–	–	0.3 × V_{VCC1}		[11] 3.1 V ≤ V_{VCC1} ≤ 17 V
IN+,*IN-* high input voltage	V_{IN+H}, V_{IN-H}	0.7 × V_{VCC1}	–	–		
IN+,*IN-* low input voltage	V_{IN+L}, V_{IN-L}	–	–	1.5	V	V_{VCC1} = 5.0 V
IN+,*IN-* high input voltage	V_{IN+H}, V_{IN-H}	3.5	–	–	V	
IN- input current	I_{IN-}	–	70	200	µA	V_{VCC1} = 5.0 V, V_{IN-} = *GND1*
IN+ input current	I_{IN+}	–	70	200	µA	V_{VCC1} = 5.0 V, V_{IN+} = V_{VCC1}

4.3.3 Gate driver

Note: *minimum Peak current rating valid over temperature range!*

Table 6 Gate driver

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level output peak current (source)	$I_{OUT,H,PEAK}$			–	A	[12] *IN+* = High, *IN-* = Low, V_{VCC2} = 15 V
1EDI10I12MH		1.0	2.2			
1EDI20I12MH		2.0	4.4			
1EDI30I12MH		3.0	5.9			
Low level output peak current (sink)	$I_{OUT,L,PEAK}$			–	A	[12] *IN+* = Low, *IN-* = Low, V_{VCC2} = 15 V
1EDI10I12MH		1.0	2.3			
1EDI20I12MH		2.0	4.1			
1EDI30I12MH		3.0	6.2			

11 Parameter is not subject to production test - verified by design/characterization

12 specified min. output current is forced; voltage across the device $V_{(VCC2 - OUT)}$ or $V_{(OUT - GND2)}$ < V_{VCC2}.

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4.3.4 Short circuit clamping

Table 7 Short circuit clamping

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Clamping voltage (*OUT*) (V_{OUT} - V_{VCC2})	V_{CLPout}	–	0.9	1.3	V	[13] *IN+* = High, *IN-* = Low, I_{OUT} = 500 mA (pulse test t_{CLPmax} = 10 µs)
Clamping voltage (*CLAMP*) (V_{VCLAMP} - V_{VCC2})	$V_{CLPclamp1}$	–	1.3	–	V	[13] *IN+* = High, *IN-* = Low, I_{CLAMP} = 500 mA (pulse test t_{CLPmax} = 10 µs)
Clamping voltage (*CLAMP*)	$V_{CLPclamp2}$	–	0.7	1.1	V	[13] *IN+* = High, *IN-* = Low, I_{CLAMP} = 20 mA

4.3.5 Active Miller clamp

Table 8 Active Miller clamp

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Low level clamp current 1EDI10I12MH 1EDI20I12MH 1EDI30I12MH	$I_{CLAMP,PEAK}$	 1.0 2.0 3.0	–	–	A	[14] *IN+* = Low, *IN-* = Low, V_{CLAMP} = 15 V pulsed t_{pulse} = 2 µs
Clamp threshold voltage	V_{CLAMP}	1.6	2.0	2.4	V	[15]

13 With respect to *GND2*.
14 Parameter is not subject to production test - verified by design/characterization
15 With respect to *GND2*.

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4.3.6 Dynamic characteristics

Dynamic characteristics are measured with V_{VCC1} = 5 V and V_{VCC2} = 15 V.

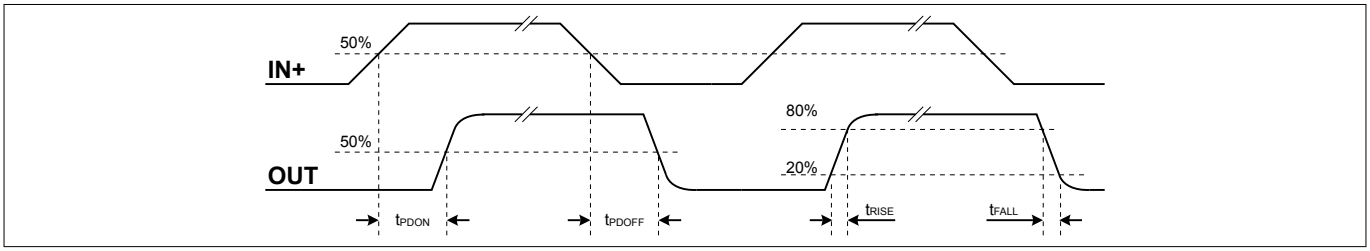

Figure 8 Propagation delay, rise and fall time

Table 9 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input IN to output propagation delay ON	t_{PDON}	270	300	330	ns	C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50% @ 25°C
Input IN to output propagation delay OFF	t_{PDOFF}	270	300	330	ns	
Input IN to output propagation delay distortion (t_{PDOFF} - t_{PDON})	t_{PDISTO}	-30	5	40	ns	
Input pulse suppression time *IN+*, *IN-*	t_{MININ+}, t_{MININ-}	230	240	–	ns	
IN input to output propagation delay ON variation due to temp	t_{PDONt}	–	–	14	ns	[16] C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT} =50%
IN input to output propagation delay OFF variation due to temp	t_{PDOFFt}	–	–	14	ns	
IN input to output propagation delay distortion variation due to temp (t_{PDOFF}-t_{PDON})	$t_{PDISTOt}$	–	–	8	ns	
Rise time	t_{RISE}	5	10	20	ns	C_{LOAD} = 1 nF V_L 20%, V_H 80%
Fall time	t_{FALL}	3	9	19	ns	

4.3.7 Active shut down

Table 10 Active shut down

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Active shut down voltage	V_{ACTSD}	–	2.0	2.3	V	[17] $I_{OUT-}/I_{OUT-,PEAK}$=0.1, *VCC2* open

16 Parameter is not subject to production test - verified by design/characterization
17 With respect to *GND2*.

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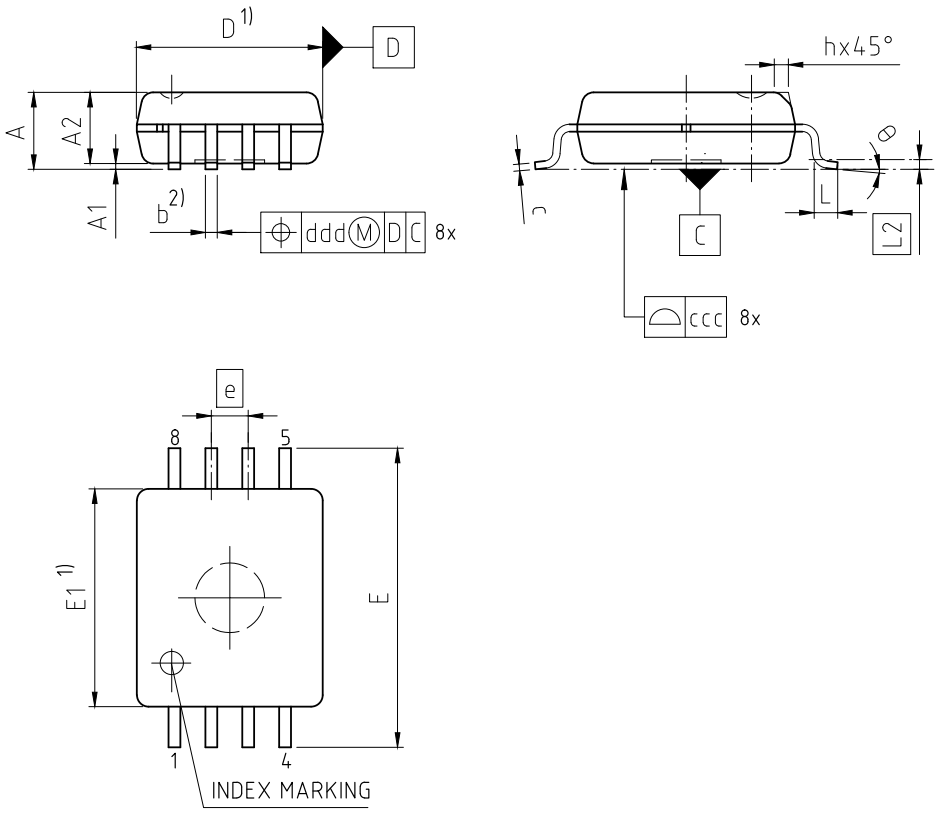
5 Package outline



1) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSIONS OF MAX 0.15MM PER SIDE.
2) DOES NOT INCLUDE DAMBAR PROTRUSION OF MAX 0.10MM.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	2.65	-	0.104
A1	0.10	0.20	0.004	0.008
A2	2.25	2.45	0.089	0.096
b	0.30	0.50	0.012	0.020
c	0.23	0.32	0.009	0.013
D	6.20	6.40	0.244	0.252
E	10.00	10.60	0.394	0.417
E1	7.40	7.60	0.291	0.299
e	1.27 BSC		0.050 BSC	
N	8		8	
L	0.50	0.90	0.020	0.035
L2	0.25 BSC		0.010 BSC	
h	0.25	0.45	0.010	0.018
Θ	0°	8°	0°	8°
ccc	0.10		0.004	
ddd	0.25		0.010	

DOCUMENT NO.
Z8B00179262

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Figure 9 PG-DSO-8-59 (Plastic (green) dual small outline package)

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6 Application notes

6.1 Reference layout for thermal data

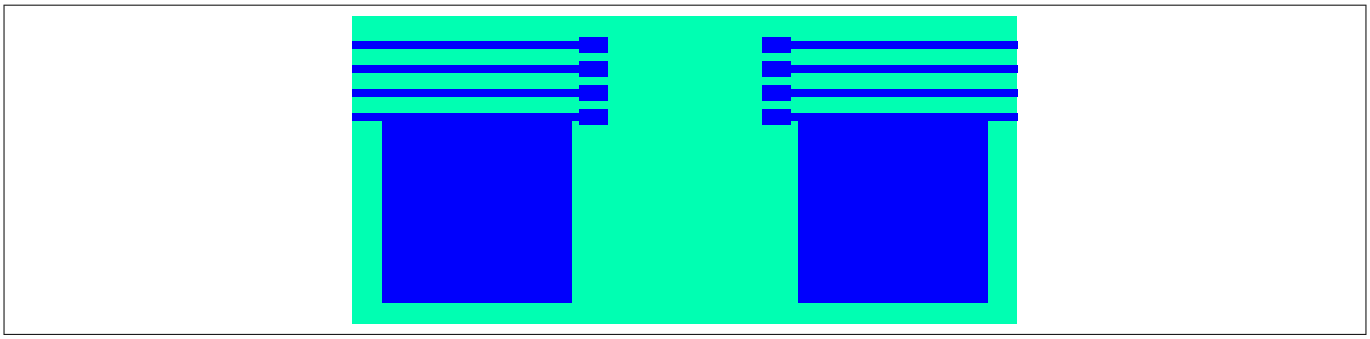

Figure 10 Reference layout for thermal data (Copper thickness 35 µm)

This PCB layout represents the reference layout used for the thermal characterization.

Pin 4 (*GND1*) and pin 5 (*GND2*) require each a ground plane of 100 mm² for achieving maximum power dissipation. The package is built to dissipate most of the heat generated through these pins.

The thermal coefficient junction-top ($\Psi_{th,jt}$) can be used to calculate the junction temperature at a given top case temperature and driver power dissipation:

$T_j = \Psi_{th,jt} \cdot P_D + T_{top}$

6.2 Printed circuit board guidelines

The following factors should be taken into account for an optimum PCB layout.

- Sufficient spacing should be kept between high voltage isolated side and low voltage side circuits.
- The same minimum distance between two adjacent high-side isolated parts of the PCB should be maintained to increase the effective isolation and to reduce parasitic coupling.
- In order to ensure low supply ripple and clean switching signals, bypass capacitor trace lengths should be kept as short as possible.

Revision history

Document version	Date of release	Description of changes
2.1	2017-09-04	Increase of typical gate driver output current values; formatting updated for electrical parameters and pins
2.0	2016-07-05	Extended description of VCC1 scaled input thresholds
1.0	2016-04-14	Missing electrical product parameters updated

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