

MOSFET

OptiMOS™ 2 Small-Signal-Transistor, 30 V

Features

- Dual N-channel
- Enhancement mode
- Logic level (4.5V rated)
- Avalanche rated
- Qualified according to AEC Q101
- 100% lead-free; RoHS compliant
- Halogen-free according to IEC61249-2-21

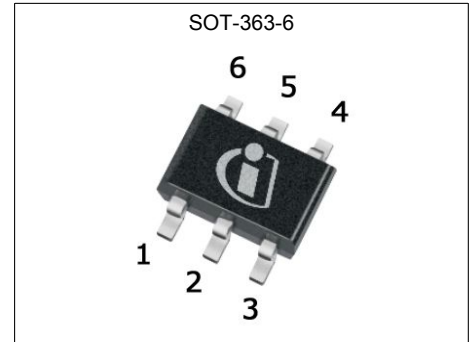
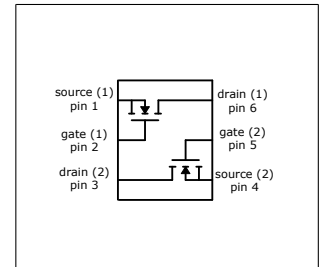


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}, V_{GS}=4.5\text{ V}$	600	$m\Omega$
$R_{DS(on),max}, V_{GS}=10\text{ V}$	400	$m\Omega$
I_D	0.88	A



Type / Ordering Code	Package	Marking	Related Links
BSD340N	PG-SOT363	XGs	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified, only one of both transistors in operation.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	0.88 0.71	A	$T_A=25\text{ °C}$ $T_A=70\text{ °C}$
Pulsed drain current	$I_{D,pulse}$	-	-	3.5	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	1.6	mJ	$I_D=0.88\text{ A}$, $R_{GS}=16\text{ }\Omega$
Reverse diode dv/dt	dv/dt	-	-	6	kV/ μ s	$I_D=0.88\text{ A}$, $V_{DS}=16\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=150\text{ °C}$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	0.5	W	$T_A=25\text{ °C}$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56
ESD Class	-	-	0	-	-	JESD22-A114 -HBM, ESD Class 0 = < 250V
Soldering Temperature	-	-	260	-	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - ambient, minimal footprint ¹⁾	R_{thJA}	-	-	250	K/W	-

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.0	V	$V_{DS}=0\text{ V}$, $I_D=1.6\text{ }\mu\text{A}$
Drain-source leakage current	I_{DSS}	-	-	0.01 5	A	$V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	10	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	447 286	600 400	m Ω	$V_{GS}=4.5\text{ V}$, $I_D=0.29\text{ A}$ $V_{GS}=10\text{ V}$, $I_D=0.88\text{ A}$
Transconductance	g_{fs}	-	1.2	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=0.71\text{ A}$

¹⁾ Performed on 40 mm x 40 mm FR4 PCB. The traces are 1mm wide, 70m thick and 20mm long; they are present on both sides of the PCB

Table 5 Dynamic characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	31	41	pF	$V_{GS}=0\text{ V}$, $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	12	16	pF	$V_{GS}=0\text{ V}$, $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	2.4	3.6	pF	$V_{GS}=0\text{ V}$, $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	2.6	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=0.88\text{ A}$, $R_{G,ext}=6\ \Omega$
Rise time	t_r	-	6.3	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=0.88\text{ A}$, $R_{G,ext}=6\ \Omega$
Turn-off delay time	$t_{d(off)}$	-	4.6	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=0.88\text{ A}$, $R_{G,ext}=6\ \Omega$
Fall time	t_f	-	2.5	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=0.88\text{ A}$, $R_{G,ext}=6\ \Omega$

Table 6 Gate charge characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	0.11	0.15	nC	$V_{DD}=15\text{ V}$, $I_D=0.88\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	0.08	0.1	nC	$V_{DD}=15\text{ V}$, $I_D=0.88\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	-	0.46	0.7	nC	$V_{DD}=15\text{ V}$, $I_D=0.88\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	3.6	-	V	$V_{DD}=15\text{ V}$, $I_D=0.88\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	0.45	A	$T_A=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	3.5	A	$T_A=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.89	1.1	V	$V_{GS}=0\text{ V}$, $I_F=0.88\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	7.8	-	ns	$V_R=15\text{ V}$, $I_F=0.88\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	1.9	-	nC	$V_R=15\text{ V}$, $I_F=0.88\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subjected to production test.

4 Electrical characteristics diagrams

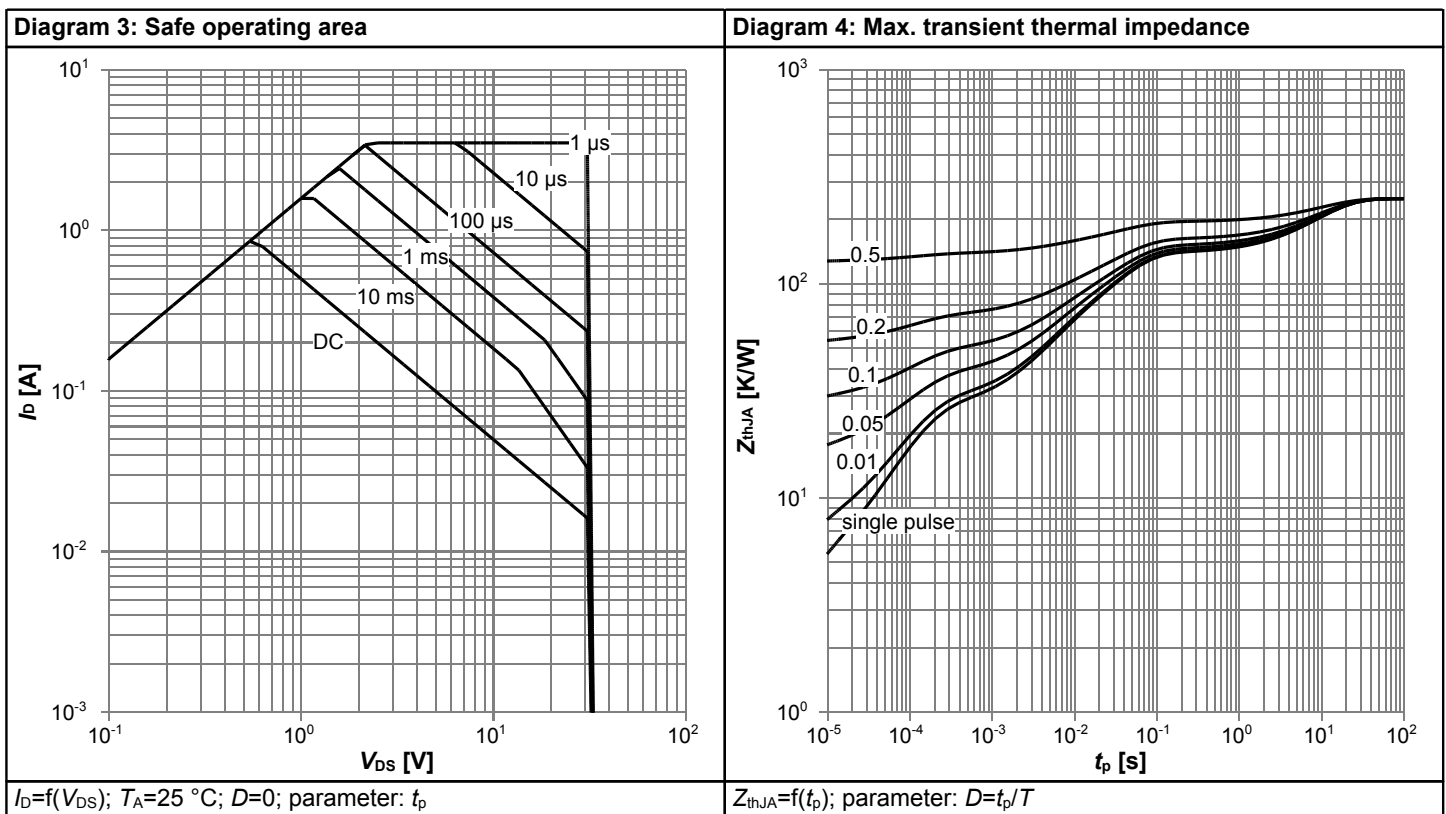
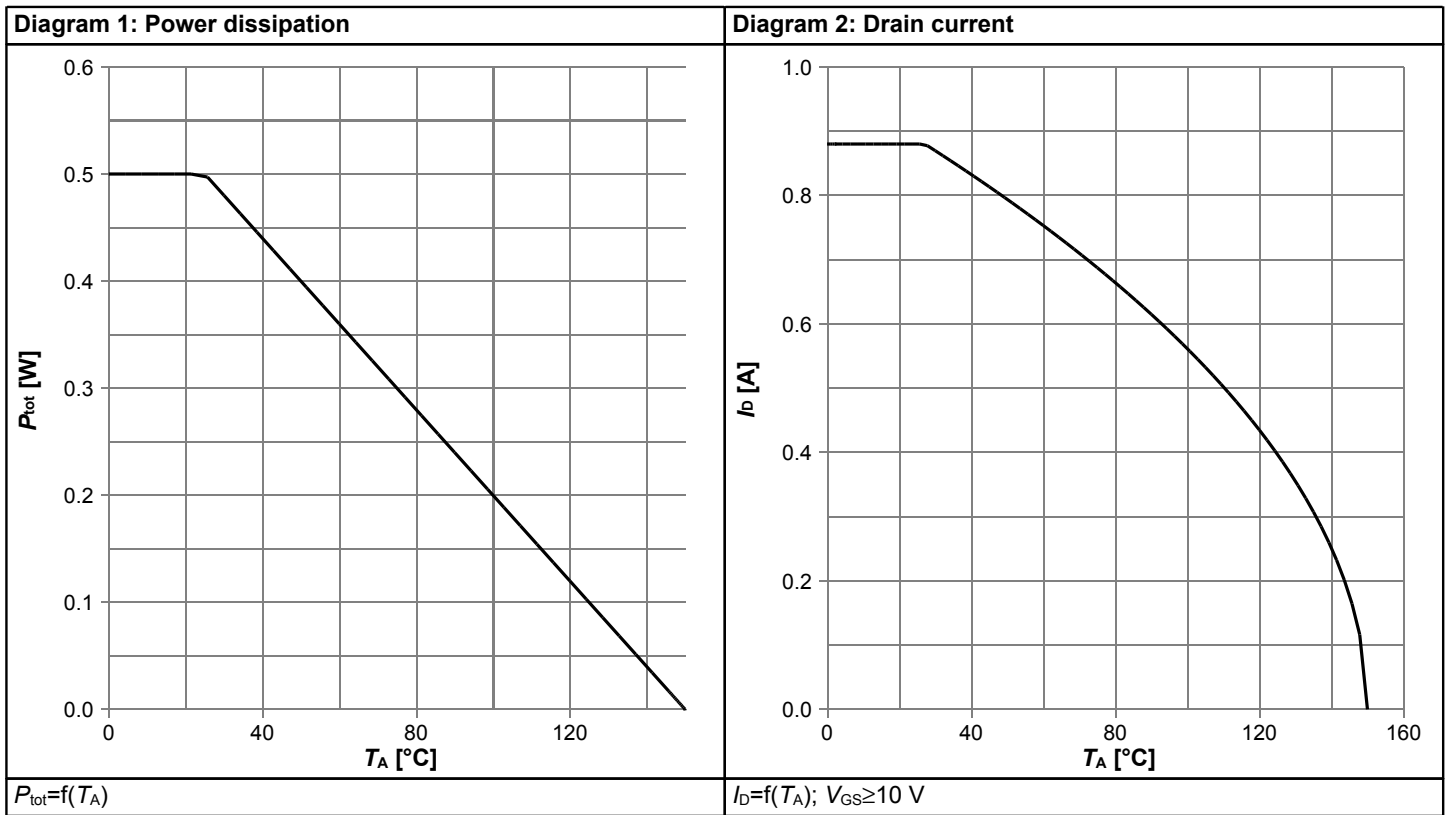
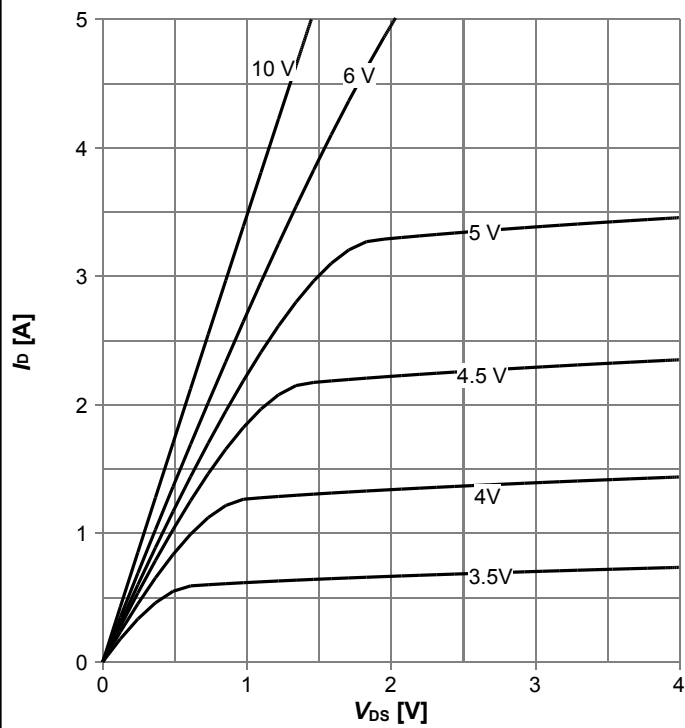
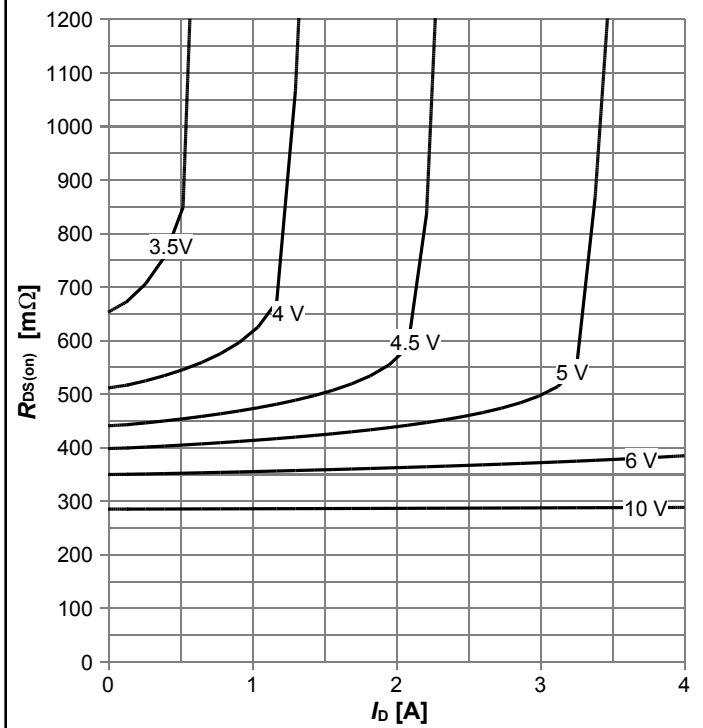


Diagram 5: Typ. output characteristics



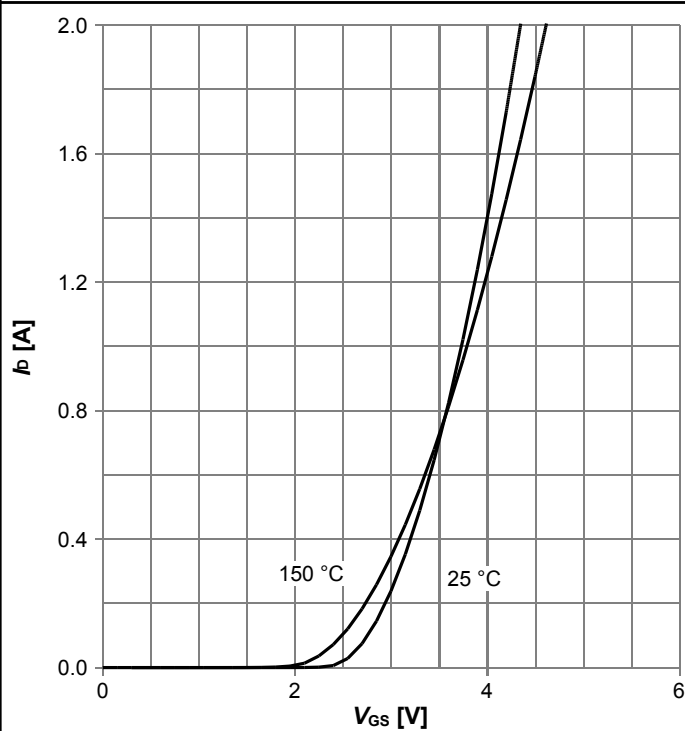
$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on resistance



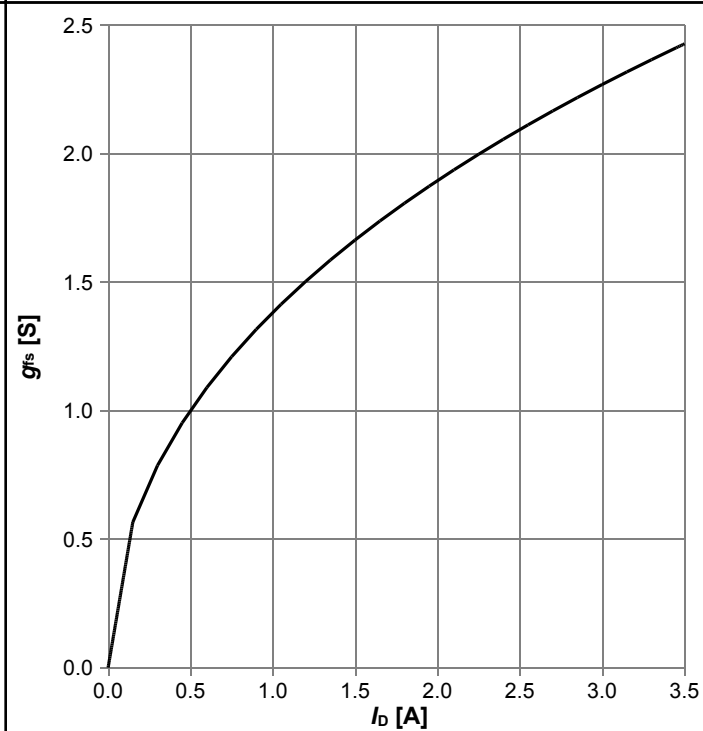
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics



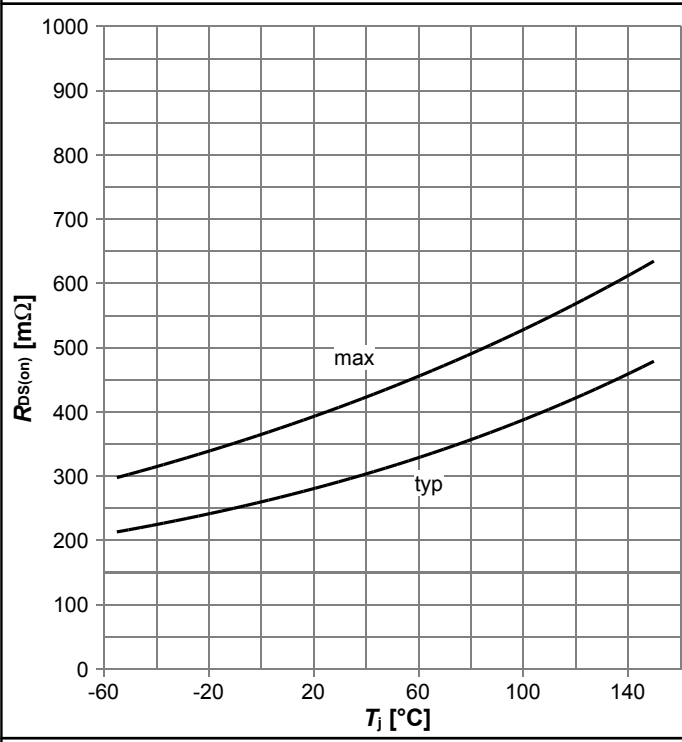
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

Diagram 8: Typ. forward transconductance



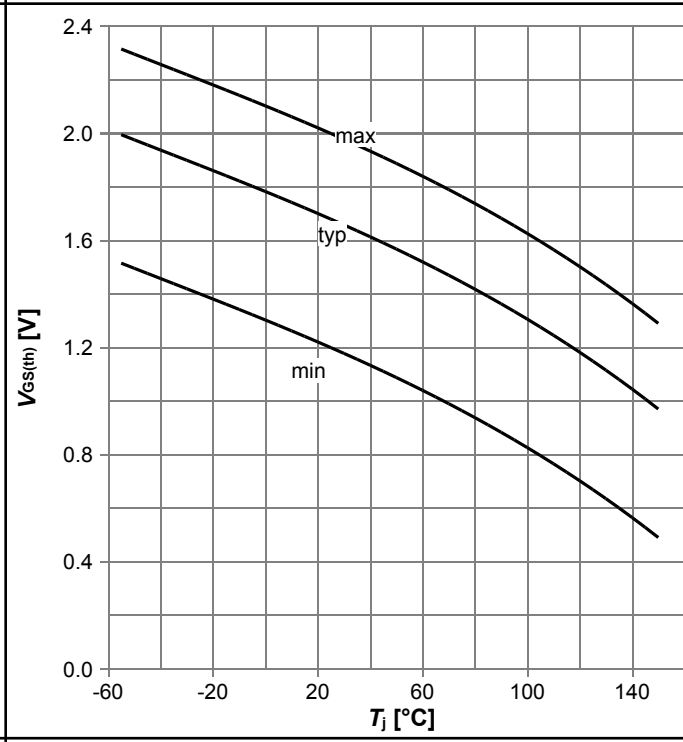
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



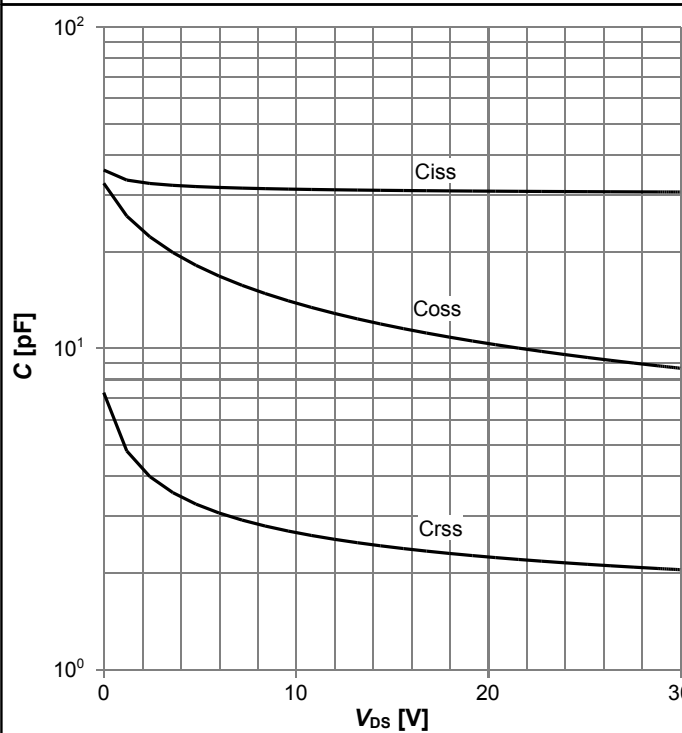
$R_{DS(on)}=f(T_j)$; $I_D=0.88$ A; $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



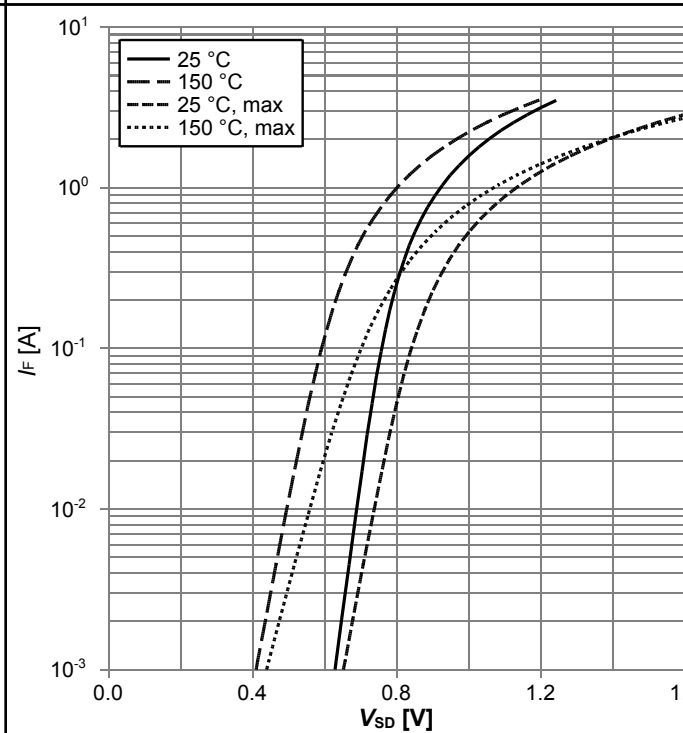
$V_{GS(th)}=f(T_j)$; $V_{DS}=V_{GS}$; $I_D=1.6$ μA; parameter: I_D

Diagram 11: Typ. capacitances



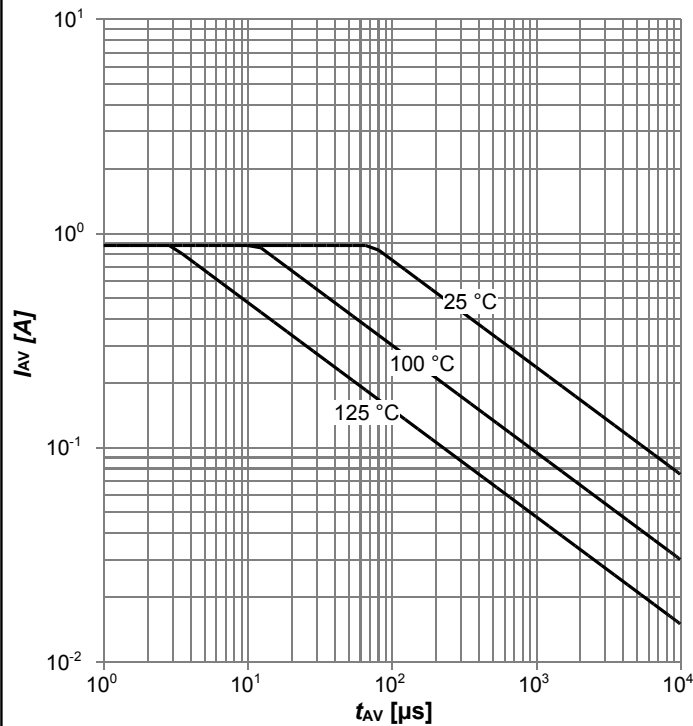
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz; $T_j=25$ °C

Diagram 12: Forward characteristics of reverse diode



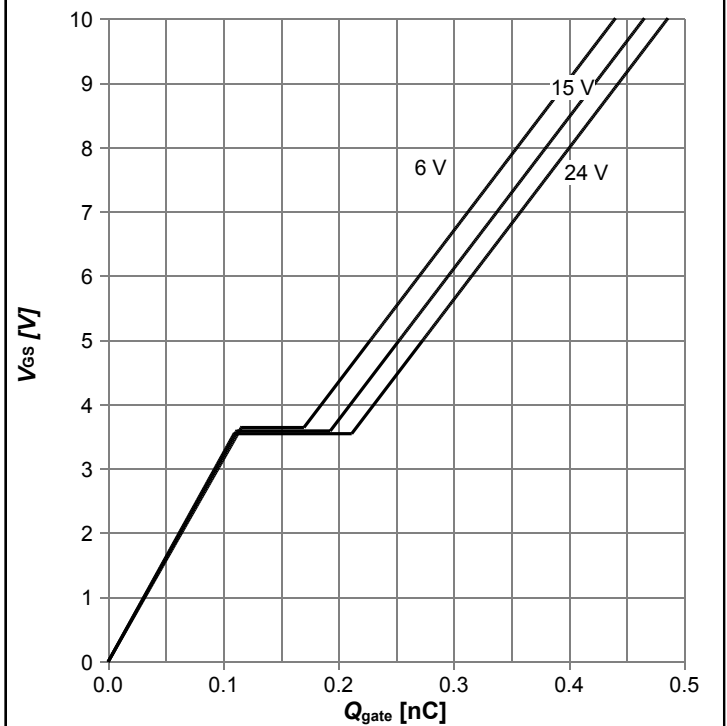
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



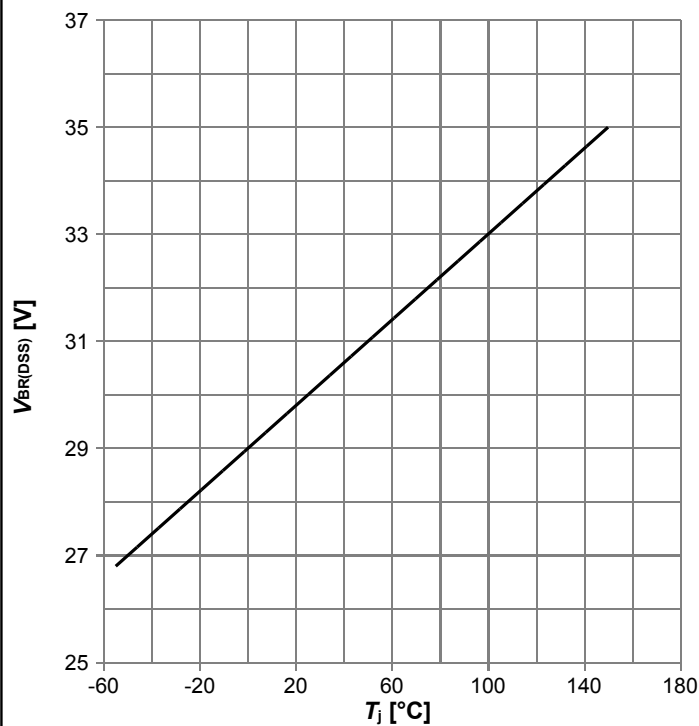
$I_{AS}=f(t_{AV}); R_{GS}=16 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



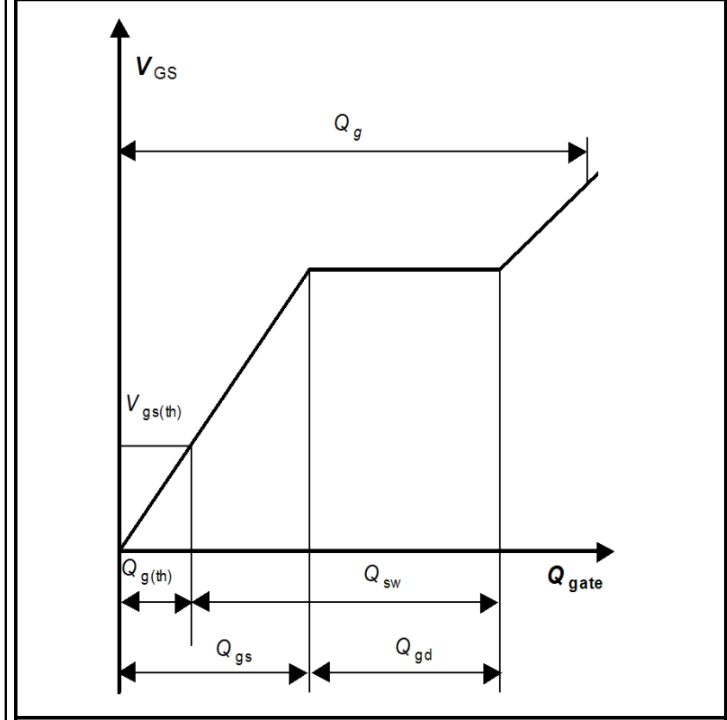
$V_{GS}=f(Q_{gate}); I_D=0.88$ A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



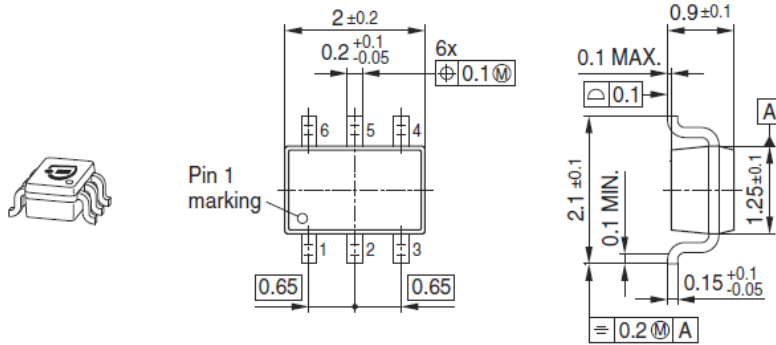
$V_{BR(DSS)}=f(T_j); I_D=250 \mu$ A

Gate charge waveforms



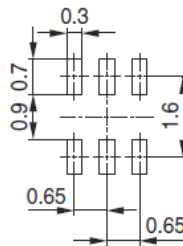
5 Package Outlines

Package Outline

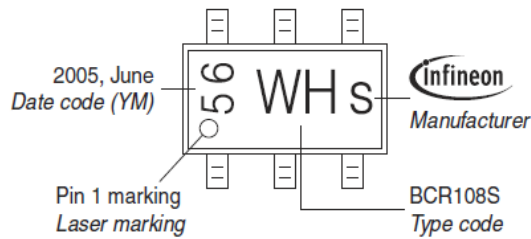


Foot Print

Soldering Type: Reflow Soldering



Marking Layout (Example)



Tape and Reel

Reel $\varnothing 180$ mm: 3.000 Pieces/Reel
 Reels/Box: 1 x 3.000 = 3.000
 Reels/Box: 10 x 3.000 = 30.000

Reel $\varnothing 330$ mm: 10.000 Pieces/Reel
 Reels/Box: 1 x 10.000 = 10.000

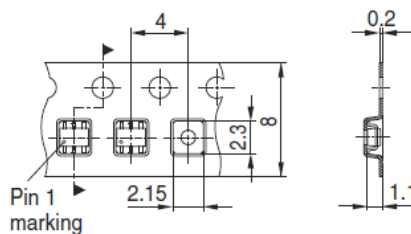


Figure 1 Outline PG-SOT363, dimensions in mm

Revision History

BSD340N

Revision: 2016-06-23, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-06-23	Release of final version

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