

OptiMOS™ - 6 Power-Transistor



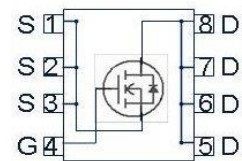
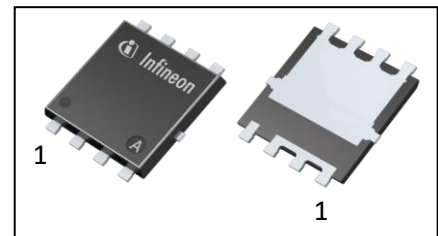
Features

- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal Level
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	0.6	mΩ
I_D	120	A

PG-TDSON-8-53



Type	Package	Marking
IAUC120N04S6N006	PG-TDSON-8-53	6N04N006

Maximum ratings, at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Drain current	I_D	$V_{GS}=10\text{V}$, Chip Limitation ^{1,2)}	405	A
		$V_{GS}=10\text{V}$, DC current ³⁾	120	
		$T_a=85^\circ\text{C}$, $V_{GS}=10\text{V}$, R_{thJA} on 2s2p ^{4,5)}	55	
Pulsed drain current ⁵⁾	$I_{D,pulse}$	$T_C=25^\circ\text{C}$, $t_p=100\mu\text{s}$	1500	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=60\text{A}$, $R_G=25\Omega$	750	mJ
Avalanche current, single pulse	I_{AS}	$R_G=25\Omega$	120	A
Gate source voltage	V_{GS}	-	± 20	V
Power dissipation	P_{tot}	$T_C=25^\circ\text{C}$	187	W
Operating and storage temperature	T_j , T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics⁵⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	0.8	K/W
Thermal resistance, junction - ambient ⁴⁾	R_{thJA}	-	-	26	-	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=130\mu A$	2.2	2.6	3.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{DS}=40V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	-	33	
Gate-source leakage current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=7V, I_D=60A$	-	0.54	0.85	m Ω
		$V_{GS}=10V, I_D=60A$	-	0.46	0.60	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	7607	10117	pF
Output capacitance	C_{oss}		-	2249	2991	
Reverse transfer capacitance	C_{rss}		-	100	150	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=120A, R_G=3.5\Omega$	-	13	-	ns
Rise time	t_r		-	8	-	
Turn-off delay time	$t_{d(off)}$		-	33	-	
Fall time	t_f		-	16	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=32V, I_D=120A,$ $V_{GS}=0 \text{ to } 10V$	-	31	40	nC
Gate to drain charge	Q_{gd}		-	22	32	
Gate charge total	Q_g		-	116	151	
Gate plateau voltage	$V_{plateau}$		-	4.0	-	V

Reverse Diode

Diode continuous forward current ⁵⁾	I_S	$T_C=25^\circ C$	-	-	256	A
Diode pulse current ⁵⁾	$I_{S,pulse}$		-	-	1780	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=60A,$ $T_J=25^\circ C$	-	0.8	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=20V, I_F=50A,$ $di_F/dt=100A/\mu s$	-	66	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	83	-	nC

¹⁾ Practically the current is limited by overall system design including customer specific PCB.

²⁾ The parameter is not subject to production test - verified by characterization.

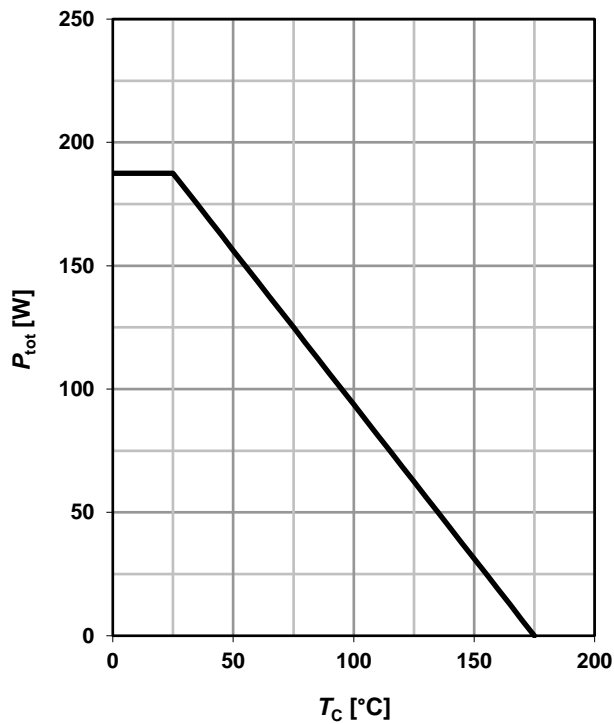
³⁾ The product can operate at specified current based on best practice to minimize electromigration at the solder joint. For rare events and inrush currents the value may be exceeded.

⁴⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

⁵⁾ The parameter is not subject to production test - verified by design.

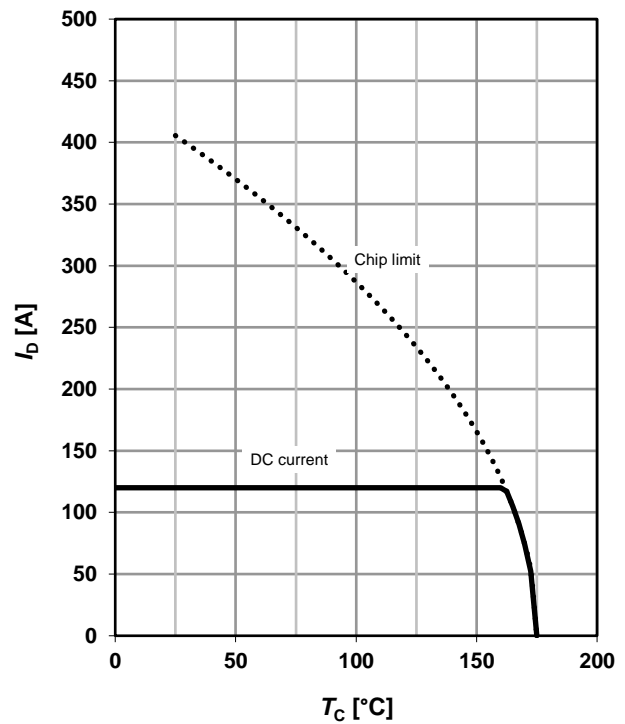
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



2 Drain current

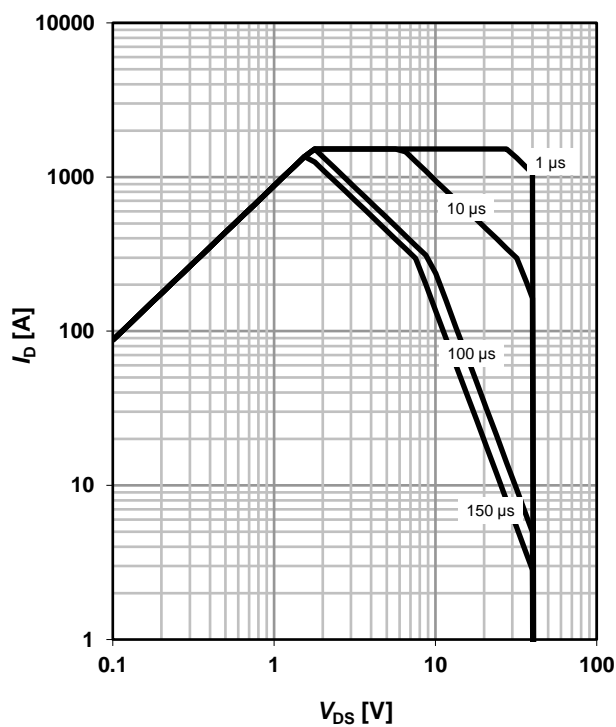
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

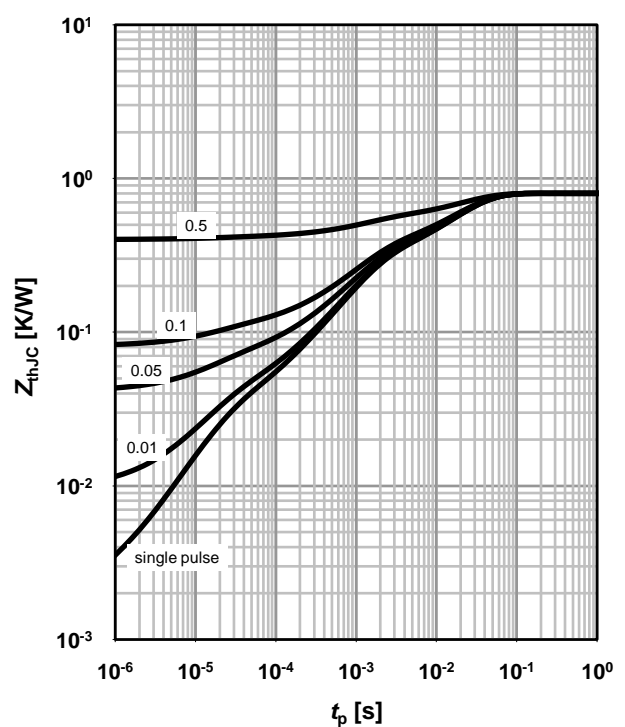
parameter: t_p



4 Max. transient thermal impedance

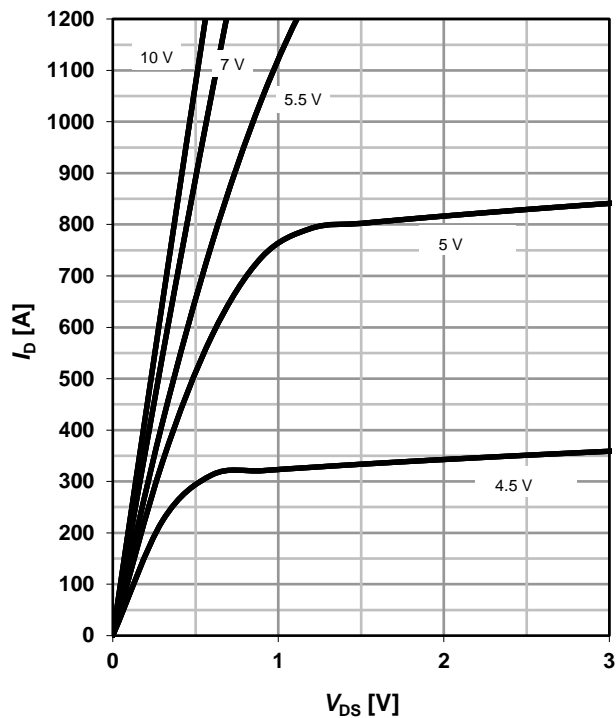
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



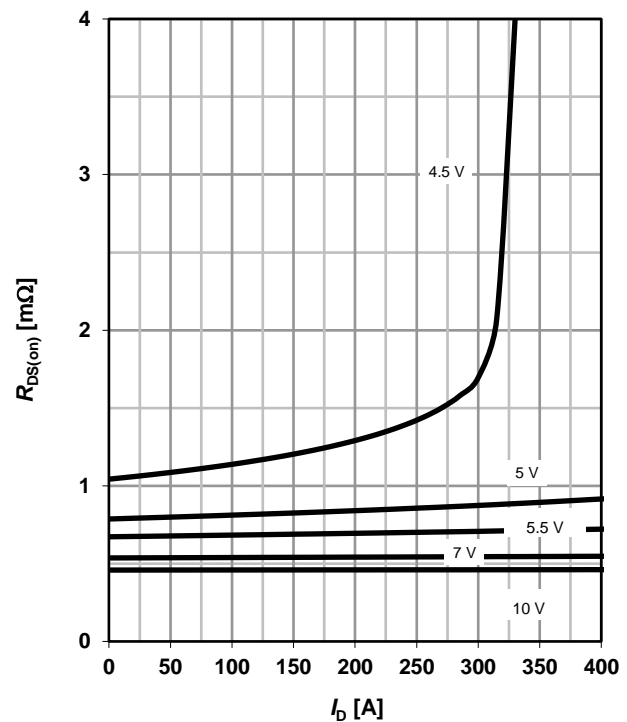
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


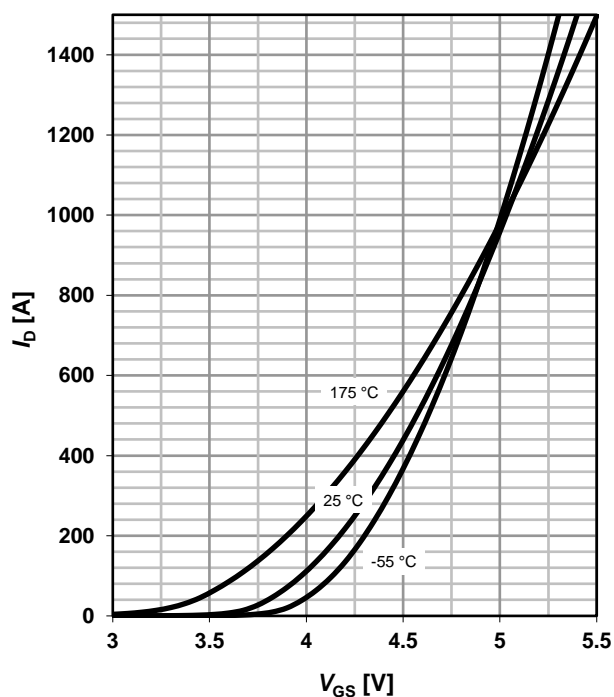
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

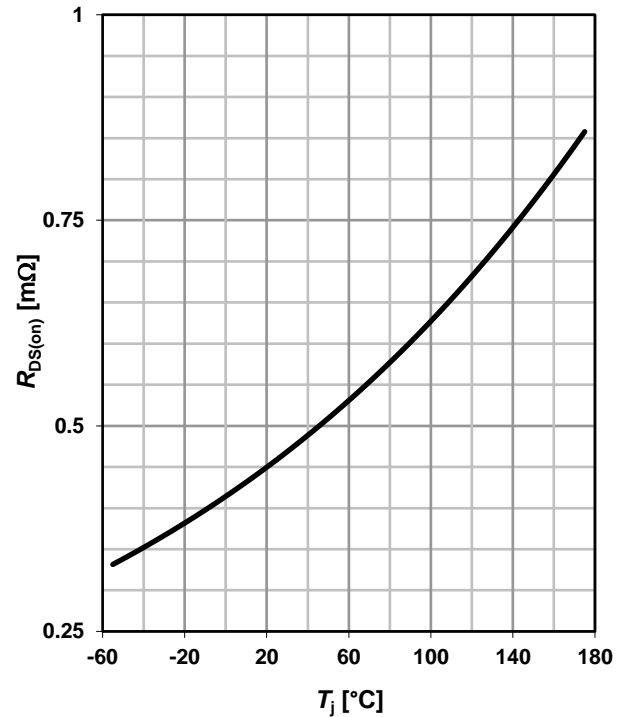
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter: T_j


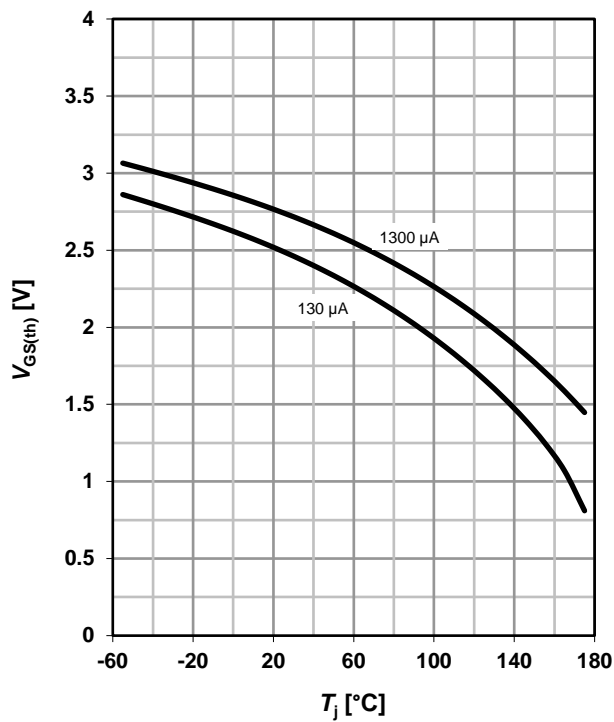
8 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(T_j); I_D = 60\text{ A}; V_{GS} = 10\text{ V}$


9 Typ. gate threshold voltage

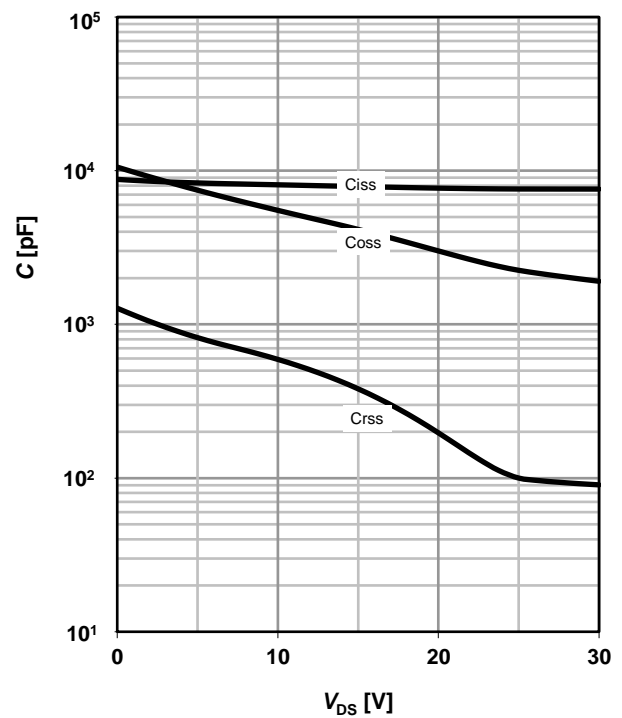
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

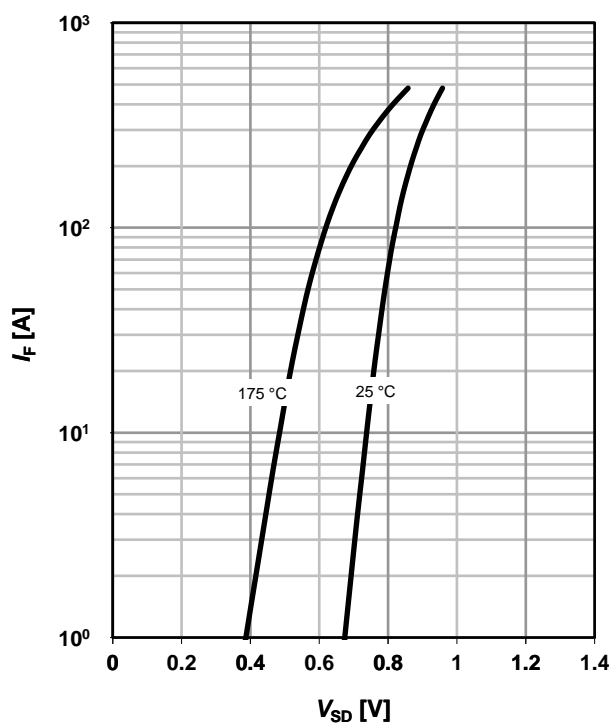
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

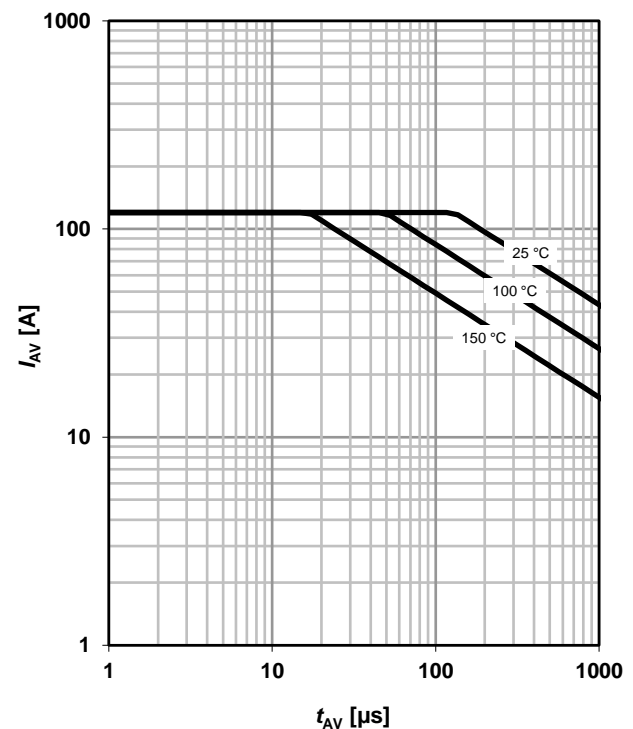
parameter: T_j



12 Avalanche characteristics

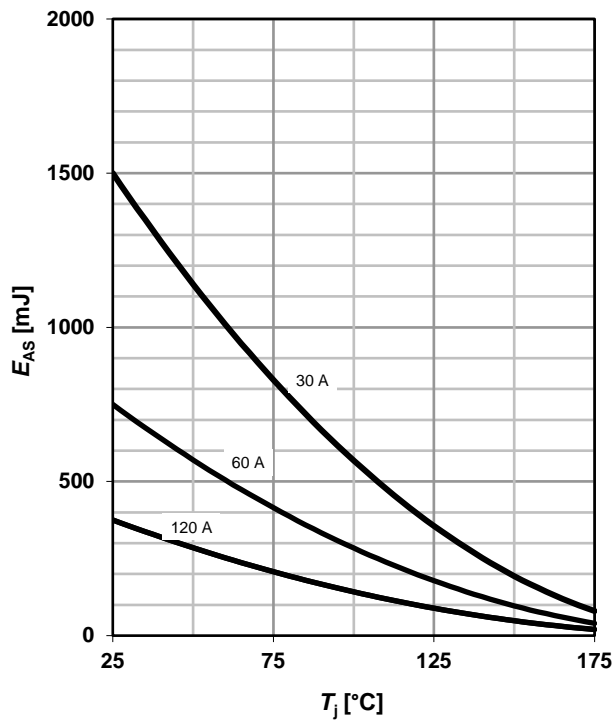
$$I_{AS} = f(t_{AV})$$

parameter: $T_{j(start)} > 25^\circ C$



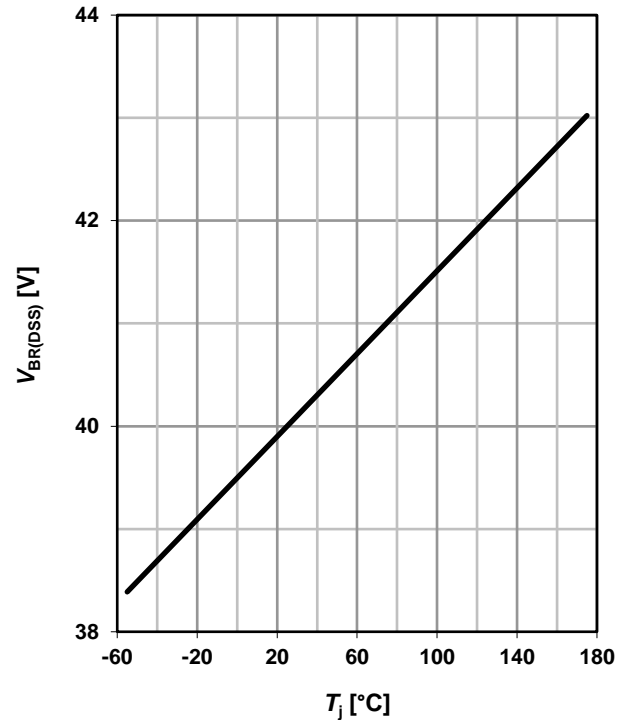
13 Avalanche energy

$$E_{AS} = f(T_j)$$



14 Drain-source breakdown voltage

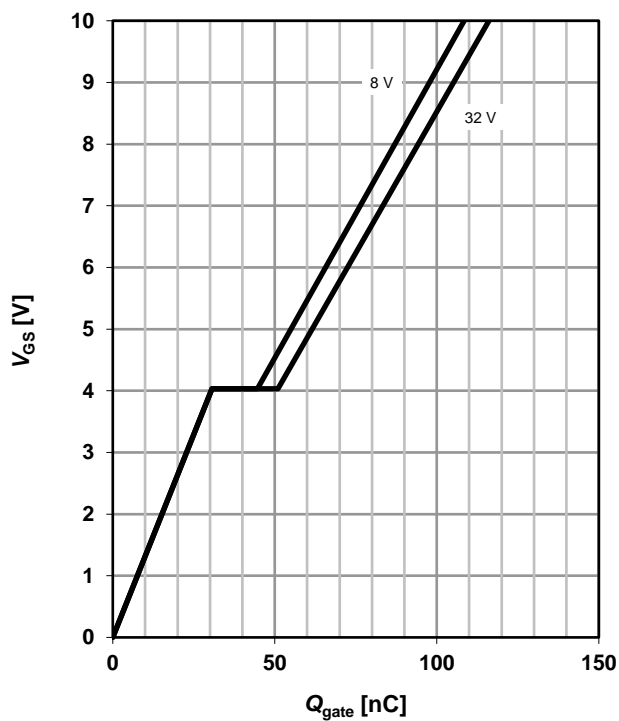
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



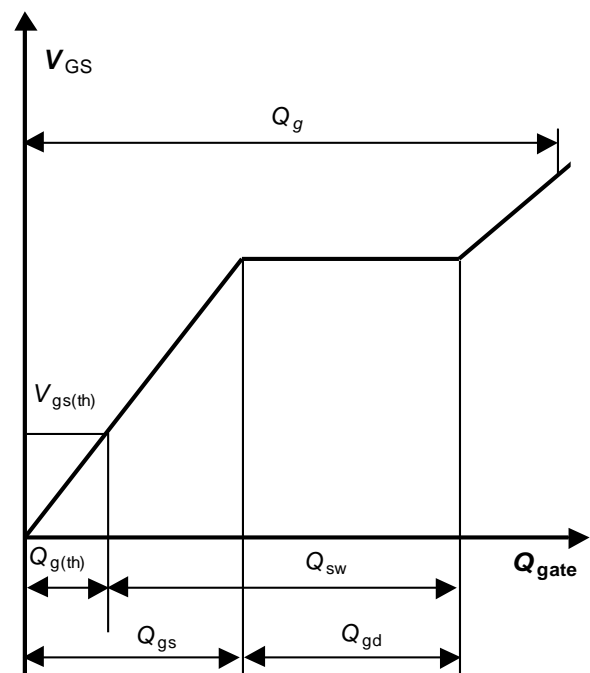
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 120 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



[illegible]

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- Figure 1 shows the dimensions of the PCB layout. The top view (a) includes dimensions for the copper layer, solder mask, and stencil apertures. The bottom view (b) includes dimensions for the solder mask and stencil apertures. The legend indicates: copper (solid grey), solder mask (hatched), and stencil apertures (diagonal lines).

Technical drawing showing the 1000 Series PCB Mounting Dimensions. The drawing includes a top view of the PCB with dimensions: 8 (total width), 4 (pitch), 12 (total length), 0.3 (hole diameter), 1.3 (mounting hole diameter), and 0.3 (mounting hole offset). A label 'PIN 1 INDEX MARKING' points to the first hole.

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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.0	05.06.2020	Final Data Sheet