

# n-Channel Power MOSFET

OptiMOS™  
BSF030NE2LQ

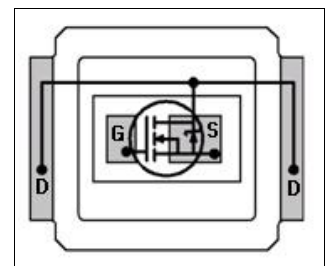
## Data Sheet

2.3, 2011-09-19  
Final

## Industrial & Multimarket

## 1 Description

OptiMOS™25V products are class leading power MOSFETs for highest power density and energy efficient solutions. Ultra low gate and output charges together with lowest on state resistance in small footprint packages make OptiMOS™ 25V the best choice for the demanding requirements of voltage regulator solutions in Servers, Datacom and Telecom applications. Super fast switching Control FETs together with low EMI Sync FETs provide solutions that are easy to design in. OptiMOS™ products are available in high performance packages to tackle your most challenging applications giving full flexibility in optimizing space, efficiency and cost. OptiMOS™ products are designed to meet and exceed the energy efficiency and power density requirements of the sharpened next generation voltage regulation standards in computing applications.



### Features

- Optimized for high performance buck converters
- 100% avalanche tested
- Low parasitic inductance
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Low profile (<0.7 mm)
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Double-sided cooling
- Compatible with DirectFET® package SQ footprint and outline
- 100% Rg Tested

### Applications

- On board power for server
- Power management for high performance computing
- Synchronous rectification
- High power density point of load converters



**Table 1 Key Performance Parameters**

Parameter	Value	Unit	<b>Related Links</b> <a href="#">IFX OptiMOS webpage</a> <a href="#">IFX OptiMOS product brief</a> <a href="#">IFX OptiMOS spice models</a> <a href="#">IFX Design tools</a>
$V_{DS}$	25	V	
$R_{DS(on),max}$	3	m $\Omega$	
$I_D$	75	A	
$Q_{OSS}$	13	nC	
$Q_{g,typ}$	23		

Type	Package	Marking
BSF030NE2LQ	MG-WDSO-2	03E2

1) J-STD20 and JESD22

## 2 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified.

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	75	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$
		-	-	47		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$
		-	-	24		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=45\text{ K/W}^{(1)}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	300		$T_C=25\text{ °C}$
Avalanche current, single pulse <sup>3)</sup>	$I_{AS}$	-	-	40		
Avalanche energy, single pulse	$E_{AS}$	-	-	50	mJ	$I_D=35\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	
Power dissipation	$P_{tot}$	-	-	28	W	$T_C=25\text{ °C}$
		-	-	2.2		$T_A=25\text{ °C}, R_{thJA}=58\text{ K/W}$
Operating and storage temperature	$T_j, T_{stg}$	-40	-	150	°C	
IEC climatic category; DIN IEC 68-1		-				

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

2) See figure 3 for more detailed information

3) See figure 13 for more detailed information

## 3 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	1.0	-	K/W	bottom
		-	-	4.5		top
Device on PCB	$R_{thJA}$	-	-	58		6 cm <sup>2</sup> cooling area <sup>1)</sup>

1) See figure 13 for more detailed information

## 4 Electrical characteristics

Electrical characteristics, at  $T_J=25\text{ °C}$ , unless otherwise specified.

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	25	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1.0\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2		$V_{DS}=V_{GS}$ , $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1	10	$\mu\text{A}$	$V_{DS}=25\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_J=25\text{ °C}$
		-	10	100		$V_{DS}=25\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_J=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	3.3	4.1	m $\Omega$	$V_{GS}=4.5\text{ V}$ , $I_D=30\text{ A}$
		-	2.5	3		$V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$
Gate resistance	$R_G$	-	0.6	-	$\Omega$	
Transconductance	$g_{fs}$	55	110	-	S	$ V_{DS}  > 2 I_D R_{DS(on)max}$ , $I_D=30\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1700	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=12\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	660	-		
Reverse transfer capacitance	$C_{rss}$	-	72	-		
Turn-on delay time	$t_{d(on)}$	-	2.8	-	ns	$V_{DD}=12\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_G=1.6\text{ }\Omega$
Rise time	$t_r$	-	3.4	-		
Turn-off delay time	$t_{d(off)}$	-	18	-		
Fall time	$t_f$	-	2.6	-		

**Table 6 Gate charge characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition	
		Min.	Typ.	Max.			
Gate to source charge	$Q_{gs}$	-	4.4	-	nC	$V_{DD}=12\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$	
Gate charge at threshold	$Q_{g(th)}$	-	2.7	-			
Gate to drain charge	$Q_{gd}$	-	2.7	-			
Switching charge	$Q_{sw}$	-	4.3	-			
Gate charge total	$Q_g$	-	11.3	-			
Gate plateau voltage	$V_{plateau}$	-	2.6	-	V		
Gate charge total	$Q_g$	-	23	-	nC	$V_{DD}=12\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	9.8	-			$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Output charge	$Q_{oss}$	-	13	-			$V_{DD}=12\text{ V}$ , $V_{GS}=0\text{ V}$

1) See figure 16 for gate charge parameter definition

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_s$	-	-	28	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{s,pulse}$	-	-	112		
Diode forward voltage	$V_{SD}$	-	0.86	1	V	$V_{GS}=0\text{ V}$ , $I_F=30\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery charge	$Q_{rr}$	-	10	-	nC	$V_R=15\text{ V}$ , $I_F=I_s$ , $di_F/dt=400\text{ A}/\mu\text{s}$

## 5 Electrical characteristics diagrams

Table 8

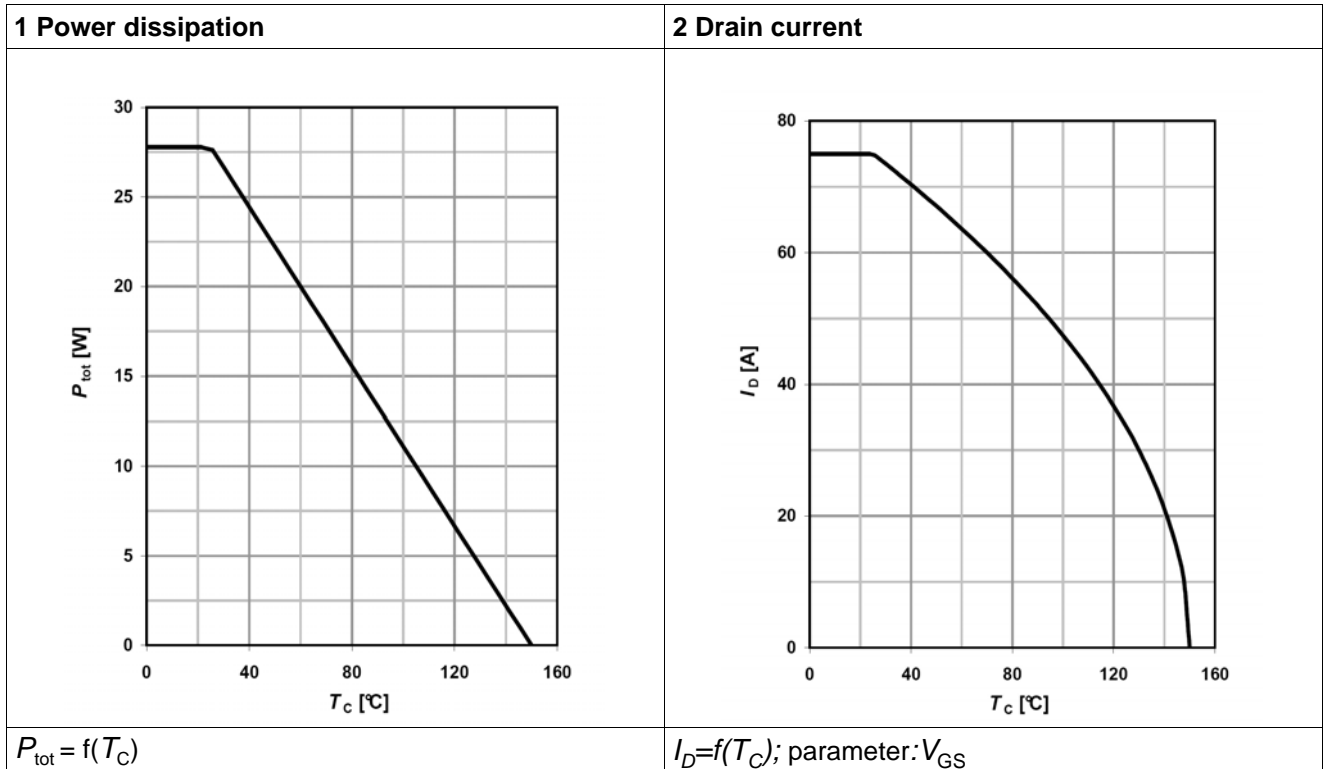


Table 9

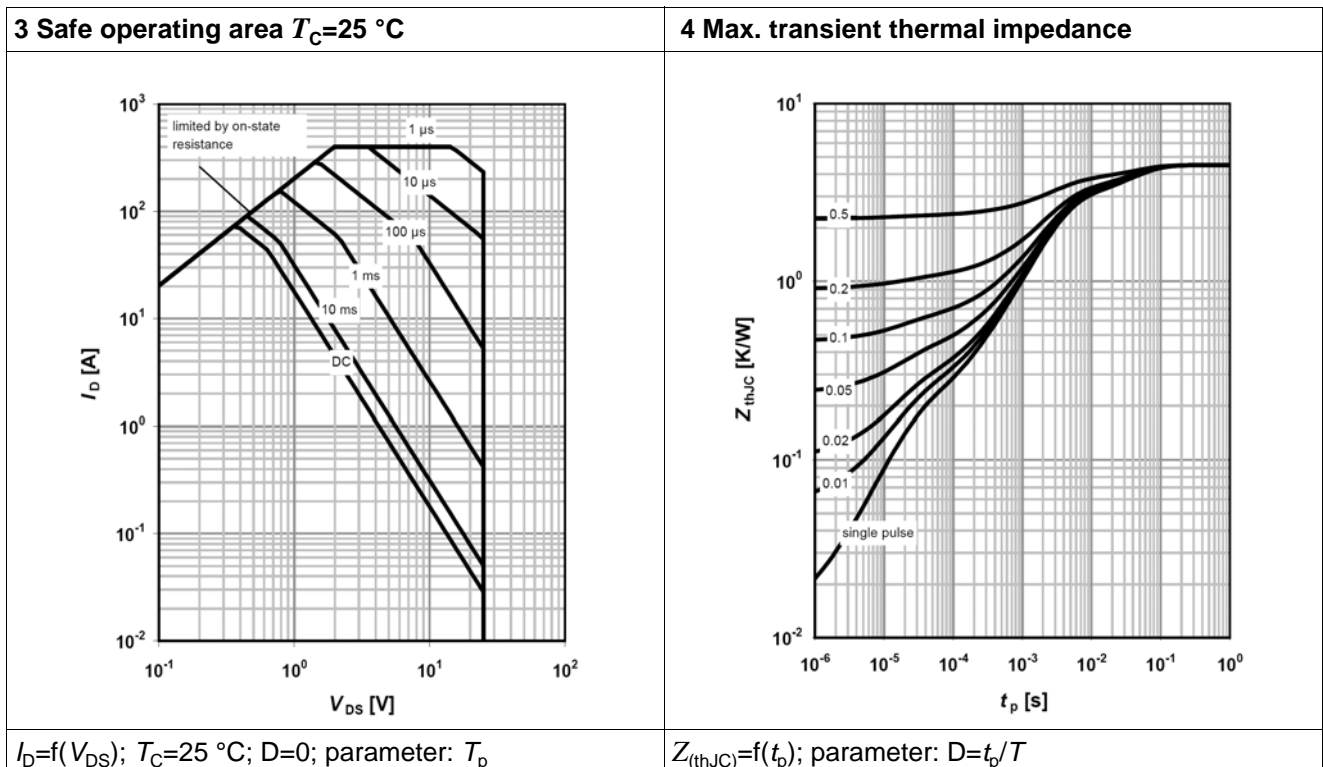


Table 10

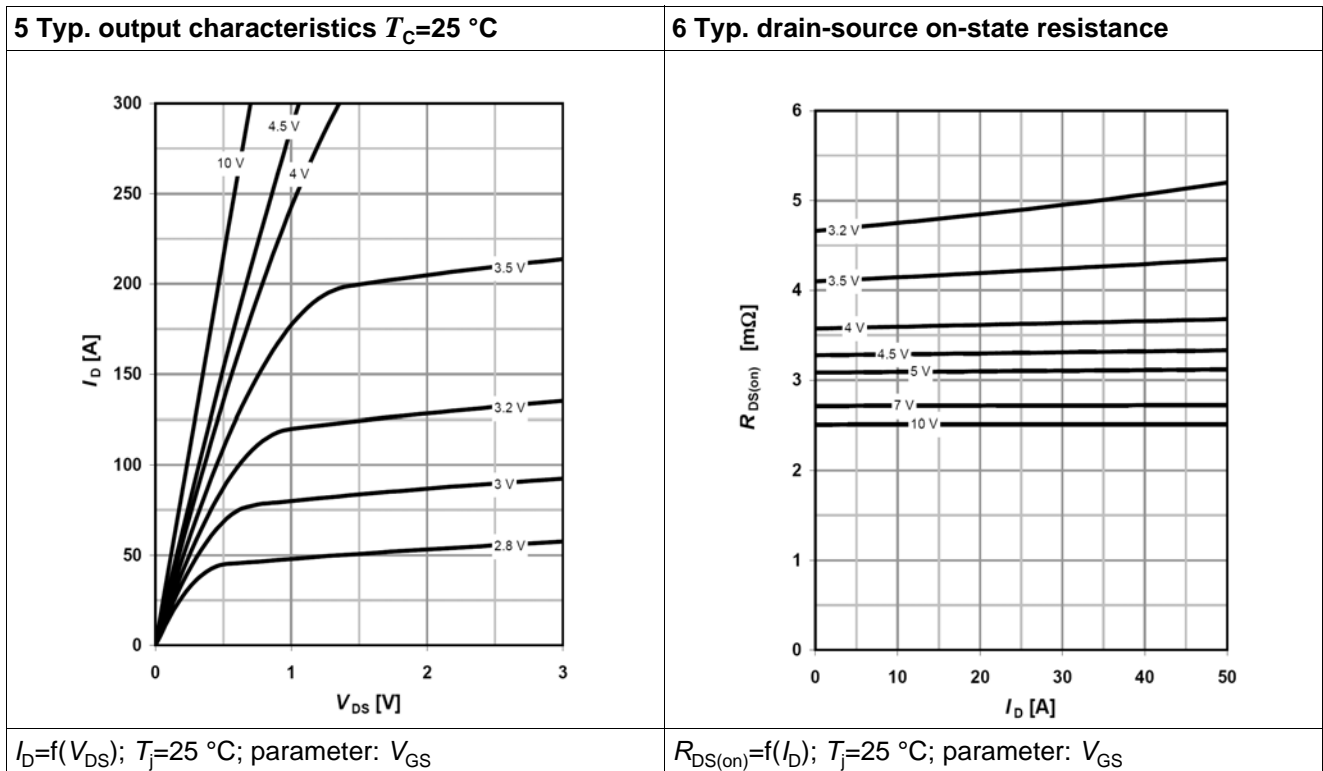


Table 11

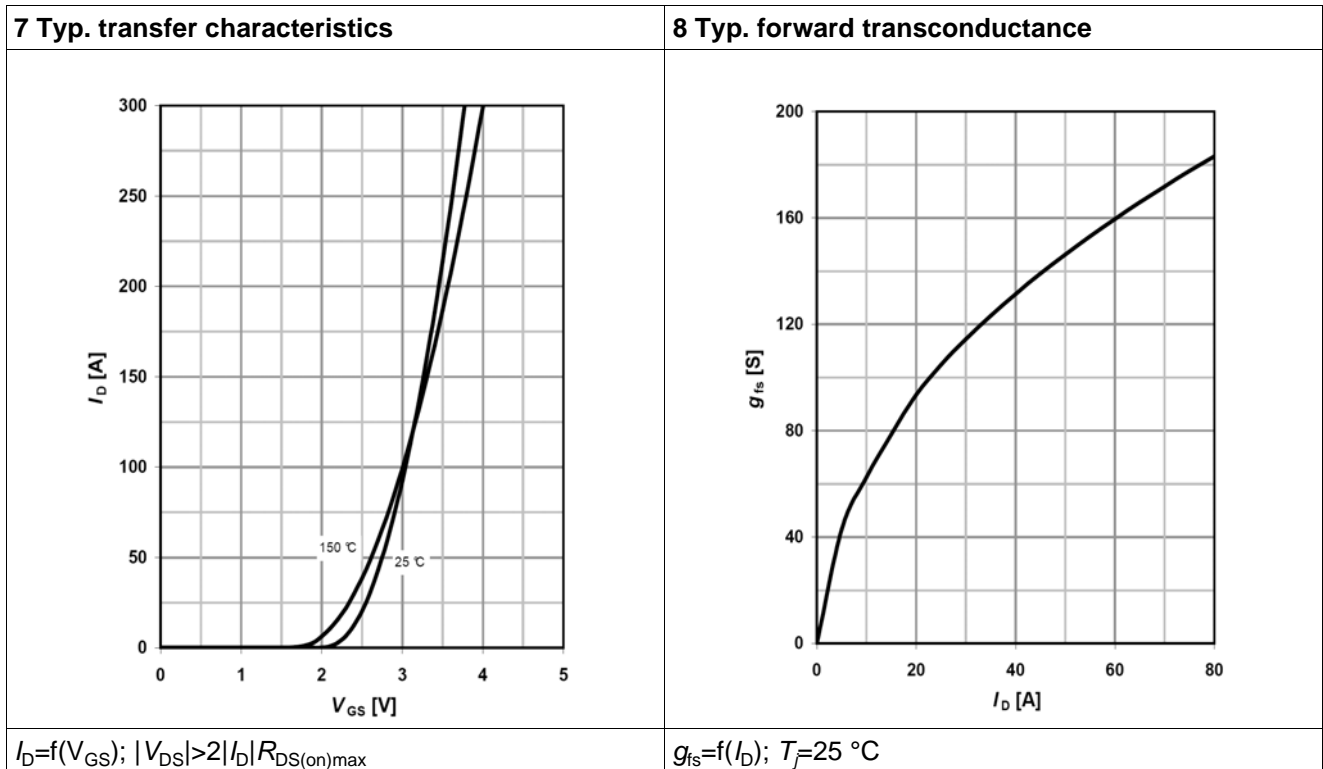


Table 12

<p><b>9 Drain-source on-state resistance</b></p> <p><math>R_{DS(on)} = f(T_j); I_D = 30 \text{ A}; V_{GS} = 10 \text{ V}</math></p>	<p><b>10 Typ. gate threshold voltage</b></p> <p><math>V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 250 \mu\text{A}</math></p>
---	--

Table 13

<p><b>11 Typ. capacitances</b></p> <p><math>C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}</math></p>	<p><b>12 Forward characteristics of reverse diode</b></p> <p><math>I_F = f(V_{SD}); \text{parameter: } T_j</math></p>
---	---



Table 14

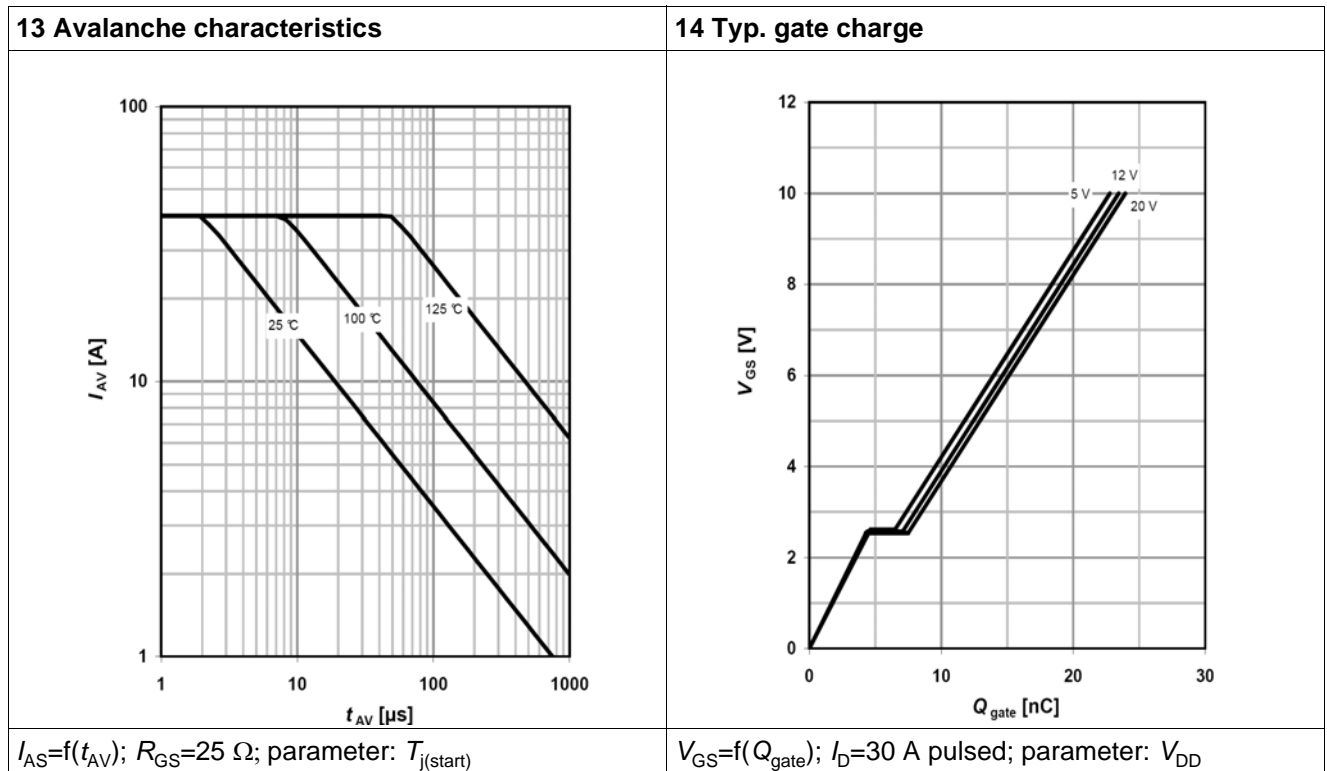
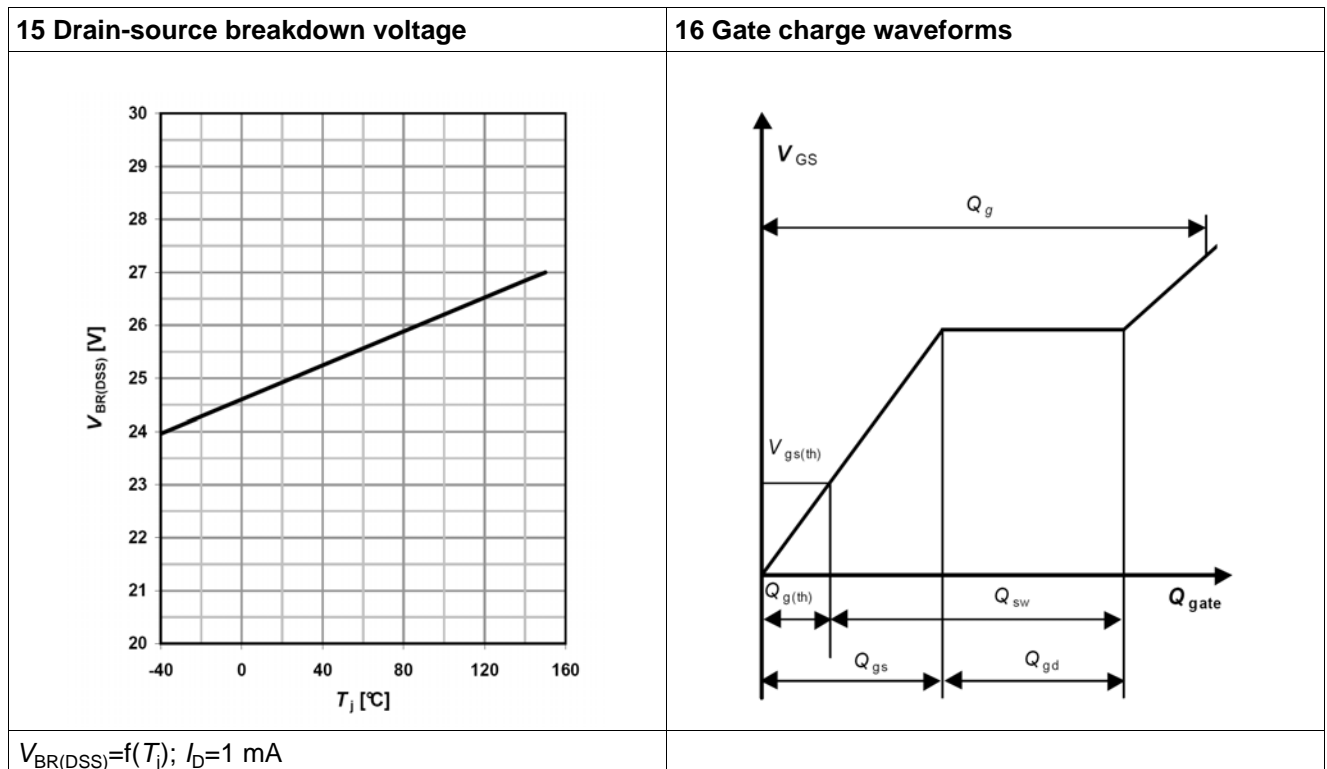
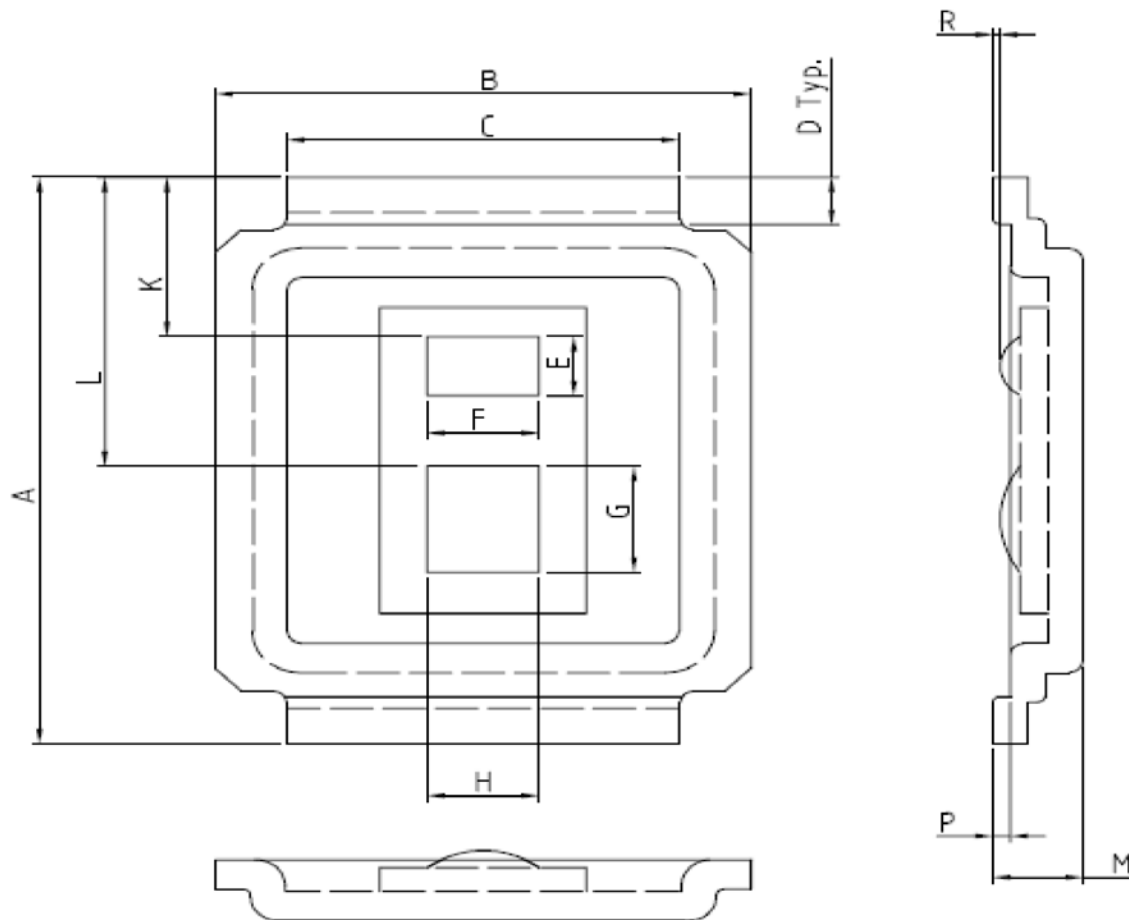


Table 15



## 6 Package outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.75	4.88	0.187	0.192
B	3.70	3.95	0.146	0.156
C	2.75	2.85	0.108	0.112
D	0.35	0.45	0.014	0.018
E	0.48	0.52	0.019	0.020
F	0.78	0.82	0.031	0.032
G	0.88	0.92	0.035	0.036
H	0.78	0.82	0.031	0.032
K	1.25	1.45	0.049	0.057
L	2.35	2.55	0.093	0.100
M	0.60	0.70	0.024	0.028
R	0.00	0.10	0.000	0.004
P	0.08	0.17	0.003	0.007

DOCUMENT NO.  
Z8B00134584

SCALE

7.5mm

EUROPEAN PROJECTION

ISSUE DATE  
05-05-2009

REVISION  
02

Figure 1 Outlines MG-WDSO-2, dimensions in mm/inches

7 Package outlines

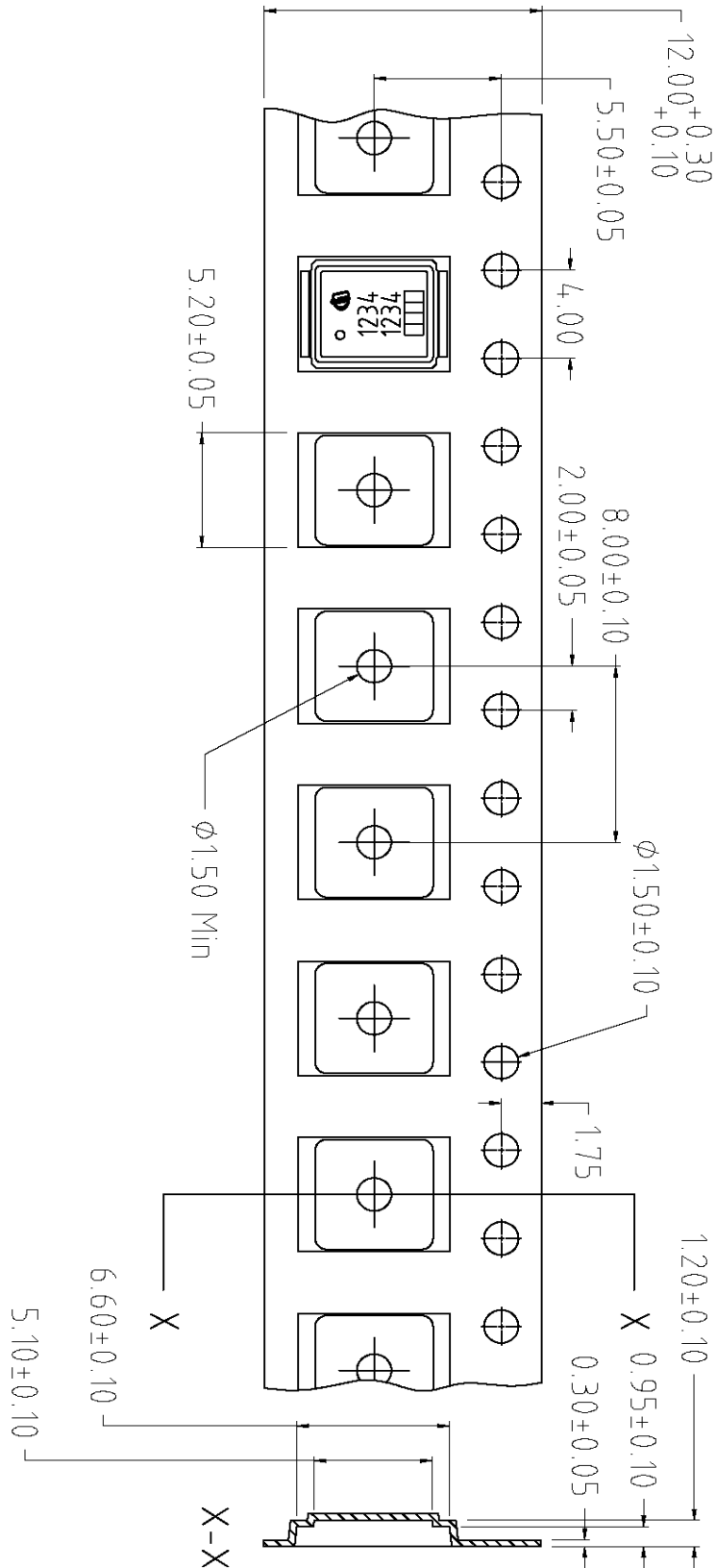


Figure 2 Outlines MG-WDSO-2, dimensions in mm/inches

## 8 Package outlines

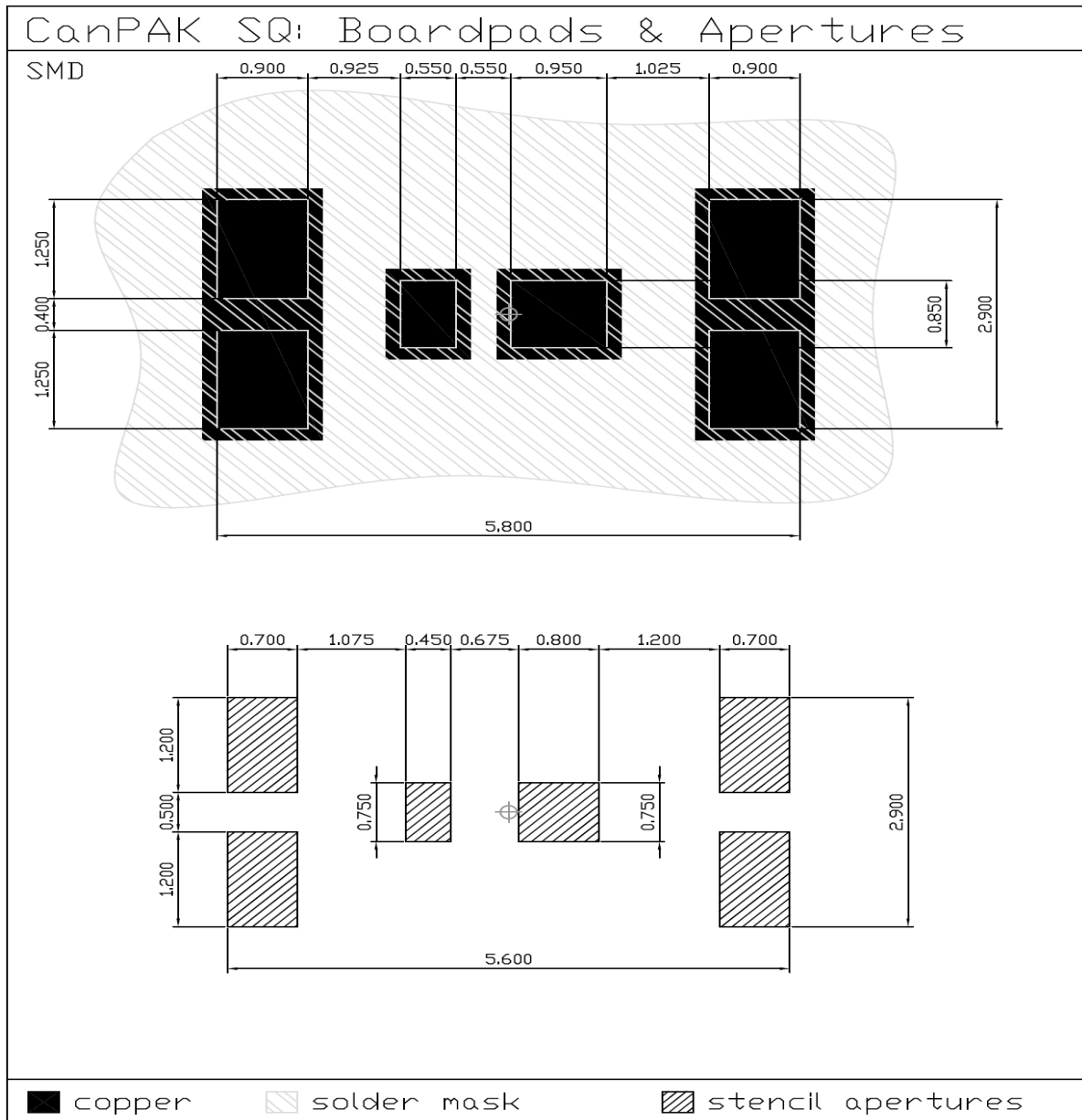
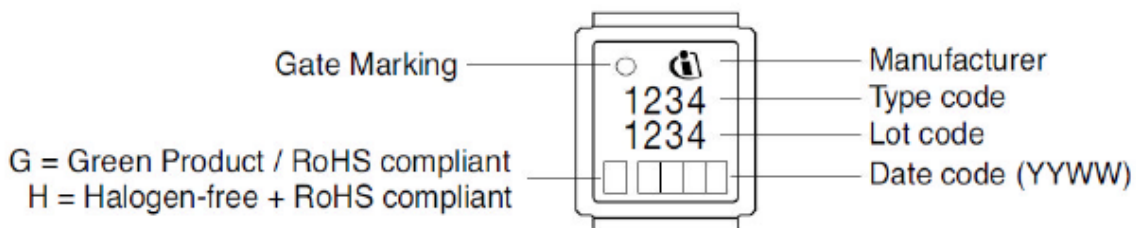


Figure 3 Outlines MG-WDSO-2, dimensions in mm/inches. Recommended stencil thickness 150µm

## 9 Marking Layout



## 9 Revision History

Revision History: 2011-09-19, 2.3

Previous Revision:

Revision	Subjects (major changes since last revision)
0.4	Release of target data sheet
2.0	Release Final version
2.2	DirectFET Disclaimer expired
2.3	Update VGStH

### We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all?

Your feedback will help us to continuously improve the quality of this document.

Please send your proposal (including a reference to this document) to: [erratum@infineon.com](mailto:erratum@infineon.com)



Edition 2011-09-19

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2011 Infineon Technologies AG

All Rights Reserved.

### Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

### Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

### Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.