

IR2110L4

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +400V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V
Logic and power ground $\pm 5V$ offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

V_{OFFSET}	400V max.
I_{O+/-}	2A / 2A
V_{OUT}	10 - 20V
ton/off (typ.)	120ns & 94ns
Delay Matching	10ns

Description

The IR2110L4 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers features a

high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 400 volts.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min.	Max.	Units
V _B	High Side Floating Supply Voltage	-0.5	V _S + 20	V
V _S	High Side Floating Supply Offset Voltage	—	400	
V _{HO}	High Side Floating Output Voltage	V _S - 0.5	V _B + 0.5	
V _{CC}	Low Side Fixed Supply Voltage	-0.5	20	
V _{LO}	Low Side Output Voltage	-0.5	V _{CC} + 0.5	
V _{DD}	Logic Supply Voltage	-0.5	V _{SS} + 20	
V _{SS}	Logic Supply Offset Voltage	V _{CC} - 20	V _{CC} + 0.5	
V _{IN}	Logic Input Voltage (HIN, LIN & SD)	V _{SS} - 0.5	V _{DD} + 0.5	
dV _S /dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50	V/ns
P _D	Package Power Dissipation @ T _A \leq +25°C	—	1.6	W
R _{thJA}	Thermal Resistance, Junction to Ambient	—	75	°C/W
T _J	Junction Temperature	-55	125	°C
T _S	Storage Temperature	-55	150	
T _L	Lead Temperature (Soldering, 10 seconds)	—	300	
	Weight	1.5 (typical)		g

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figures 36 and 37.

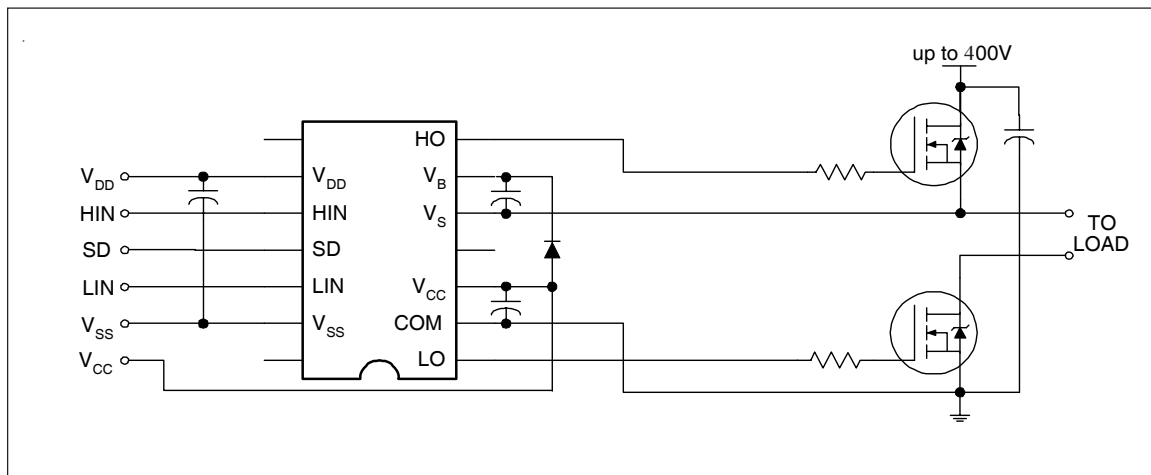
Symbol	Parameter	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	$V_S + 10$	$V_S + 20$	V
V_S	High Side Floating Supply Offset Voltage	-4	400	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Low Side Fixed Supply Voltage	10	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{DD}	Logic Supply Voltage	$V_{SS} + 5$	$V_{SS} + 20$	
V_{SS}	Logic Supply Offset Voltage	-5	5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_B , V_{DD}) = 15V, and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

Symbol	Parameter	$T_j = 25^\circ\text{C}$			$T_j = -55 \text{ to } 125^\circ\text{C}$		Units	Test Conditions
		Min.	Typ.	Max.	Min.	Max.		
t_{on}	Turn-On Propagation Delay	—	120	150	—	260	ns	$V_S = 0\text{V}$
t_{off}	Turn-Off Propagation Delay	—	94	125	—	220		$V_S = 400\text{V}$
t_{sd}	Shutdown Propagation Delay	—	110	140	—	235		$V_S = 400\text{V}$
t_r	Turn-On Rise Time	—	25	35	—	50		$C_L = 1000\text{pf}$
t_f	Turn-Off Fall Time	—	17	25	—	40		$C_L = 1000\text{pf}$
MT	Delay Matching, HS & LS Turn-On/Off	—	—	20	—	—		$ t_{on} - t_{on} / t_{off} - t_{off} $

Typical Connection



Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	T _j = 25°C			T _j = -55 to 125°C		Units	Test Conditions
		Min	Typ.	Max.	Min.	Max.		
V _{IH}	Logic "1" Input Voltage	9.5	—	—	10	—	V	V _{DD} = 15V
V _{IL}	Logic "0" Input Voltage	—	—	6.0	—	5.7		V _{DD} = 15V
V _{OH}	High Level Output Voltage, V _{BIAS} - V _O	—	0.7	1.2	—	1.5		V _{IN} = V _{IH} , I _O = 0A
V _{OL}	Low Level Output Voltage, V _O	—	—	0.1	—	0.1		V _{IN} = V _{IL} , I _O = 0A
I _{LK}	Offset Supply Leakage Current	—	—	50	—	250	μA	V _B = V _S = 400V
I _{QBS}	Quiescent V _{BS} Supply Current	—	125	230	—	500		V _{IN} = V _{IH} or V _{IL}
I _{QCC}	Quiescent V _{CC} Supply Current	—	180	340	—	600		V _{IN} = V _{IH} or V _{IL}
I _{QDD}	Quiescent V _{DD} Supply Current	—	5	30	—	60		V _{IN} = V _{IH} or V _{IL}
I _{IN+}	Logic "1" Input Bias Current	—	15	40	—	70		V _{IN} = 15V
I _{IN-}	Logic "0" Input Bias Current	—	—	1.0	—	10		V _{IN} = 0V
V _{BSUV+}	V _{BS} Supply Undervoltage Positive Going Threshold	7.5	8.6	9.7	—	—	V	
V _{BSUV-}	V _{BS} Supply Undervoltage Negative Going Threshold	7.0	8.2	9.4	—	—		
V _{CCUV+}	V _{CC} Supply Undervoltage Positive Going Threshold	7.4	8.5	9.6	—	—		
V _{CCUV-}	V _{CC} Supply Undervoltage Negative Going Threshold	7.0	8.2	9.4	—	—		
I _{O+}	Output High Short Circuit Pulsed Current	2.0	—	—	—	—	A	V _O = 0V, V _{IN} = V _{DD} PW ≤ 10μs
I _{O-}	Output Low Short Circuit Pulsed Current	2.0	—	—	—	—		V _O = 15V, V _{IN} = 0V PW ≤ 10μs

IR2110L4

International
IR Rectifier

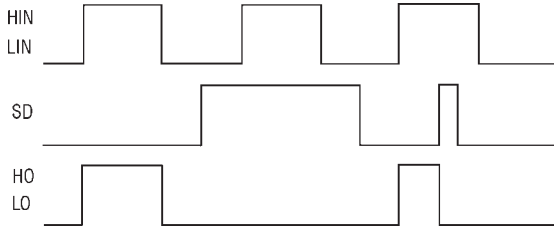


Figure 1. Input/Output Timing Diagram

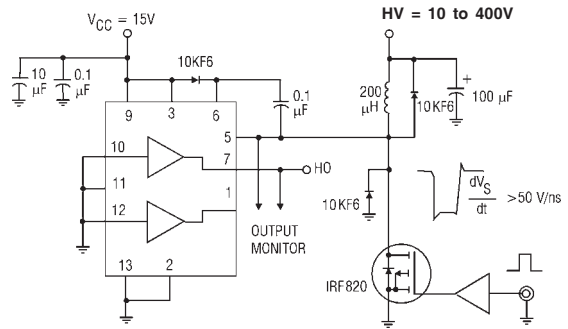


Figure 2. Floating Supply Voltage Transient Test Circuit

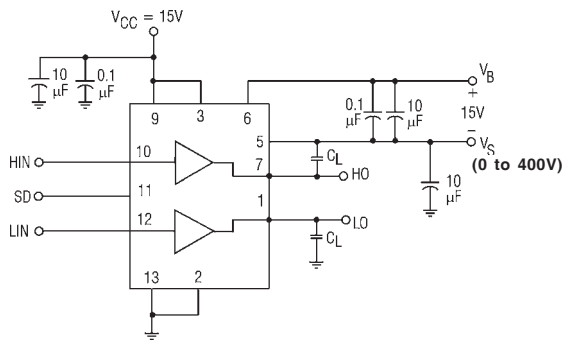


Figure 3. Switching Time Test Circuit

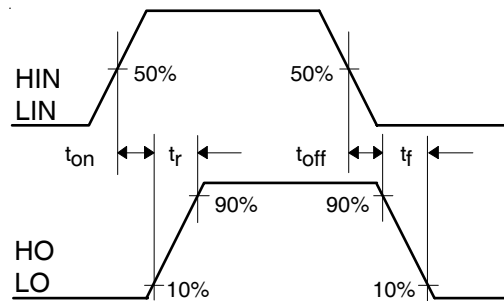


Figure 4. Switching Time Waveform Definition

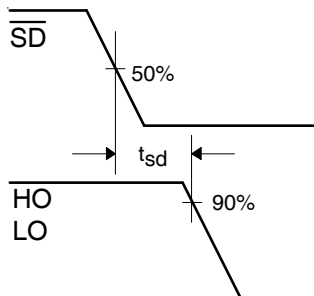


Figure 5. Shutdown Waveform Definitions

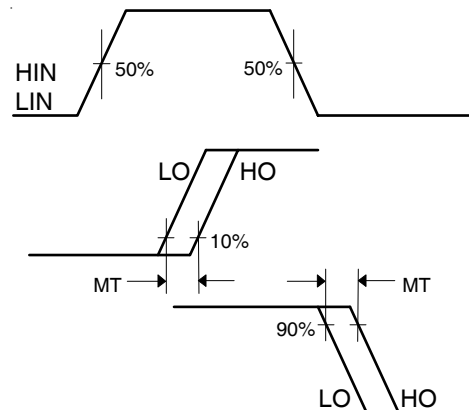


Figure 6. Delay Matching Waveform Definitions

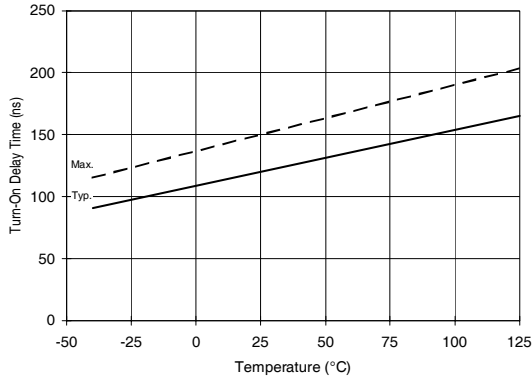


Figure 7A. Turn-On Time vs. Temperature

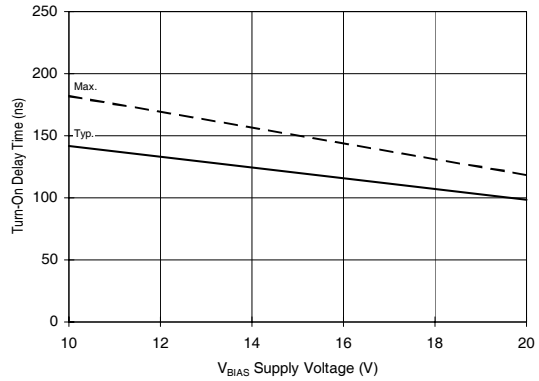


Figure 7B. Turn-On Time vs. Voltage

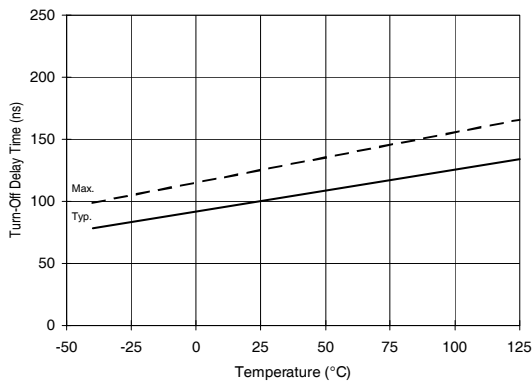


Figure 8A. Turn-Off Time vs. Temperature

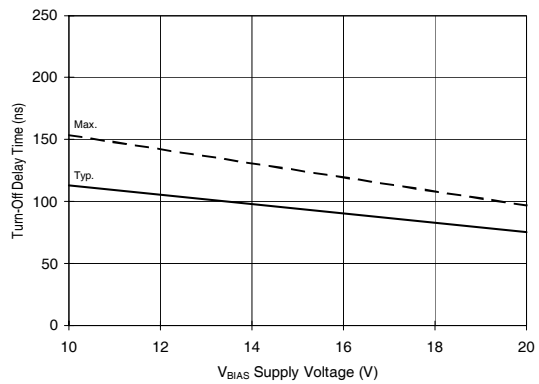


Figure 8B. Turn-Off Time vs. Voltage

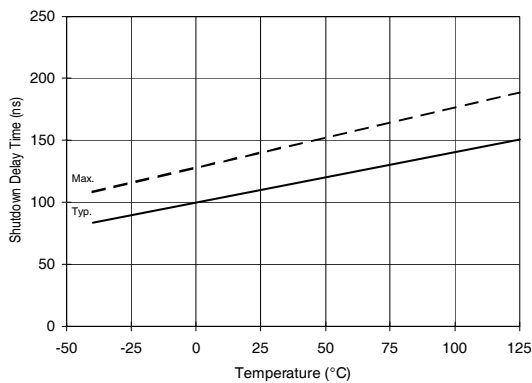


Figure 9A. Shutdown Time vs. Temperature

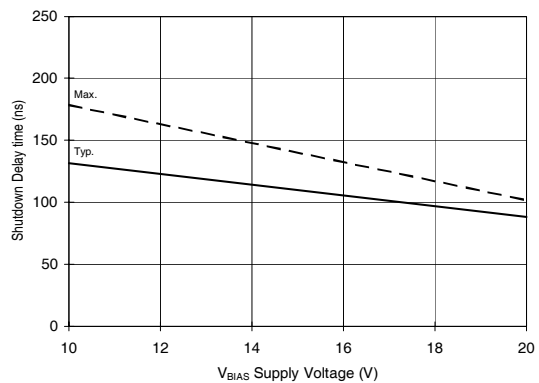


Figure 9B. Shutdown Time vs. Voltage

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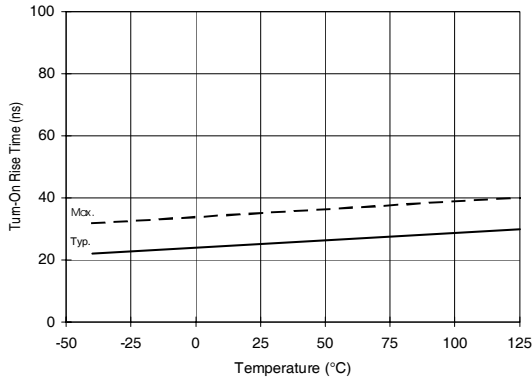


Figure 10A. Turn-On Rise Time vs. Temperature

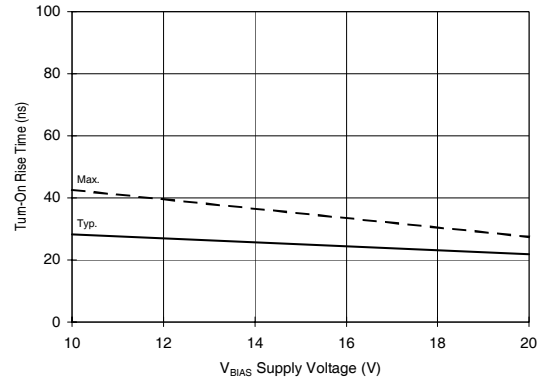


Figure 10B. Turn-On Rise Time vs. Voltage

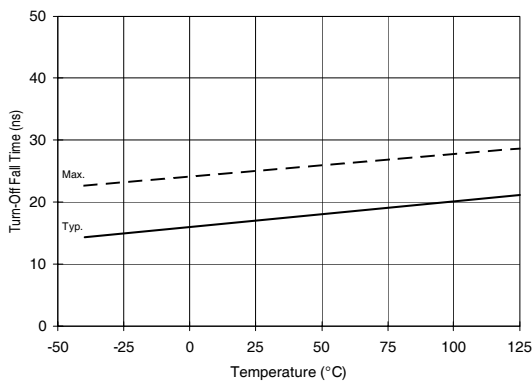


Figure 11A. Turn-Off Fall Time vs. Temperature

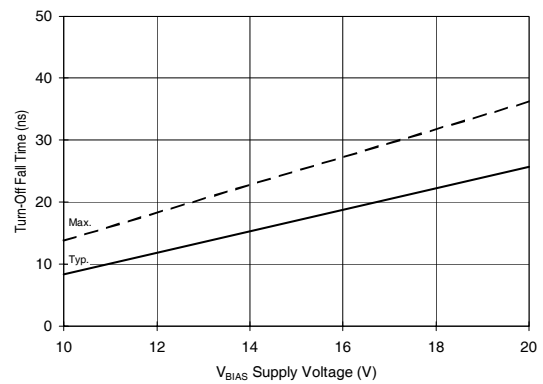


Figure 11B. Turn-Off Fall Time vs. Voltage

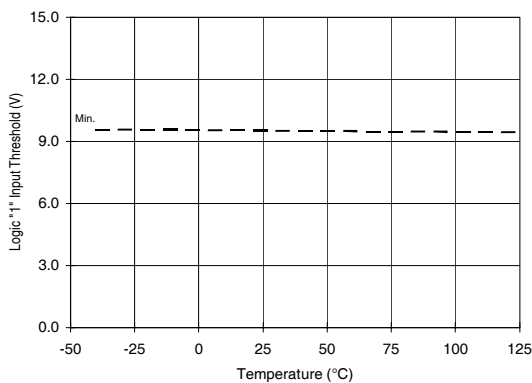


Figure 12A. Logic "1" Input Threshold vs. Temperature

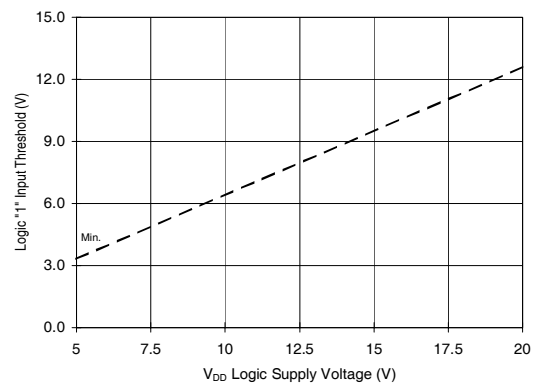


Figure 12B. Logic "1" Input Threshold vs. Voltage

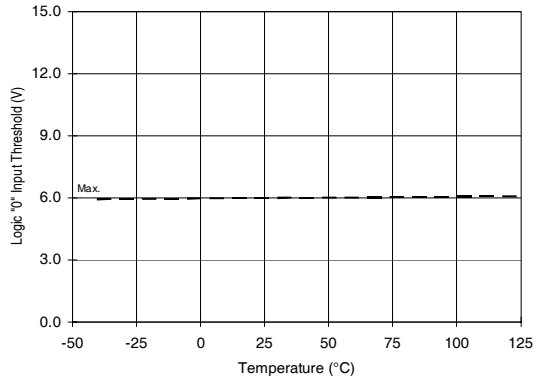


Figure 13A. Logic "0" Input Threshold vs. Temperature

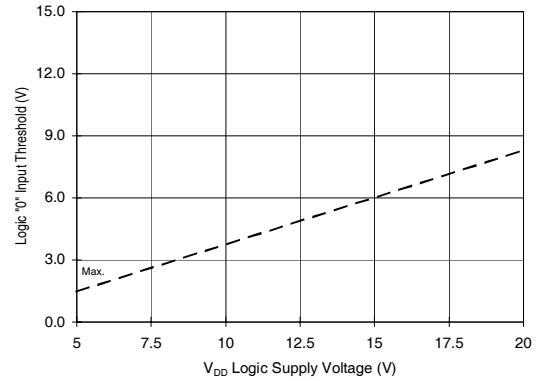


Figure 13B. Logic "0" Input Threshold vs. Voltage

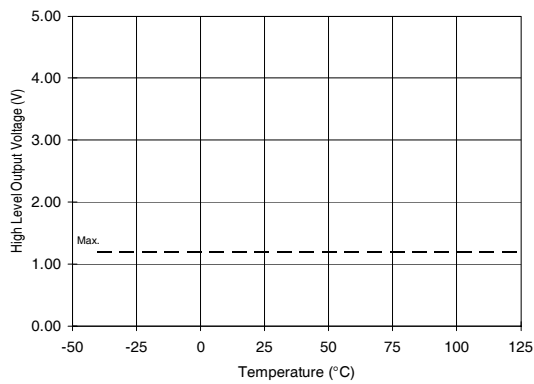


Figure 14A. High Level Output vs. Temperature

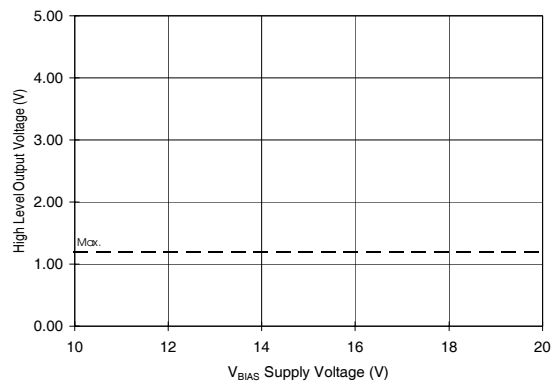


Figure 14B. High Level Output vs. Voltage

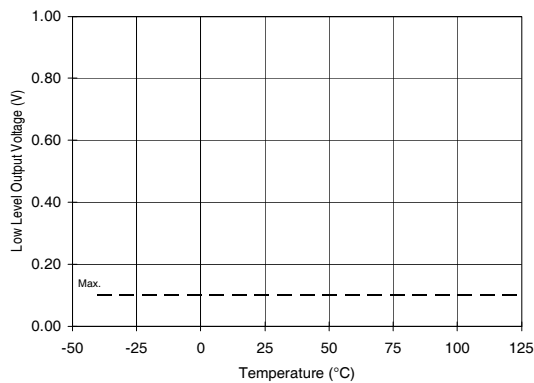


Figure 15A. Low Level Output vs. Temperature

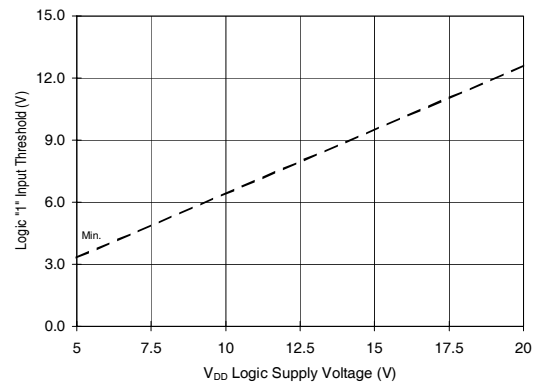


Figure 15B. Low Level Output vs. Voltage

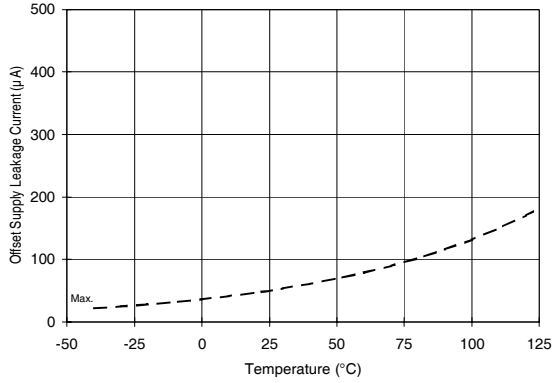


Figure 16A. Offset Supply Current vs. Temperature

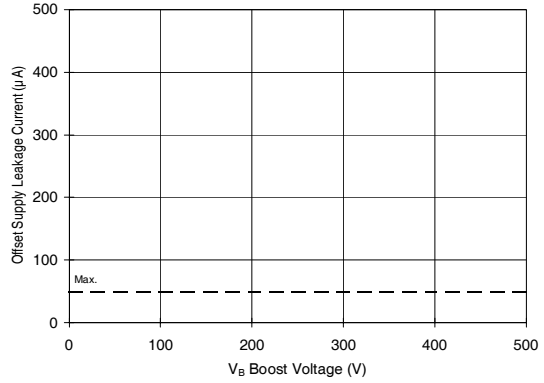


Figure 16B. Offset Supply Current vs. Voltage

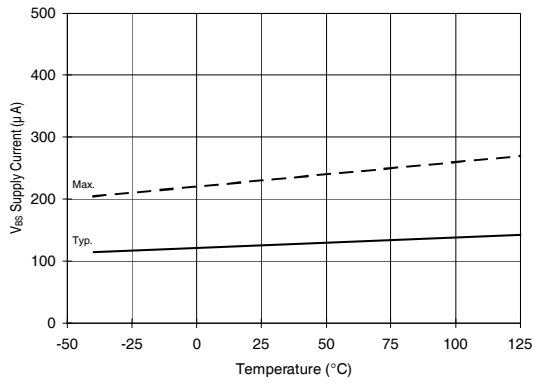


Figure 17A. V_{BS} Supply Current vs. Temperature

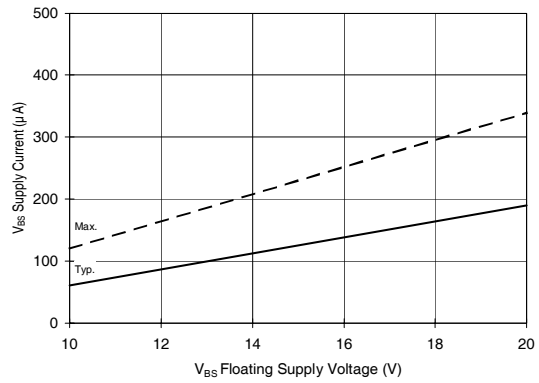


Figure 17B. V_{BS} Supply Current vs. Voltage

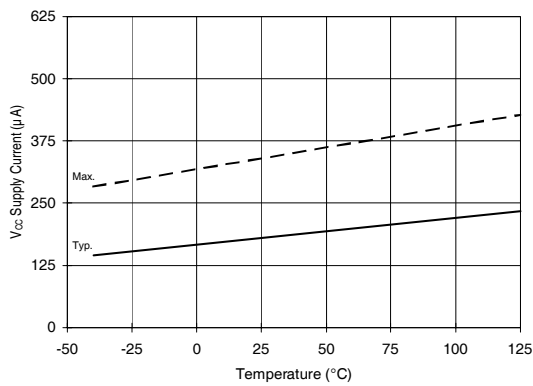


Figure 18A. V_{CC} Supply Current vs. Temperature

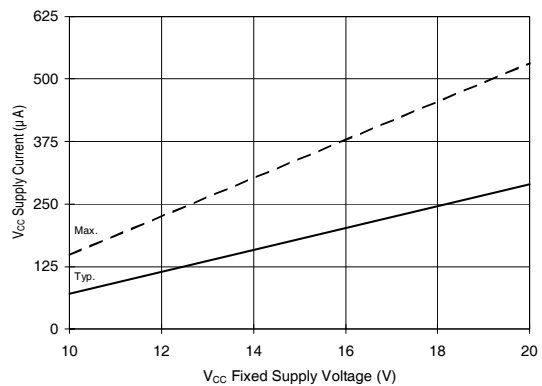


Figure 18B. V_{CC} Supply Current vs. Voltage

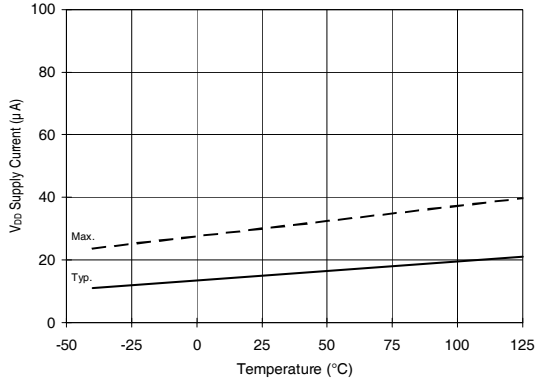


Figure 19A. V_{DD} Supply Current vs. Temperature

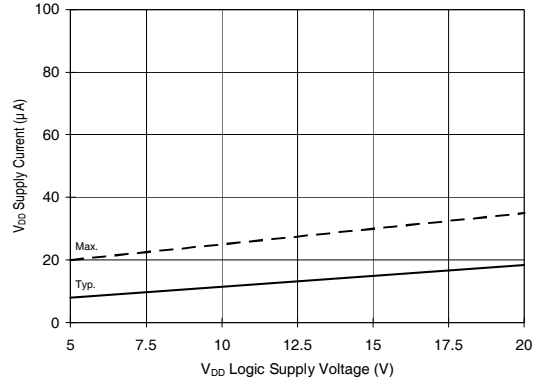


Figure 19B. V_{DD} Supply Current vs. Voltage

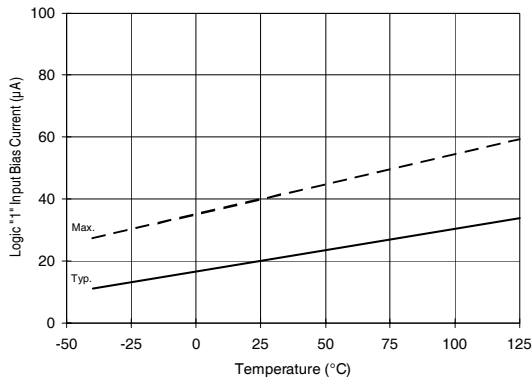


Figure 20A. Logic "1" Input Current vs. Temperature

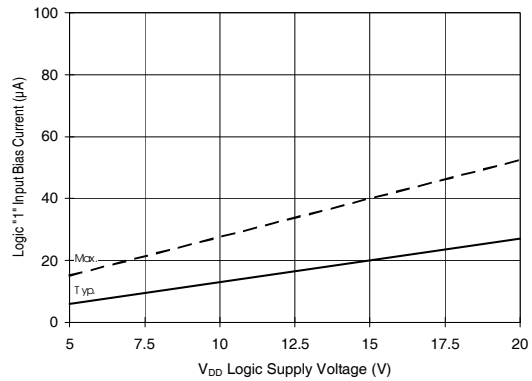


Figure 20B. Logic "1" Input Current vs. Voltage

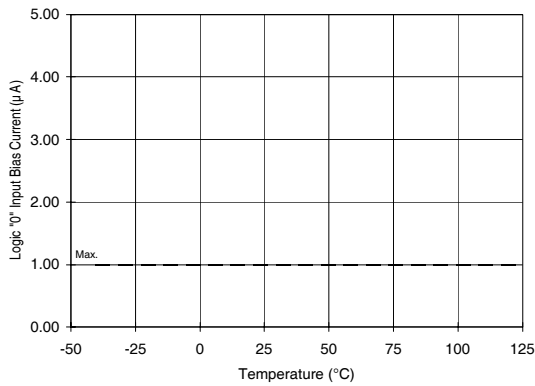


Figure 21A. Logic "0" Input Current vs. Temperature

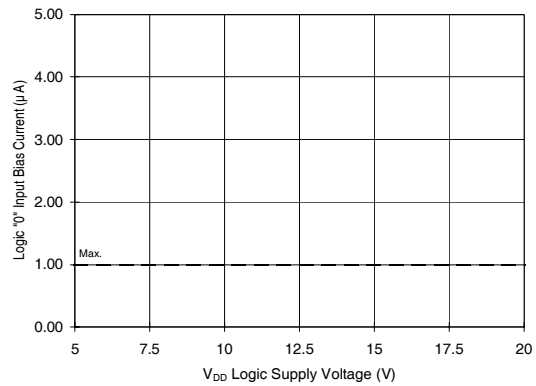


Figure 21B. Logic "0" Input Current vs. Voltage

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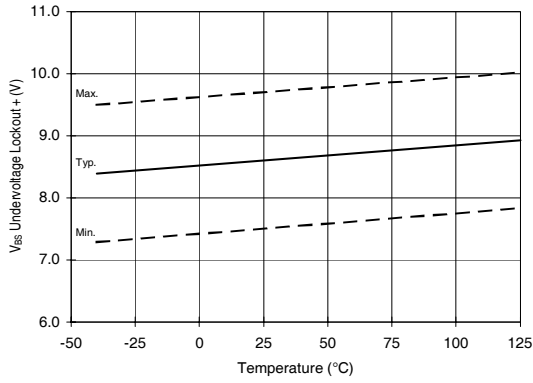


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

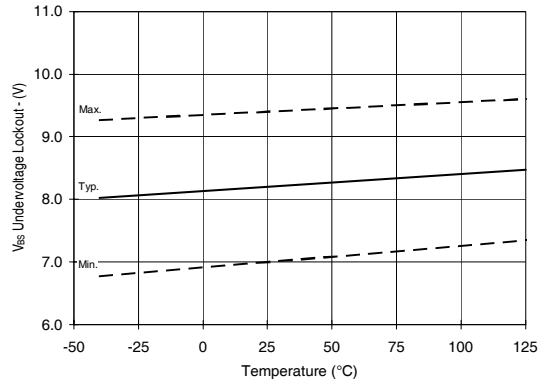


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

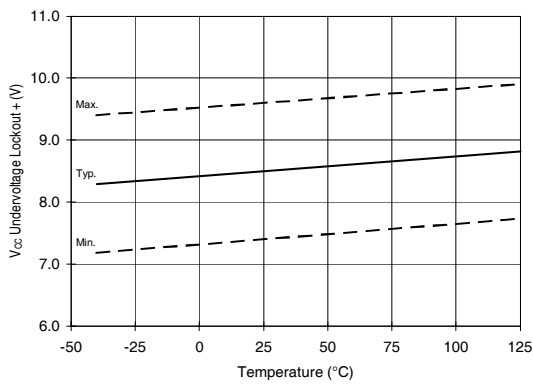


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

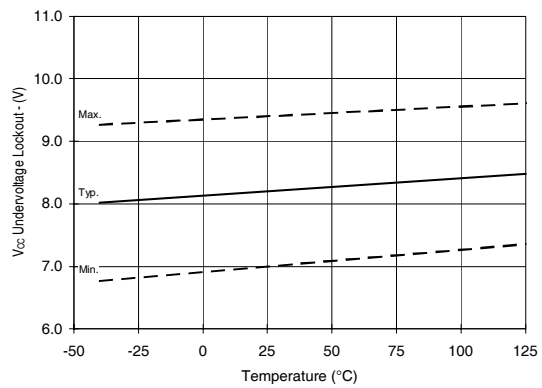


Figure 25. V_{CC} Undervoltage (-) vs. Temperature

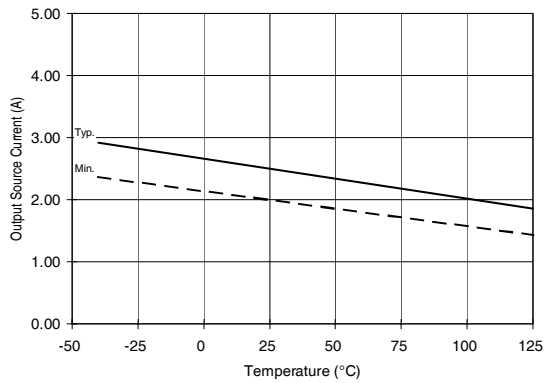


Figure 26A. Output Source Current vs. Temperature

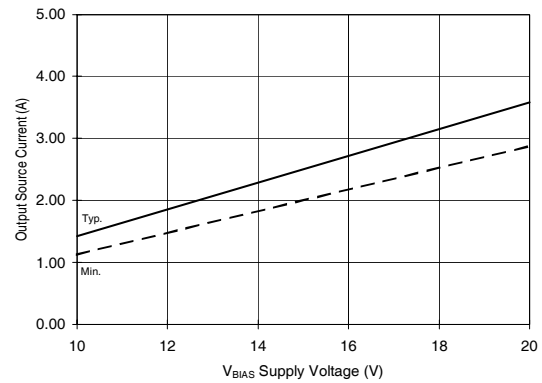


Figure 26B. Output Source Current vs. Voltage

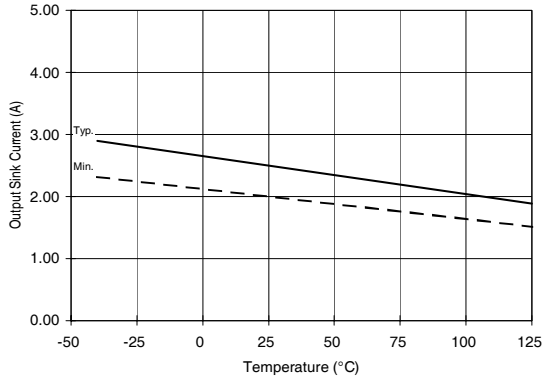


Figure 27A. Output Sink Current vs. Temperature

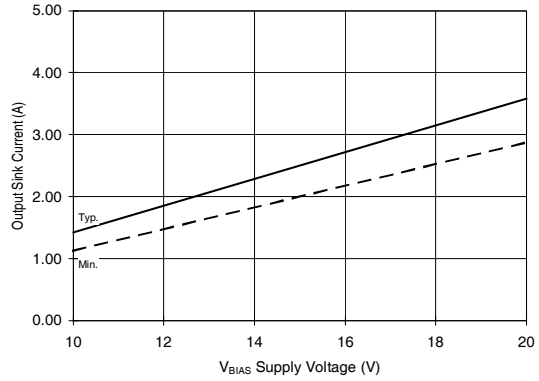


Figure 27B. Output Sink Current vs. Voltage

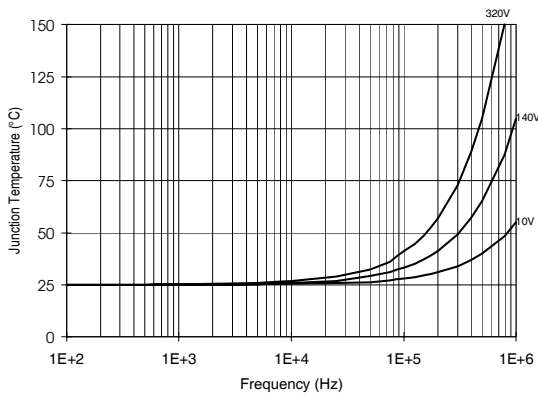


Figure 28. IR2110L6 T_J vs. Frequency (IRFBC20)
 $R_{GATE} = 33W$, $V_{CC} = 15V$

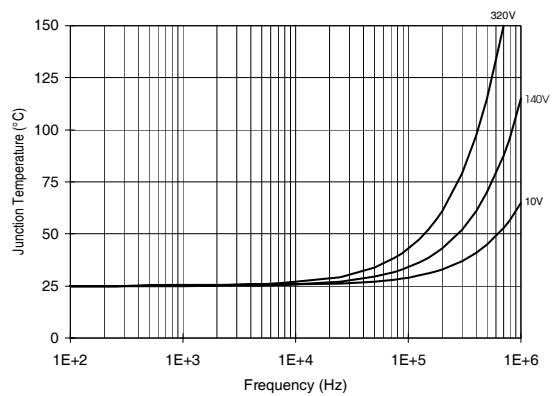


Figure 29. IR2110L6 T_J vs. Frequency (IRFBC30)
 $R_{GATE} = 22W$, $V_{CC} = 15V$

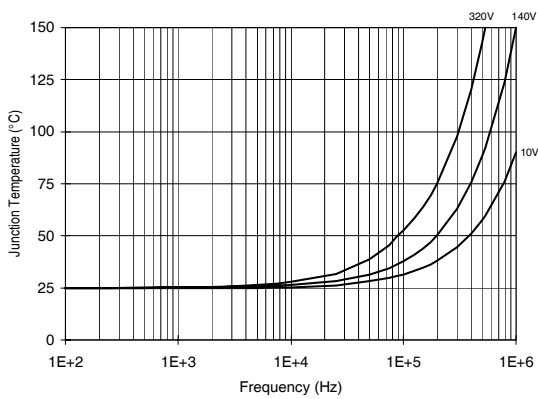


Figure 30. IR2110L6 T_J vs. Frequency (IRFBC40)
 $R_{GATE} = 15W$, $V_{CC} = 15V$

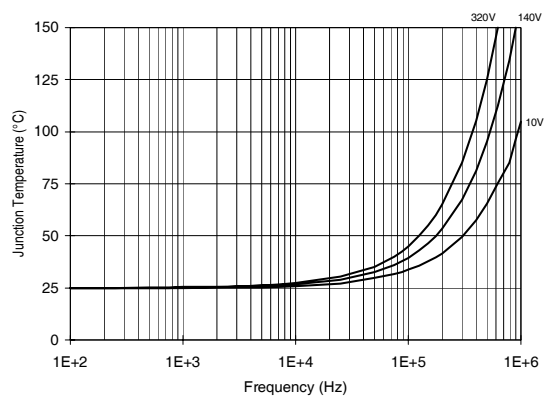


Figure 31. IR2110L6 T_J vs. Frequency (IRFPE50)
 $R_{GATE} = 10W$, $V_{CC} = 15V$

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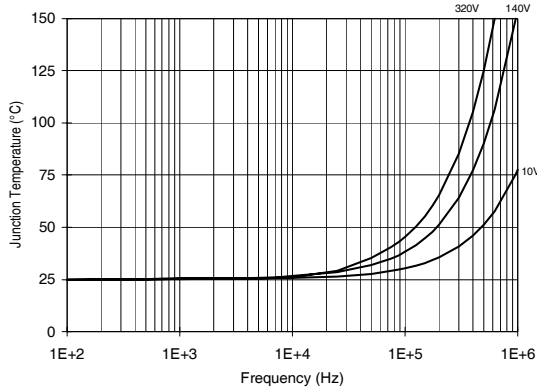


Figure 32. IR2110L6S T_J vs. Frequency (IRFBC20)
 $R_{GATE} = 33W$, $V_{CC} = 15V$

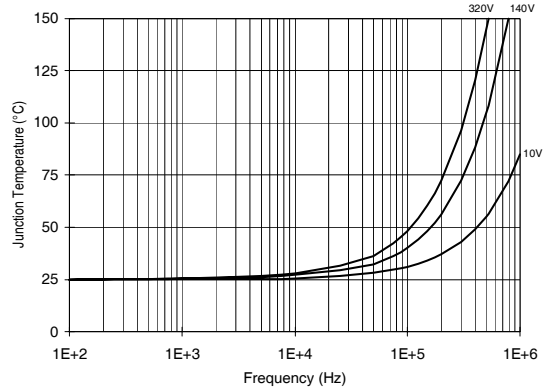


Figure 33. IR2110L6S T_J vs. Frequency (IRFBC30)
 $R_{GATE} = 22W$, $V_{CC} = 15V$

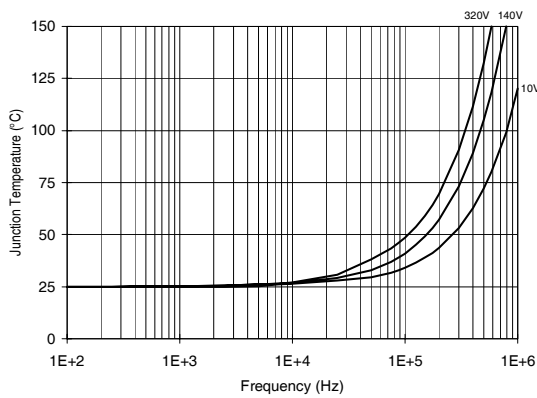


Figure 34. IR2110L6S T_J vs. Frequency (IRFBC40)
 $R_{GATE} = 15W$, $V_{CC} = 15V$

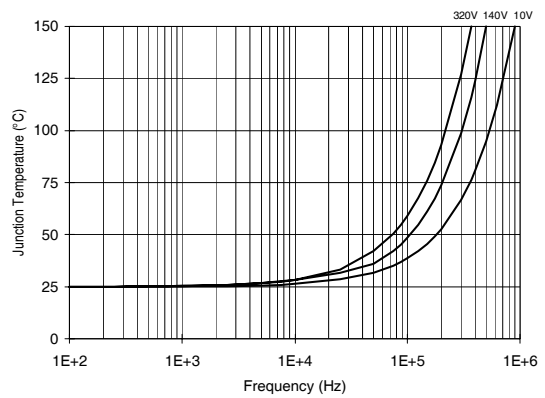


Figure 35. IR2110L6S T_J vs. Frequency (IRFPE50)
 $R_{GATE} = 10W$, $V_{CC} = 15V$

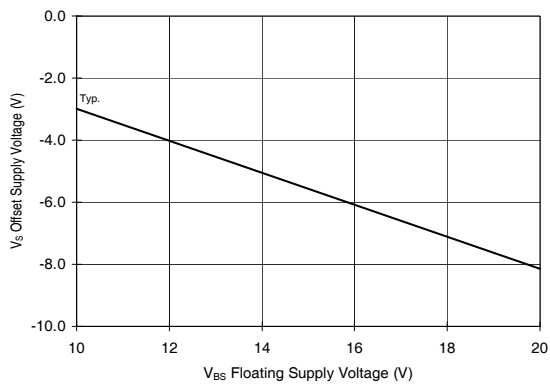


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

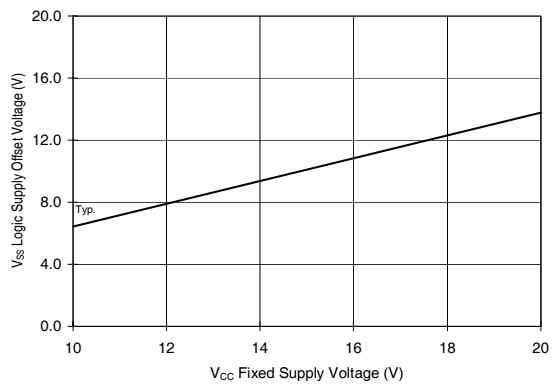
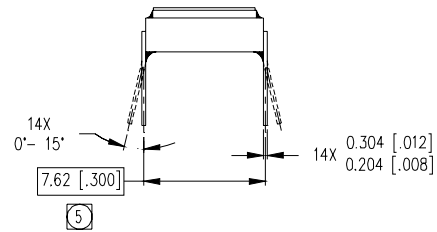
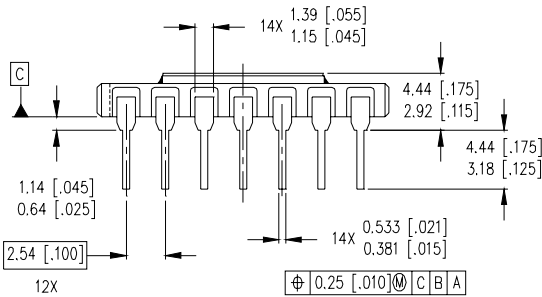
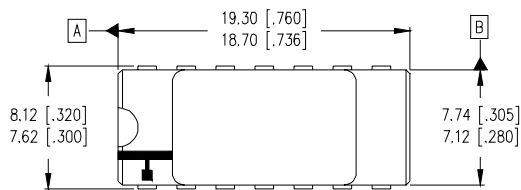
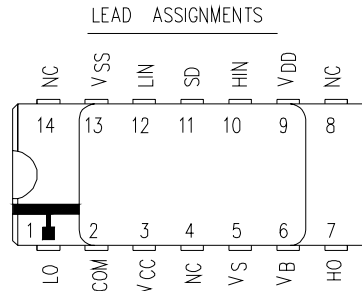
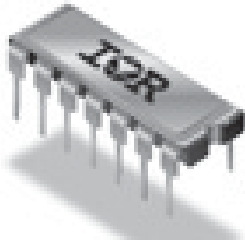


Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

IR2110L4

International
IR Rectifier

Case Outline and Dimensions — MO-036AB



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MO-036AB.
- ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

International
IR Rectifier

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Data and specifications subject to change without notice. 05/2011