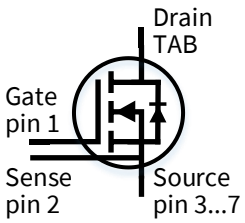
IMBG120R060M1H

CoolSiC™ 1200V SiC Trench MOSFET with .XT interconnection technology

Features

- Very low switching losses
- Short circuit withstand time 3 µs
- Fully controllable dV/dt
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.5V
- Robust against parasitic turn on, 0V turn-off gate voltage can be applied
- Robust body diode for hard commutation
- .XT interconnection technology for best-in-class thermal performance
- Package creepage and clearance distance > 6.1mm
- Sense pin for optimized switching performance



Benefits

- Efficiency improvement
- Enabling higher frequency
- Increased power density
- Cooling effort reduction
- Reduction of system complexity and cost

Potential applications

- Drives
- Infrastructure – Charger
- Energy generation - Solar string inverter and solar optimizer
- Industrial power supplies - Industrial UPS

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC 47/20/22

Note: the source and sense pins are not exchangeable, their exchange might lead to malfunction

Table 1 Key Performance and Package Parameters

Type	V_{DS}	I_D T_C = 25°C, $R_{th(j\text{-}c,max)}$	$R_{DS(on}$ T_{vj} = 25°C, I_D = 13A, V_{GS} = 18V	$T_{vj,max}$	Marking	Package
IMBG120R060M1H	1200V	36A	60mΩ	175°C	12M1H060	PG-TO263-7

Table of contents

Features **1**
Benefits **1**
Potential applications **1**
Product validation **1**
Table of contents **2**
1 Maximum ratings **3**
2 Thermal resistances **4**
3 Electrical Characteristics **5**
3.1 Static characteristics 5
3.2 Dynamic characteristics 6
3.3 Switching characteristics 7
4 Electrical characteristic diagrams **8**
5 Package drawing **14**
6 Test conditions **15**
Revision history **16**

1 Maximum ratings

For optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Table 2 Maximum ratings

Parameter	Symbol	Value	Unit
Drain-source voltage, $T_{vj} \geq 25°C$	V_{DSS}	1200	V
DC drain current for $R_{th(j\text{-}c,max)}$, limited by T_{vjmax}, V_{GS} = 18V, T_C = 25°C T_C = 100°C	I_D	 36 26	A
Pulsed drain current, t_p limited by T_{vjmax}, V_{GS} = 18V	$I_{D,pulse}$[1]	94	A
DC body diode forward current for $R_{th(j\text{-}c,max)}$, limited by T_{vjmax}, V_{GS} = 0V T_C = 25°C T_C = 100°C	I_{SD}	 38 21	A
Pulsed body diode current, t_p limited by T_{vjmax}	$I_{SD,pulse}$[1]	94	A
Gate-source voltage[2] Max transient voltage, < 1% duty cycle Recommended turn-on gate voltage Recommended turn-off gate voltage	 V_{GS} $V_{GS,on}$ $V_{GS,off}$	 -7… 23 15… 18 0	V
Short-circuit withstand time V_{DD} = 800V, $V_{DS,peak}$ < 1200V, $V_{GS,on}$ = 15V, $T_{j,start}$ = 25°C	t_{SC}	3	µs
Power dissipation, limited by T_{vjmax} T_C = 25°C T_C = 100°C	P_{tot}	 181 90	W
Virtual junction temperature	T_{vj}	-55… 175	°C
Storage temperature	T_{stg}	-55… 150	°C
Soldering temperature Reflow soldering (MSL1 according to JEDEC J-STD-020)	T_{sold}	260	°C

[1] verified by design
[2] **Important note:** The selection of positive and negative gate-source voltages impacts the long-term behavior of the device. The design guidelines described in Application Note *AN2018-09* must be considered to ensure sound operation of the device over the planned lifetime.

2 Thermal resistances

Table 3

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
MOSFET/body diode thermal resistance, junction – case	$R_{th(j-c)}$		-	0.63	0.83	K/W
Thermal resistance, junction – ambient	$R_{th(j-a)}$	leaded	-	-	62	K/W

3 Electrical Characteristics

3.1 Static characteristics

Table 4 Static characteristics (at T_{vj} = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 18V, I_D = 13A,				mΩ
		T_{vj} = 25°C	-	60	83	
		T_{vj} = 100°C	-	76	-	
		T_{vj} = 175°C	-	113	-	
		V_{GS} = 15V, I_D = 13A,				
		T_{vj} = 25°C	-	80	106	
Body diode forward voltage	V_{SD}	V_{GS} = 0V, I_{SD} = 13A				V
		T_{vj} = 25°C	-	4.1	5.2	
		T_{vj} = 100°C	-	4.0	-	
		T_{vj} = 175°C	-	3.9	-	
Gate-source threshold voltage	$V_{GS(th)}$	*(tested after 1 ms pulse at* V_{GS} = 20V*)*				V
		I_D = 5.6mA, V_{DS} = V_{GS}				
		T_{vj} = 25°C	3.5	4.5	5.7	
		T_{vj} =175°C	-	3.6	-	
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0V, V_{DS} = 1200V				µA
		T_{vj} = 25°C	-	0.6	180	
		T_{vj} = 175°C	-	1.9	-	
Gate-source leakage current	I_{GSS}	V_{GS} = 23V, V_{DS} = 0V	-	-	100	nA
		V_{GS} = -7V, V_{DS} = 0V	-	-	-100	nA
Transconductance	g_{fs}	V_{DS} = 20V, I_D = 13A	-	7	-	S
Internal gate resistance	$R_{G,int}$	f = 1MHz, V_{AC} = 25mV	-	6	-	Ω

3.2 Dynamic characteristics

Table 5 Dynamic characteristics (at T_{vj} = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Input capacitance	C_{iss}	V_{DD} = 800V, V_{GS} = 0V, f = 1MHz, V_{AC} = 25mV	-	1145	-	pF
Output capacitance	C_{oss}		-	53	-	
Reverse capacitance	C_{rss}		-	5.5	-	
C_{oss} stored energy	E_{oss}		-	22	-	µJ
Total gate charge	Q_G	V_{DD} = 800V, I_D = 13A, V_{GS} = 0/18V, turn-on pulse	-	34	-	nC
Gate to source charge	$Q_{GS,pl}$		-	8.9	-	
Gate to drain charge	Q_{GD}		-	7.3	-	

3.3 Switching characteristics

Table 6 Switching characteristics, Inductive load [3]

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
MOSFET Characteristics, T_{vj} = 25°C						
Turn-on delay time	$t_{d(on)}$	V_{DD} = 800V, I_D = 13A, V_{GS} = 0/18V, $R_{G,ext}$ = 2Ω, L_σ = 40nH, diode: body diode at V_{GS} = 0V see Fig. E	-	8.9	-	ns
Rise time	t_r		-	4.8	-	
Turn-off delay time	$t_{d(off)}$		-	20	-	
Fall time	t_f		-	9.8	-	
Turn-on energy	E_{on}		-	133	-	µJ
Turn-off energy	E_{off}		-	30	-	
Total switching energy	E_{tot}		-	163	-	
Body Diode Characteristics, T_{vj} = 25°C						
Diode reverse recovery charge	Q_{rr}	V_{DD} = 800V, I_{SD} = 13A, V_{GS} at diode = 0V, di_f/dt = 1000A/µs, Q_{rr} includes also Q_C, see Fig. C	-	165	-	nC
Diode peak reverse recovery current	I_{rrm}		-	2.9	-	A
MOSFET Characteristics, T_{vj} = 175°C						
Turn-on delay time	$t_{d(on)}$	V_{DD} = 800V, I_D = 13A, V_{GS} = 0/18V, $R_{G,ext}$ = 2Ω, L_σ = 40nH, diode: body diode at V_{GS} = 0V see Fig. E	-	8.9	-	ns
Rise time	t_r		-	11	-	
Turn-off delay time	$t_{d(off)}$		-	20	-	
Fall time	t_f		-	9.8	-	
Turn-on energy	E_{on}		-	200	-	µJ
Turn-off energy	E_{off}		-	36	-	
Total switching energy	E_{tot}		-	236	-	
Body Diode Characteristics, T_{vj} = 175°C						
Diode reverse recovery charge	Q_{rr}	V_{DD} = 800V, I_{SD} = 13A, V_{GS} at diode = 0V, di_f/dt = 1000A/µs, Q_{rr} includes also Q_C, see Fig. C	-	206	-	nC
Diode peak reverse recovery current	I_{rrm}		-	3.8	-	A

[3] The chip technology was characterized up to 200 kV/µs. The measured dV/dt was limited by measurement test setup and package.

4 Electrical characteristic diagrams

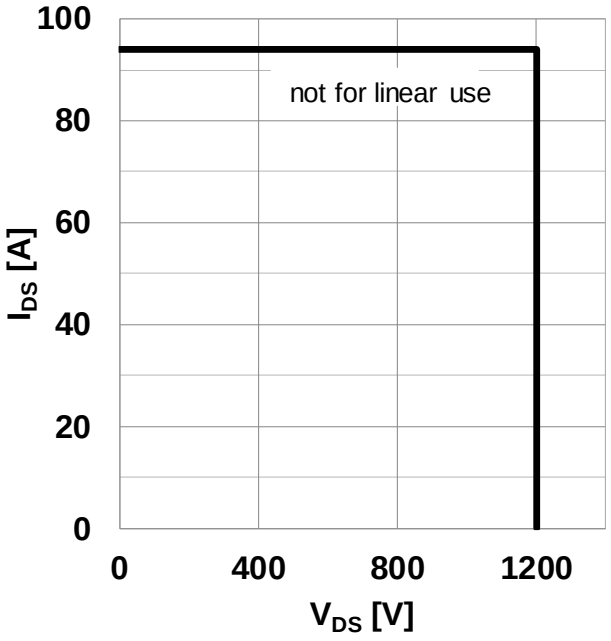


Figure 1 **Safe operating area (SOA)**
(V_{GS} = 0/18V, T_c = 25°C, $T_j \leq$ 175°C)

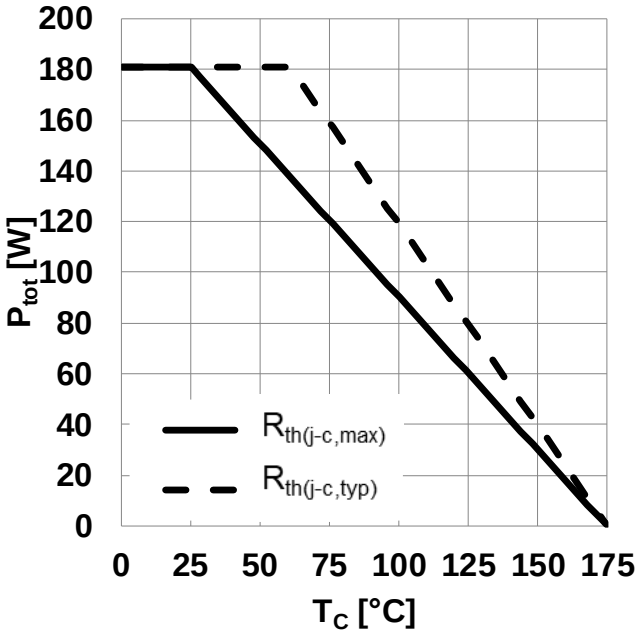


Figure 2 **Power dissipation as a function of case temperature limited by bond wire**
(P_{tot} = f(T_C))

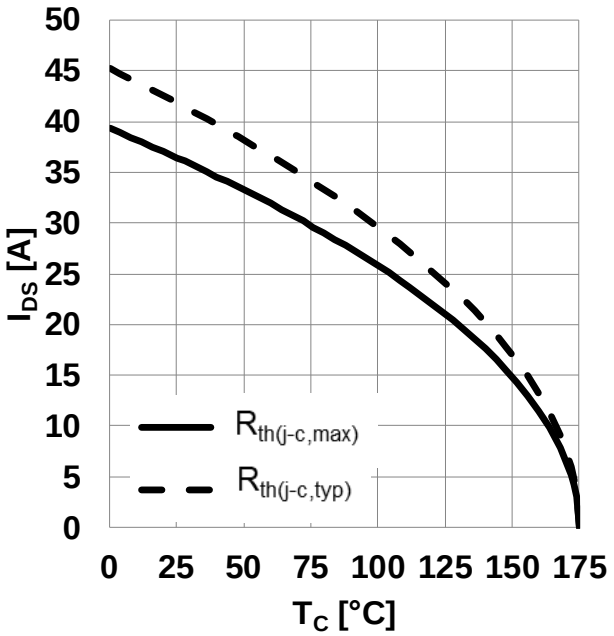


Figure 3 **Maximum DC drain to source current as a function of case temperature limited by bond wire** (I_{DS} = f(T_C))

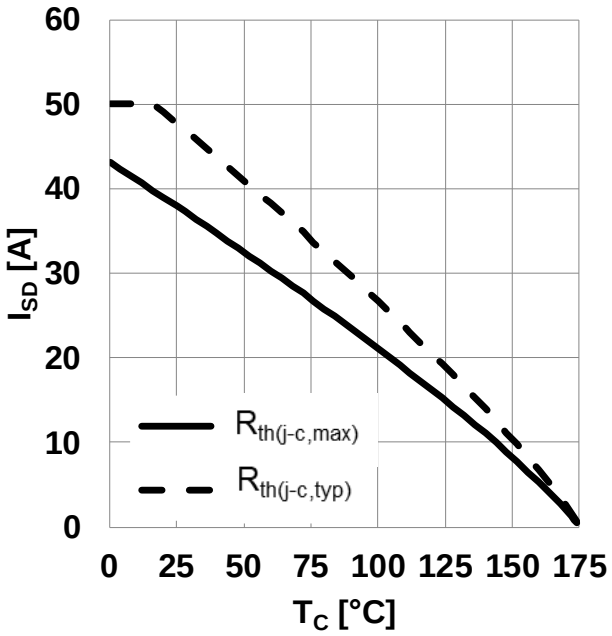


Figure 4 **Maximum source to drain current as a function of case temperature limited by bond wire** (I_{SD} = f(T_C), V_{GS} = 0V)

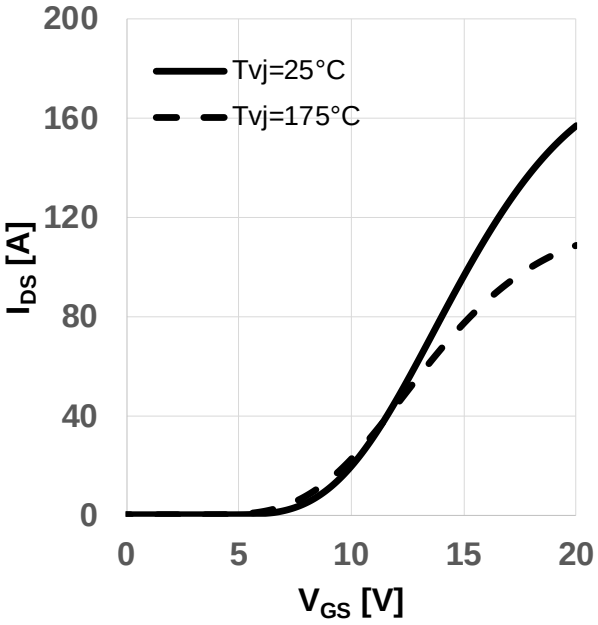


Figure 5 **Typical transfer characteristic**
(I_{DS} = f(V_{GS}), V_{DS} = 20V, t_P = 20µs)

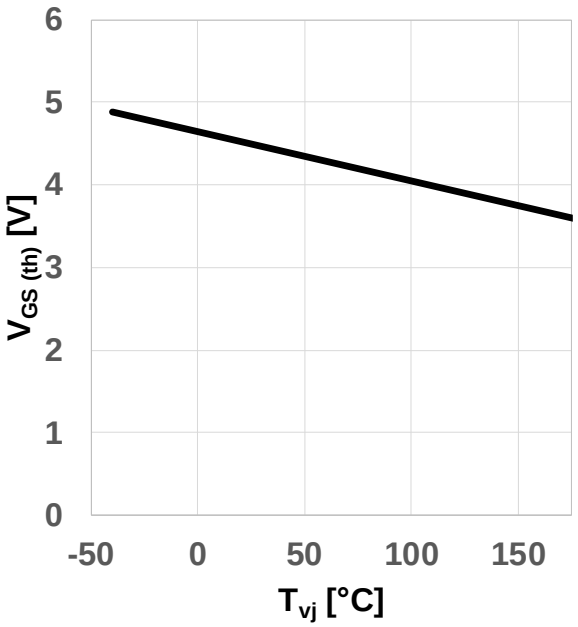


Figure 6 **Typical gate-source threshold voltage as a function of junction temperature**
($V_{GS(th)}$ = f(T_{vj}), I_{DS} = 5.6mA, V_{GS} = V_{DS})

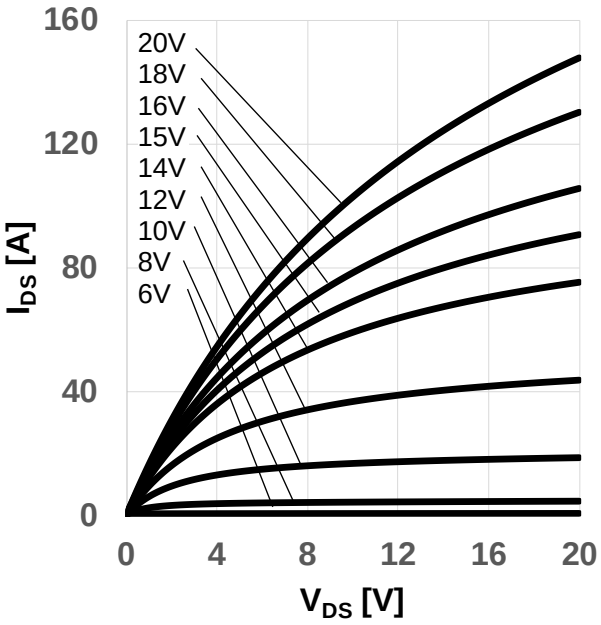


Figure 7 **Typical output characteristic, V_{GS} as parameter**
(I_{DS} = f(V_{DS}), T_{vj}=25°C, t_P = 20µs)

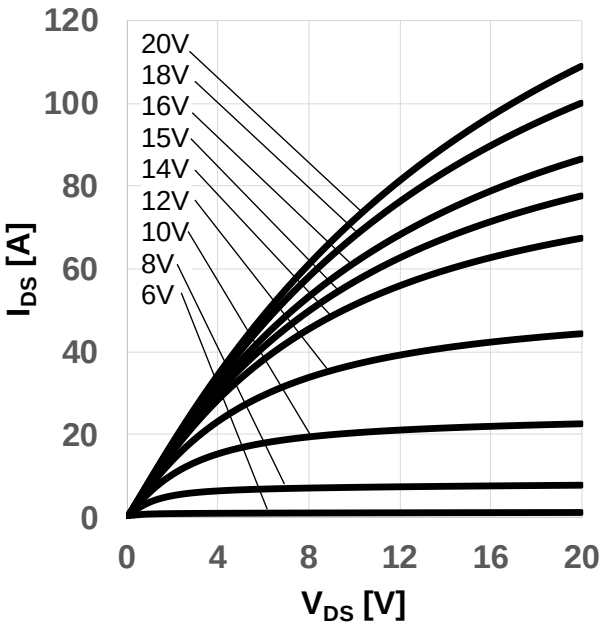


Figure 8 **Typical output characteristic, V_{GS} as parameter**
(I_{DS} = f(V_{DS}), T_{vj}=175°C, t_P = 20µs)

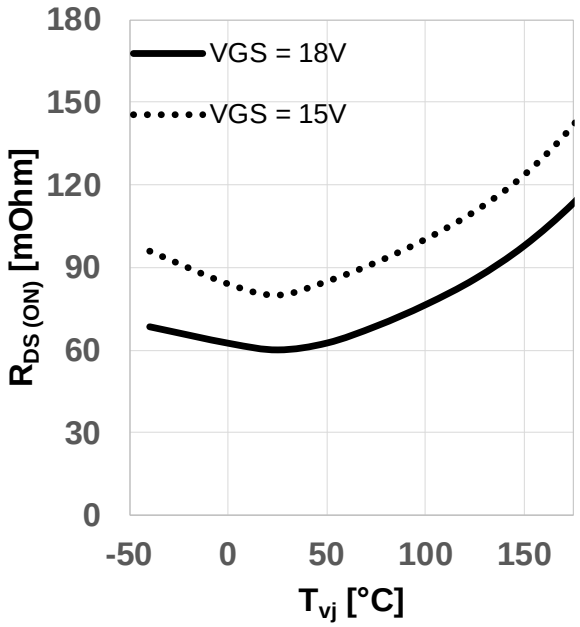


Figure 9 **Typical on-resistance as a function of junction temperature**
($R_{DS(on)} = f(T_{vj})$, $I_{DS} = 13A$)

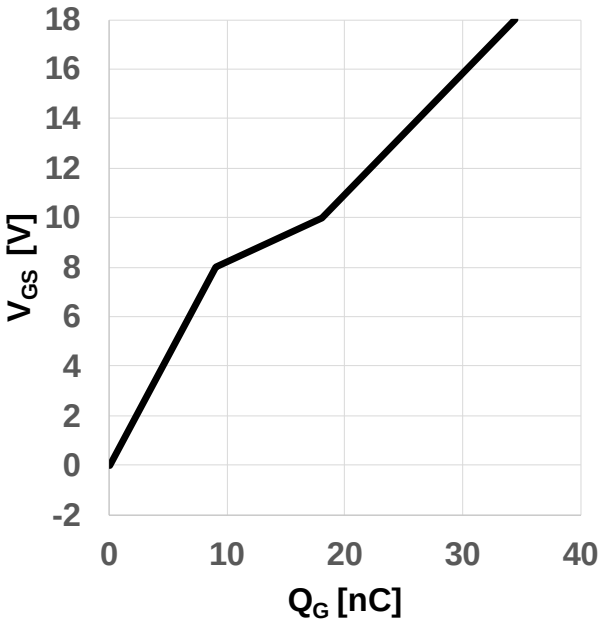


Figure 10 **Typical gate charge**
($V_{GS} = f(Q_G)$, $I_{DS} = 13A$, $V_{DS} = 800V$, turn-on pulse)

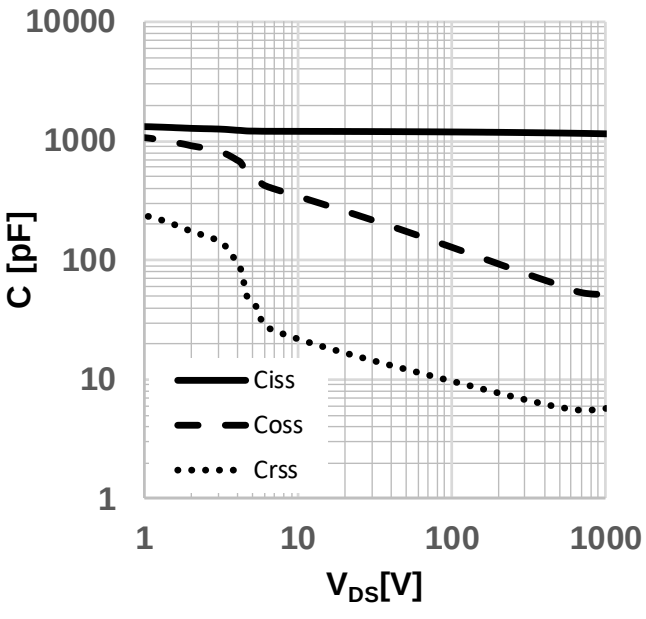


Figure 11 **Typical capacitance as a function of drain-source voltage**
($C = f(V_{DS})$, $V_{GS} = 0V$, $f = 1MHz$)

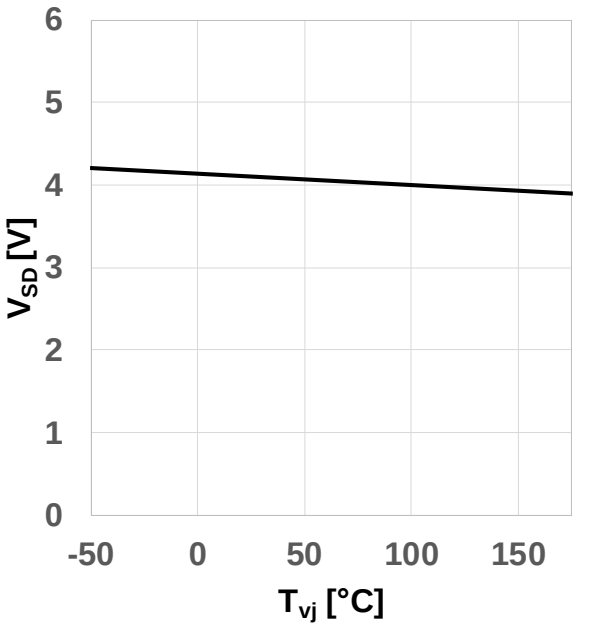


Figure 12 **Typical body diode forward voltage as function of junction temperature**
($V_{SD} = f(T_{vj})$, $V_{GS} = 0V$, $I_{SD} = 13A$)

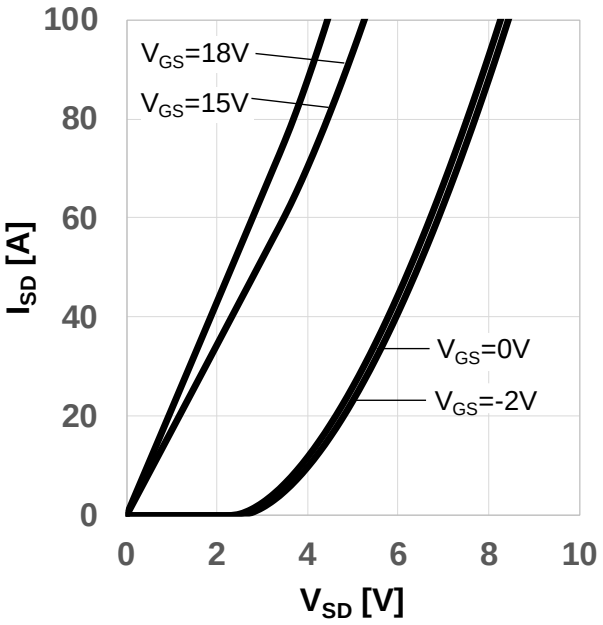


Figure 13 **Typical body diode forward current as function of forward voltage, V_{GS} as parameter**
(I_{SD} = f(V_{SD}), T_{vj} = 25°C, t_P = 20µs)

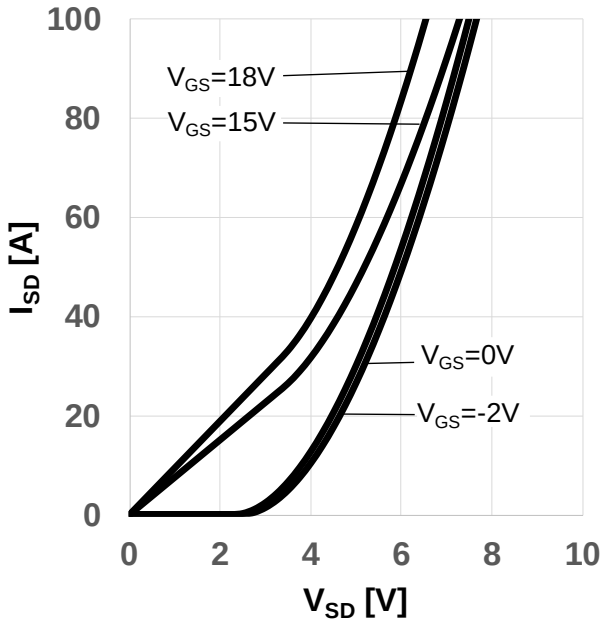


Figure 14 **Typical body diode forward current as function of forward voltage, V_{GS} as parameter**
(I_{SD} = f(V_{SD}), T_{vj} = 175°C, t_P = 20µs)

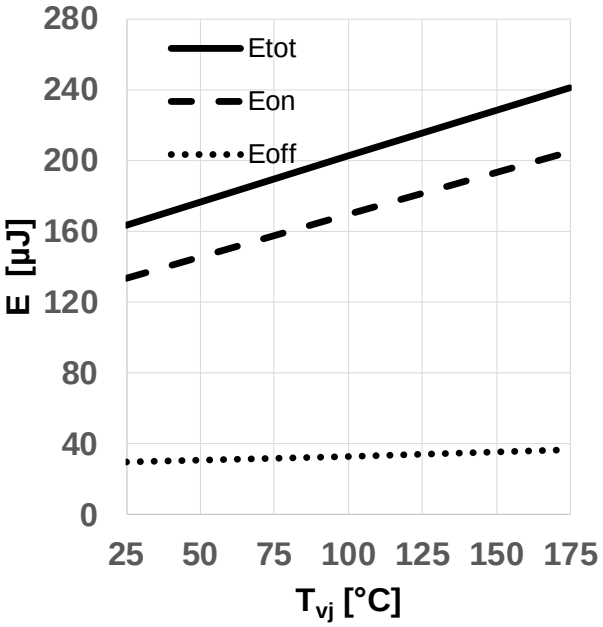


Figure 15 **Typical switching energy losses as a function of junction temperature**
(E = f(T_{vj}), V_{DD} = 800V, V_{GS} = 0V/18V, $R_{G,ext}$ = 2Ω, I_D = 13A, ind. load, test circuit in Fig. E, diode: body diode at V_{GS} = 0V)

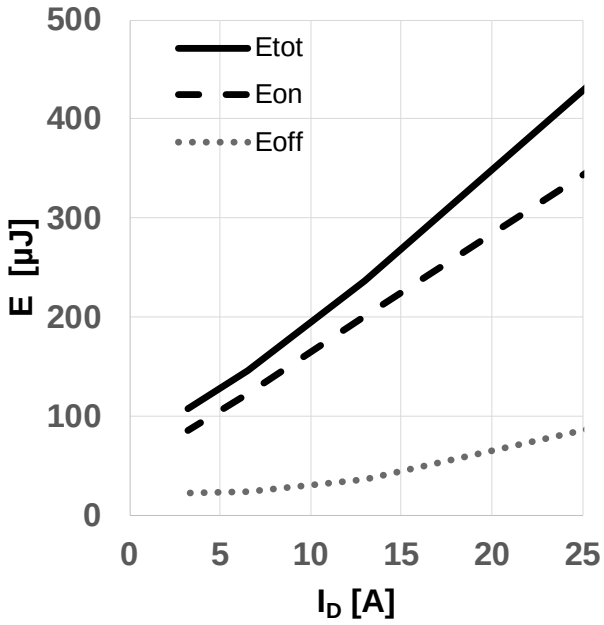


Figure 16 **Typical switching energy losses as a function of drain-source current**
(E = f(I_{DS}), V_{DD} = 800V, V_{GS} = 0V/18V, $R_{G,ext}$ = 2Ω, T_{vj} = 175°C, ind. load, test circuit in Fig. E, diode: body diode at V_{GS} = 0V)

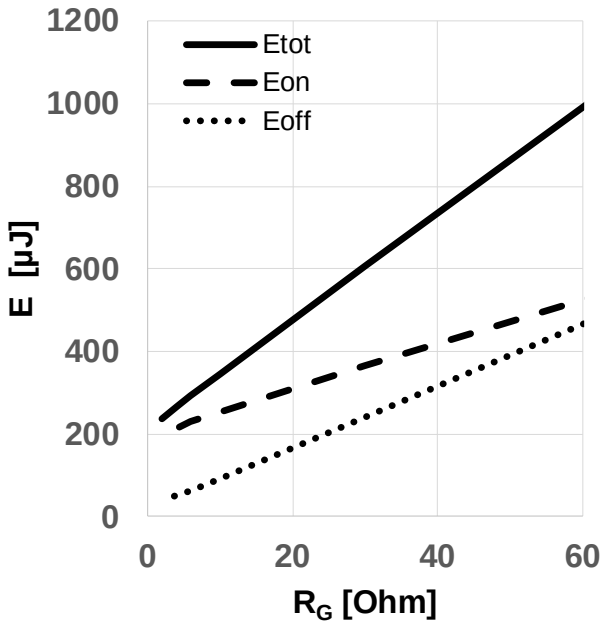


Figure 17 **Typical switching energy losses as a function of gate resistance**
(E = f($R_{G,ext}$), V_{DD} = 800V, V_{GS} = 0V/18V, I_D = 13A, T_{vj} = 175°C, ind. load, test circuit in Fig. E, diode: body diode at V_{GS} = 0V)

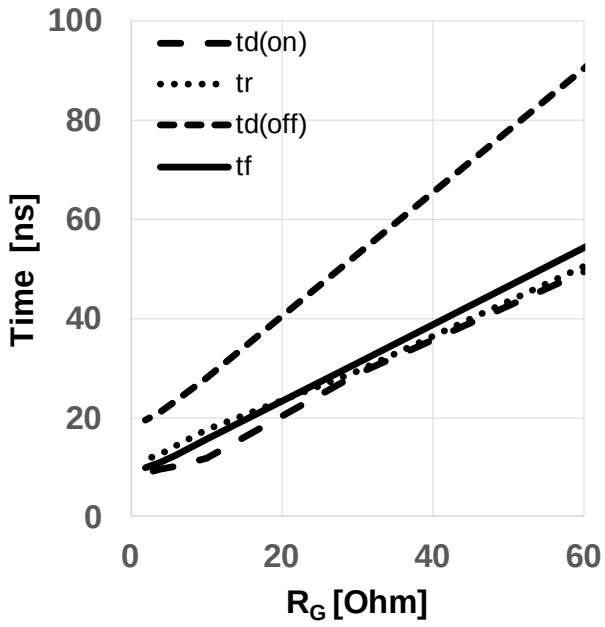


Figure 18 **Typical switching times as a function of gate resistor**
(t = f($R_{G,ext}$), V_{DD} = 800V, V_{GS} = 0V/18V, I_D = 13A, T_{vj} = 175°C, ind. load, test circuit in Fig. E, diode: body diode at V_{GS} = 0V)

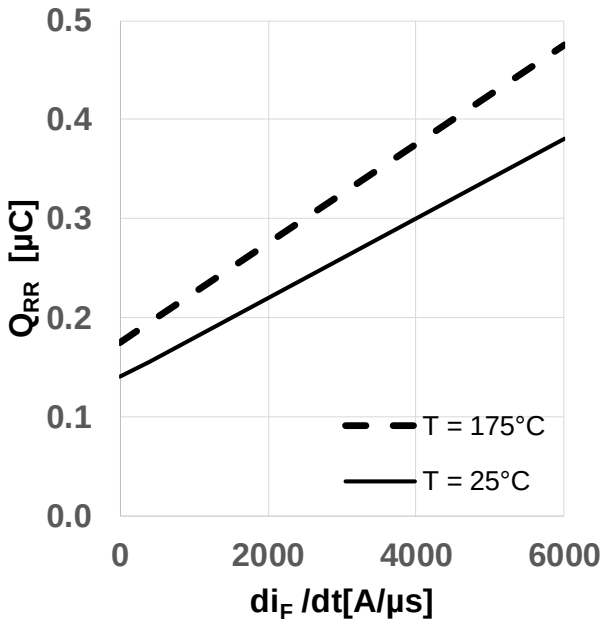


Figure 19 **Typical reverse recovery charge as a function of diode current slope**
(Q_{rr} = f(di_f/dt), V_{DD} = 800V, V_{GS} = 0V/18V, I_D = 13A, ind. load, test circuit in Fig.E, body diode at V_{GS} = 0V)

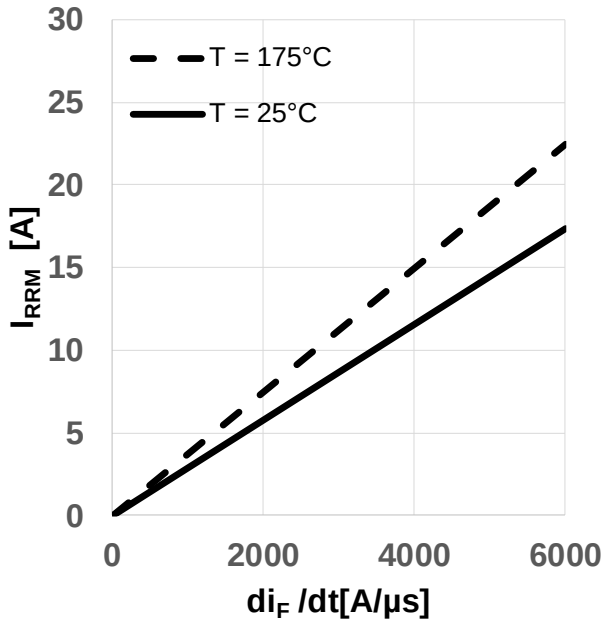
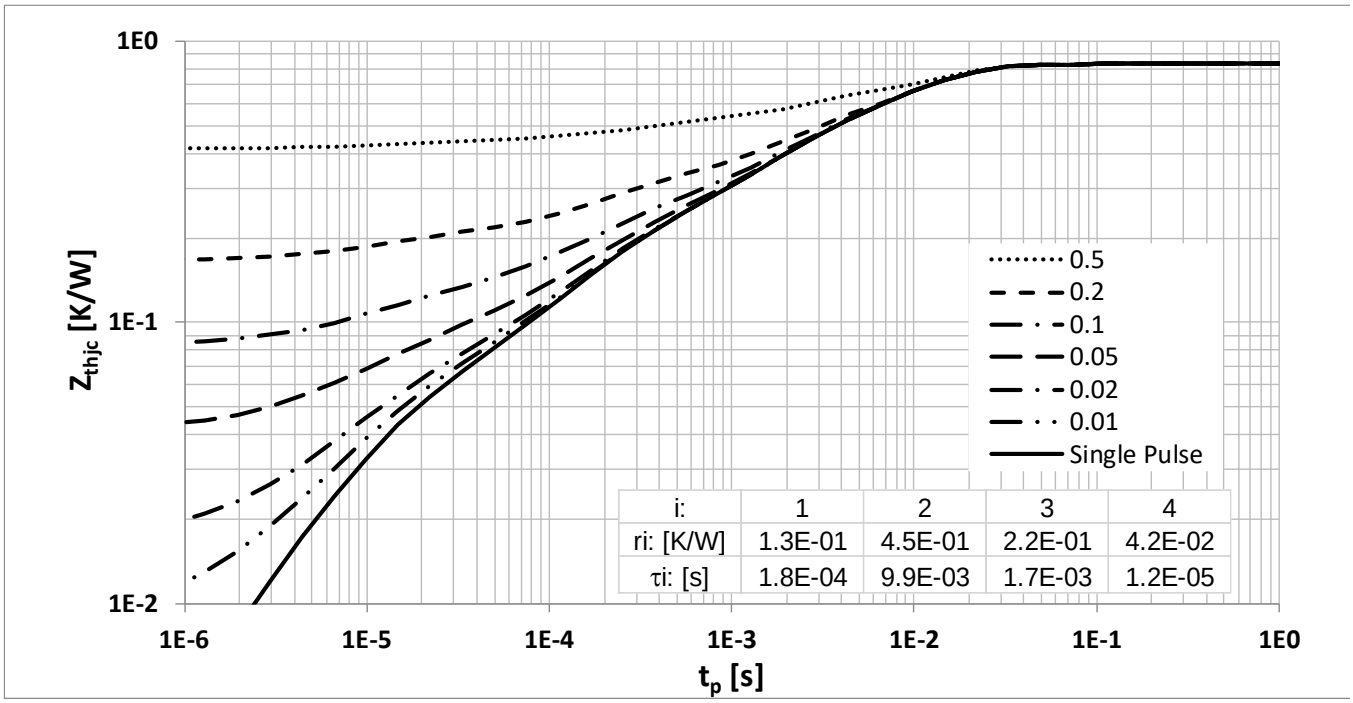


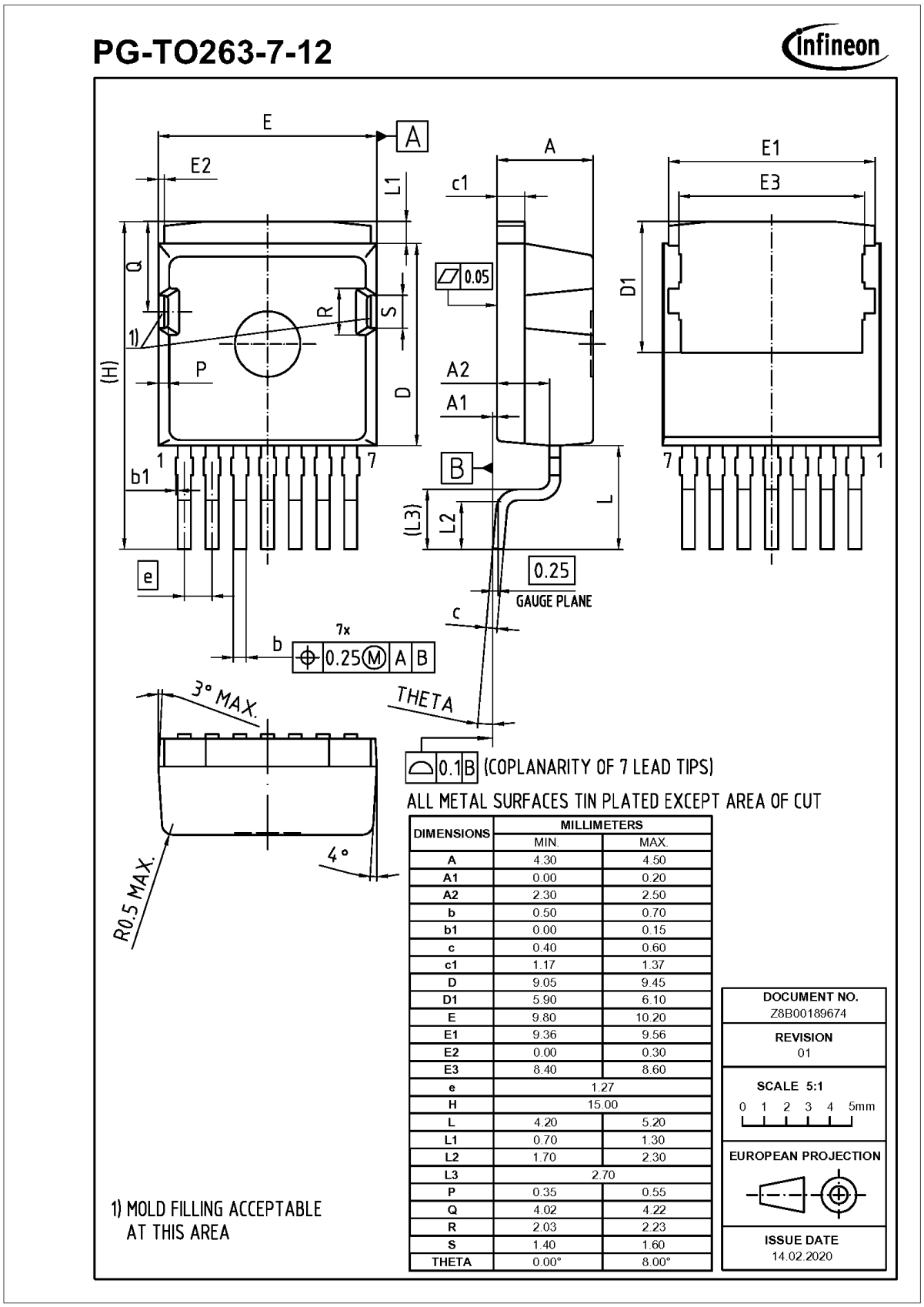
Figure 20 **Typical reverse recovery current as a function of diode current slope**
(I_{rrm} = f(di_f/dt), V_{DD} = 800V, V_{GS} = 0V/18V, I_D = 13A, ind. load, test circuit in Fig.E, body diode at V_{GS} = 0V)



i:	1	2	3	4
ri: [K/W]	1.3E-01	4.5E-01	2.2E-01	4.2E-02
τi: [s]	1.8E-04	9.9E-03	1.7E-03	1.2E-05

Figure 21 Max. transient thermal resistance (MOSFET/diode)
($Z_{th(j\text{-}c,max)} = f(t_P)$, parameter $D = t_p/T$, thermal equivalent circuit in Fig. D)

5 Package drawing



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.30	4.50
A1	0.00	0.20
A2	2.30	2.50
b	0.50	0.70
b1	0.00	0.15
c	0.40	0.60
c1	1.17	1.37
D	9.05	9.45
D1	5.90	6.10
E	9.80	10.20
E1	9.36	9.56
E2	0.00	0.30
E3	8.40	8.60
e	1.27	
H	15.00	
L	4.20	5.20
L1	0.70	1.30
L2	1.70	2.30
L3	2.70	
P	0.35	0.55
Q	4.02	4.22
R	2.03	2.23
S	1.40	1.60
THETA	0.00°	8.00°

Figure 22 Package drawing

6 Test conditions

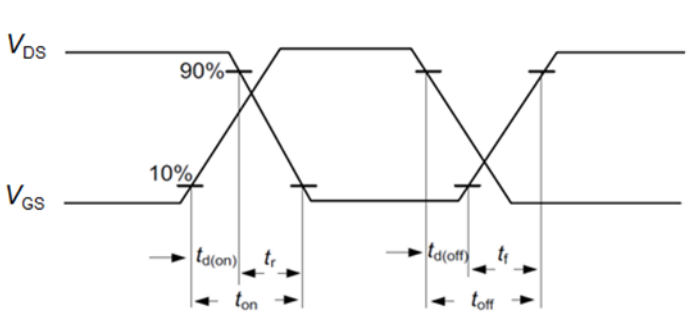


Figure A. **Definition of switching times**

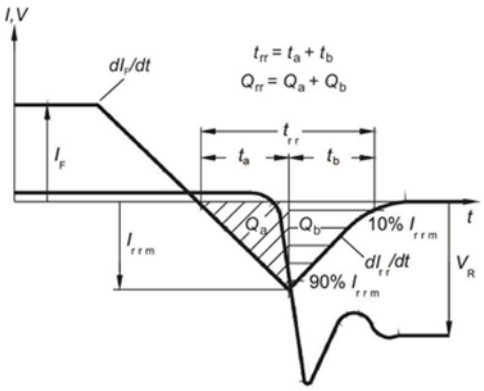


Figure C. **Definition of diode switching characteristics**

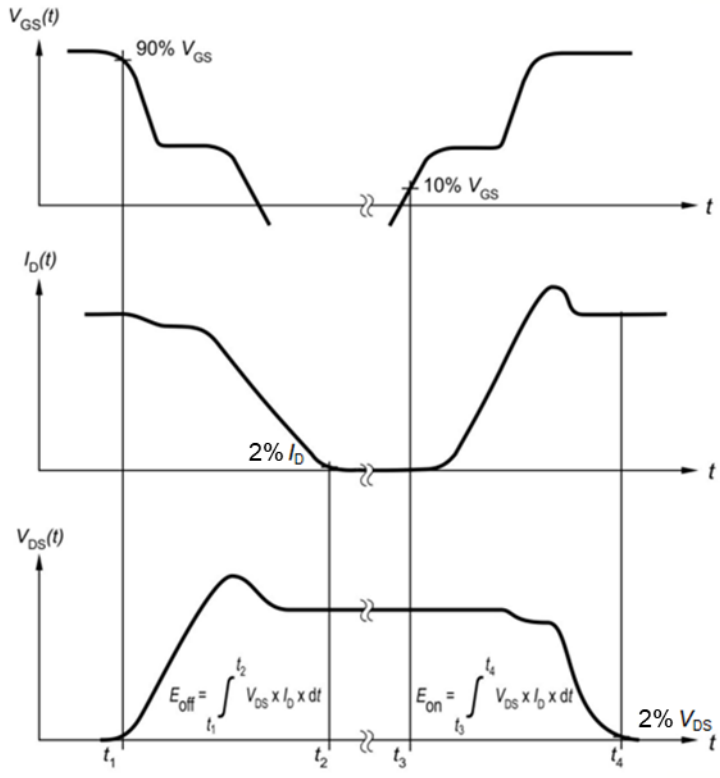


Figure B. **Definition of switching losses**

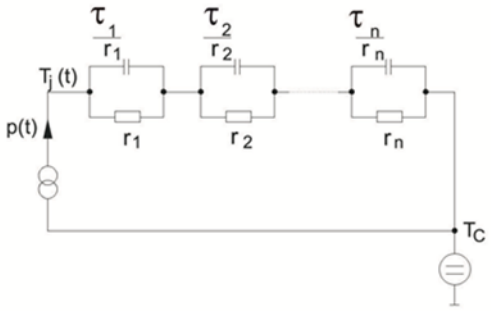


Figure D. **Thermal equivalent circuit**

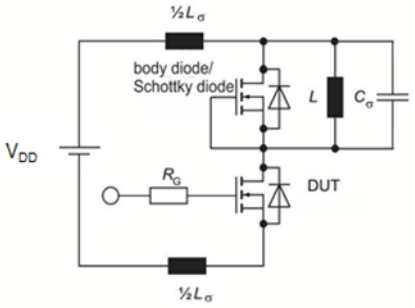


Figure E. **Dynamic test circuit**
Parasitic inductance L_σ,
parasitic capacitor C_σ,

Figure 23 Test conditions

Revision history

Document version	Date of release	Description of changes
2.1	2020-09-01	Final Datasheet
2.2	2020-12-11	Correction of circuit symbol on page 1

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