

High and Low Side Driver

Features

- Floating channel designed for bootstrap operation
- Fully operational to 200V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
- Separate logic supply range from 3.3V to 20V
- Logic and power ground +/-5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Shut down input turns off both channels
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

V _{OFFSET} (max)	200V
I _{O+/-} (typ)	3.0A / 3.0A
V_{OUT}	10 – 20V
t _{on/off} (typ)	95ns & 65ns
Delay Matching (max)	15ns

Description

The IR2010 is a high power, high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.0V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 200 volts. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.

Package Options





14-Lead PDIP

16-Lead SOIC Wide Body

Applications

- Converters
- DC motor drive

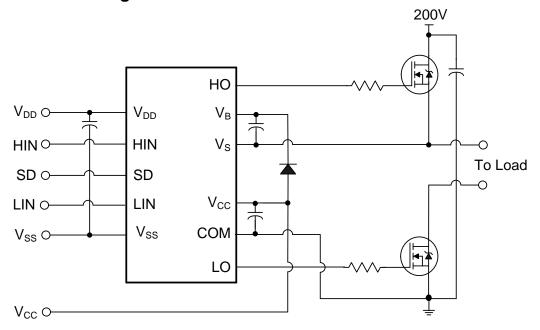
Ordering Information

Dana Dani Namakan		Standar	d Pack	Onderskie Deut Neusken	
Base Part Number	Package Type	Form	Quantity	Orderable Part Number	
IR2010PBF	PDIP14	Tube	25	IR2010PBF	
IR2010SPBF	SO16W	Tube	45	IR2010SPBF	
IR2010SPBF	SO16W	Tape and Reel	1000	IR2010STRPBF	

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Typical Connection Diagram



(Refer to Lead Assignments for correct configuration.) This diagram shows electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V_{B}	High side floating supply voltage		-0.3	225	
Vs	High side floating supply offset volta	ige	V _B - 25	$V_B + 0.3$	
V_{HO}	High side floating output voltage		V _S - 0.3	$V_B + 0.3$	V
V _{cc}	Low side fixed supply voltage		-0.3	25	7 °
V_{LO}	Low side output voltage		-0.3	V _{CC} + 0.3	
V_{DD}	Logic supply voltage		-0.3	V _{SS} + 25	
V _{SS}	Logic supply offset voltage		V _{CC} - 25	$V_{CC} + 0.3$	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V _{SS} - 0.3	$V_{DD} + 0.3$	
dV _s /dt	Allowable offset supply voltage trans	sient (figure 2)	_	50	V/ns
Ъ	Package power dissipation	14-Lead PDIP	_	1.6	10/
P_D	@ T _A ≤ +25°C	16-Lead SOIC	_	1.25	W
Duk	Thermal resistance, junction to	14-Lead PDIP	_	75	0000
Rth _{JA}	Rth _{JA} ambient		_	100	°C/W
T _J	Junction temperature	_	150		
Ts	Storage temperature	-55	150	°C	
T _L	Lead temperature (soldering, 10 sec	_	300		

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating is tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in figures 24 and 25.

Symbol	Definition	Min.	Max.	Units
V_{B}	High side floating supply absolute voltage	V _S + 10	V _S + 20	
Vs	High side floating supply offset voltage	†	200	
V_{HO}	High side floating output voltage	Vs	V_{B}	V
V_{CC}	Low side fixed supply voltage	10	20]
V_{LO}	Low side output voltage	0	V _{CC}	
V_{DD}	Logic supply voltage	V _{SS} + 3	V _{SS} + 20	
V _{SS}	Logic supply offset voltage	-5 ^{††}	5	
V _{IN}	Logic input voltage (HIN, LIN, & SD)	V _{SS}	V_{DD}	
T _A	Ambient temperature	-40	125	°C

⁺ Logic operational for V_S of -4 to +200V. Logic state held for V_S of -4V to - V_{BS} .

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⁺⁺ When V_{DD} < 5V, the minimum V_{SS} offset is limited to - V_{DD} (Please refer to the Design Tip DT97-3 for more details).



Dynamic Electrical Characteristics

 V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, C_L = 1000pF and T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in figure 3.

Symbol	Definition	Figure	Min.	Тур.	Max.	Units	Test Conditions
t _{on}	Turn-on propagation delay	7	50	95	135		$V_S = 0V$
t _{off}	Turn-off propagation delay	8	30	65	105		V _S = 200V
t _{sd}	Shutdown propagation delay	9	35	70	105	20	V _S = 200 V
t _r	Turn-on rise time	10	_	10	20	ns	
t _f	Turn-off fall time	11	_	15	25		
MT	Delay matching, HS & LS turn-on/off	6	_	_	15		

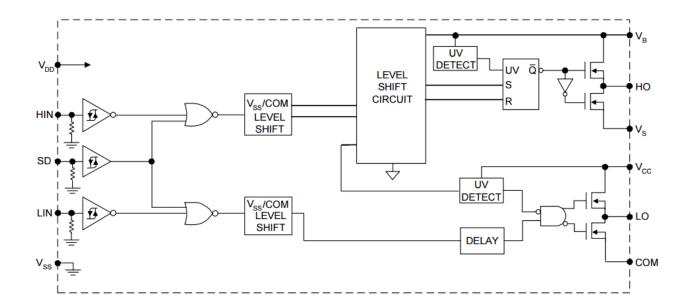
Static Electrical Characteristics

 V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V and T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Тур.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	12	9.5	_			$V_{DD} = 15V$
V_{IL}	Logic "0" input voltage	13		_	6.0		V _{DD} = 13V
V_{IH}	Logic "1" input voltage	12	2	_		V	$V_{DD} = 3.3V$
V_{IL}	Logic "0" input voltage	13	_	_	1]	$v_{DD} = 3.3v$
V_{OH}	High level output voltage, V _{BIAS} - V _O	14		_	1.0		$I_O = 0A$
V_{OL}	Low level output voltage, V _O	15		_	0.1		1 ₀ = 0A
I_{LK}	Offset supply leakage current	16		_	50		$V_{B} = V_{S} = 200V$
I_{QBS}	Quiescent V _{BS} supply current	17	_	70	210		
I _{QCC}	Quiescent V _{CC} supply current	18	_	100	230		$V_{IN} = 0V \text{ or } V_{DD}$
I_{QDD}	Quiescent V _{DD} supply current	19	_	1	5	μA	
I _{IN+}	Logic "1" input bias current	20	_	20	40		$V_{IN} = V_{DD}$
I _{IN-}	Logic "0" input bias current	21	_	_	1.0		$V_{IN} = 0V$
V _{BSUV+}	V _{BS} supply undervoltage positive going threshold	22	7.5	8.6	9.7		
V _{BSUV} -	V _{BS} supply undervoltage negative going threshold	23	7.0	8.2	9.4	V	
V _{CCUV+}	V _{CC} supply undervoltage positive going threshold	24	7.5	8.6	9.7	V	
V _{CCUV} -	V _{CC} supply undervoltage negative going threshold	25	7.0	8.2	9.4		
I _{O+}	Output high short circuit pulsed current	26	2.5	3.0	_	Α	$V_O = 0V$, $V_{IN} = V_{DD}$ $PW \le 10 \mu s$
I _{O-}	Output low short circuit pulsed current	27	2.5	3.0	_		$V_O = 15V$, $V_{IN} = 0V$ PW $\leq 10 \mu s$



Functional Block Diagram

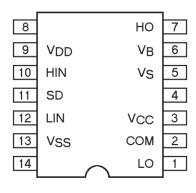




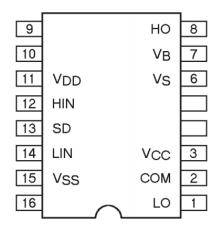
Lead Definitions

Symbol	Description
V_{DD}	Logic Supply
HIN	Logic input for high side gate driver outputs (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver outputs (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
НО	High side gate drive output
Vs	High side floating supply return
V _{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



14-Lead PDIP

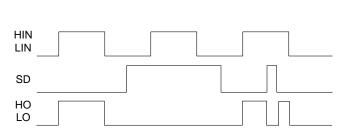


16-Lead SOIC (Wide Body)

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Application Information and Additional Details



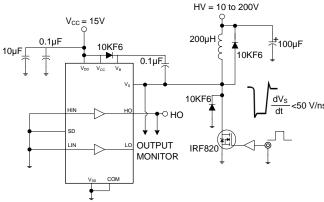
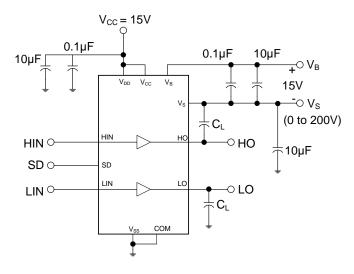


Figure 1. Input/Output Timing Diagram

Figure 2. Floating Supply Voltage Transient Test Circuit



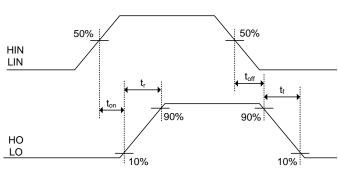


Figure 3. Switching Time Test Circuit

Figure 5. Shutdown Waveform Definitions

Figure 4. Switching Time Waveform Definition

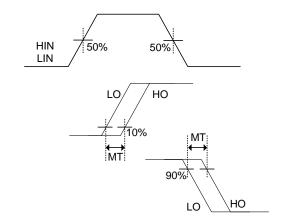
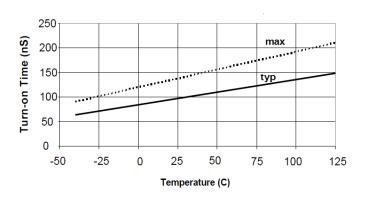


Figure 6. Delay Matching Waveform Definitions





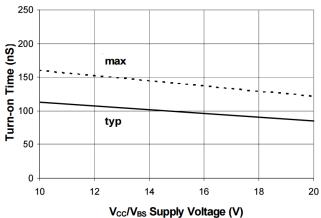
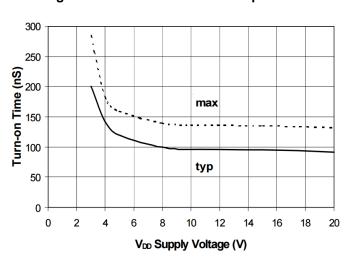


Figure 7A. Turn-on Time vs. Temperature

Figure 7B. Turn-on Time vs. V_{CC}/V_{BS} Voltage



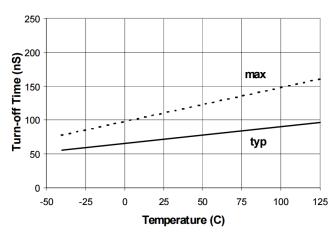
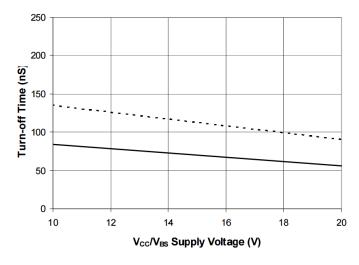


Figure 7C. Turn-on Time vs. V_{DD} Voltage

Figure 8A. Turn-off Time vs. Temperature



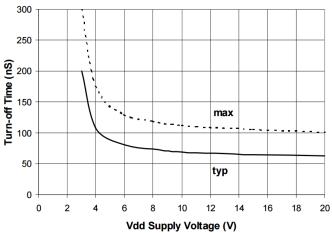
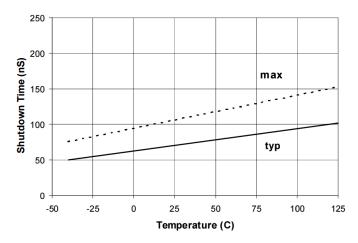


Figure 8B. Turn-off Time vs. V_{CC}/V_{BS} Voltage

Figure 8C. Turn-off Time vs. V_{DD} Voltage





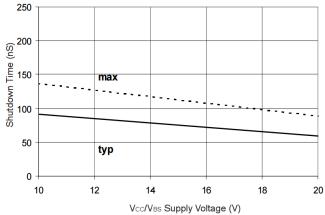
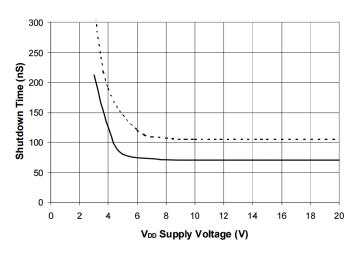


Figure 9A. Shutdown Time vs. Temperature





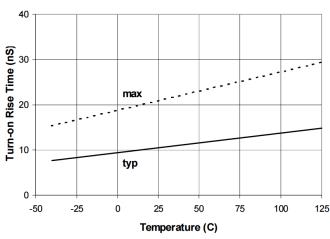
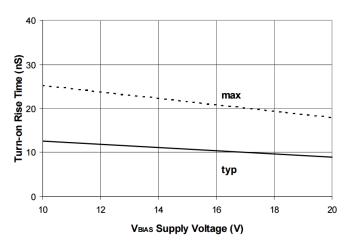


Figure 9C. Shutdown Time vs. V_{DD} Voltage

Figure 10A. Turn-on Rise Time vs. Temperature



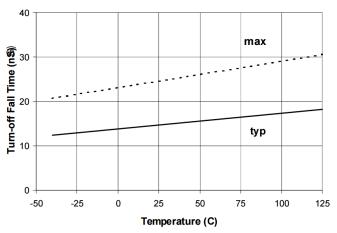


Figure 10B. Turn-on Rise Time vs. V_{BIAS} ($V_{CC}=V_{BS}=V_{DD}$) Voltage

Figure 11A. Turn-off Fall Time vs. Temperature



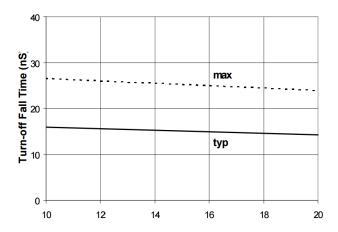


Figure 11B. Turn-Off Fall Time vs. V_{BIAS} ($V_{CC}=V_{BS}=V_{DD}$) Voltage

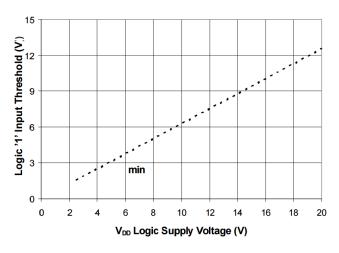


Figure 12B. Logic "1" Input Threshold vs. V_{DD} Voltage

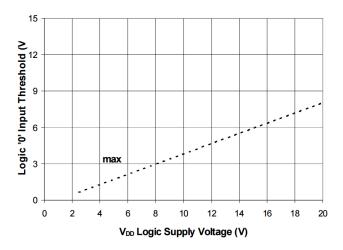


Figure 13B. Logic "0" Input Threshold vs. VDD Voltage

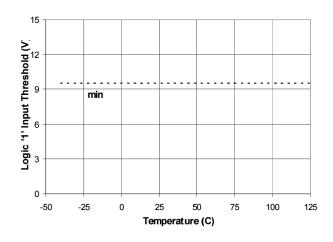


Figure 12A. Logic "1" Input Threshold vs. **Temperature**

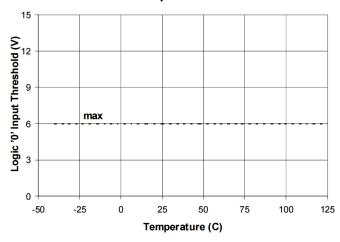


Figure 13A. Logic "0" Input Threshold vs. Temperature

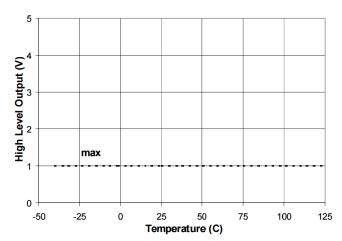
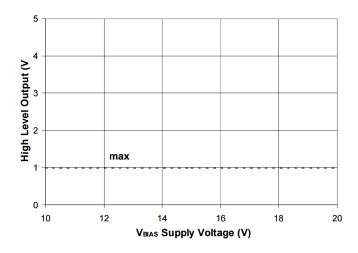


Figure 14A. High Level Output vs. Temperature





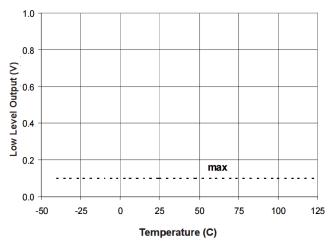
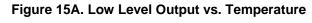
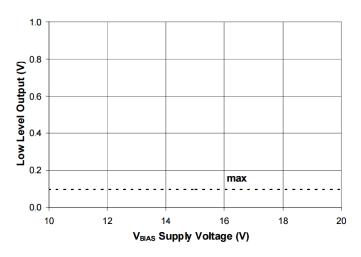


Figure 14B. High Level Output vs. V_{BIAS} Voltage





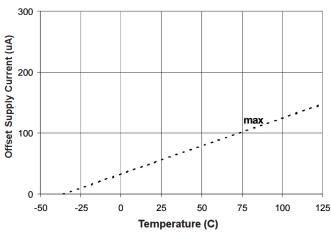
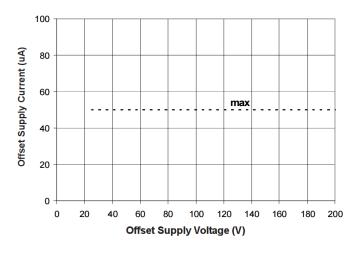


Figure 15B. Low Level Output vs. V_{BIAS} Voltage

Figure 16A. Offset Supply Current vs. Temperature



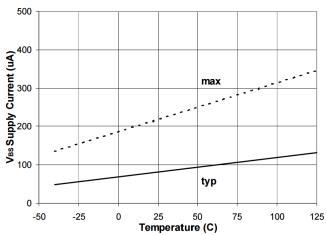
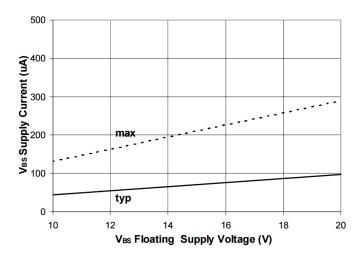


Figure 16B. Offset Supply Current vs. Offset Voltage

Figure 17A. V_{BS} Supply Current vs. Temperature





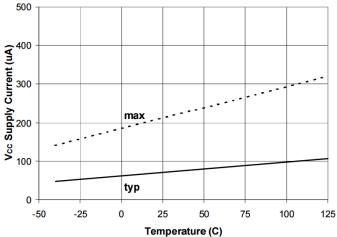
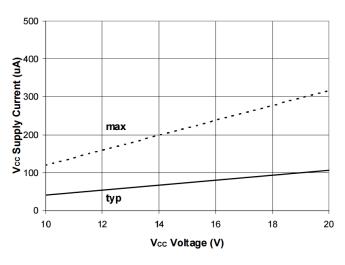


Figure 17B. V_{BS} Supply Current vs. V_{BS} Voltage

Figure 18A. V_{CC} Supply Current vs. Temperature



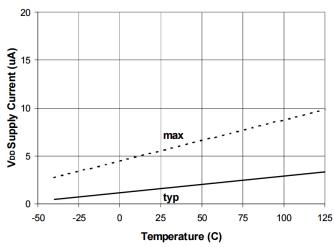
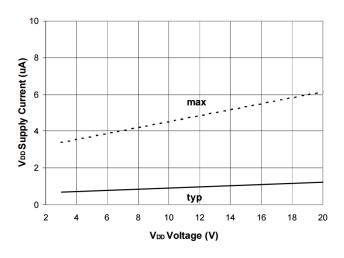


Figure 18B. V_{CC} Supply Current vs. V_{CC} Voltage

Figure 19A. V_{DD} Supply Current vs. Temperature



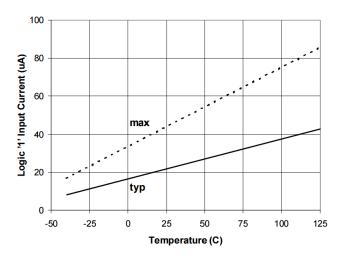
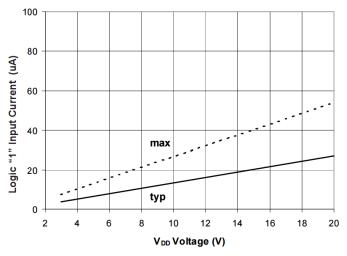


Figure 19B. V_{DD} Supply Current vs. V_{DD} Voltage

Figure 20A. Logic "1"Input Current vs. Temperature





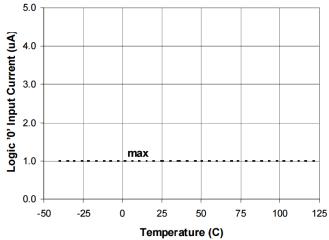
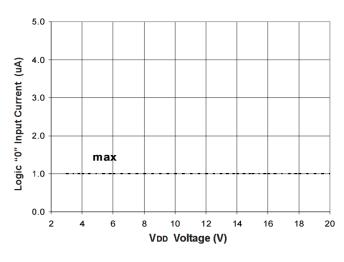


Figure 20B. Logic "1" Input Current vs. V_{DD} Voltage

Figure 21A. Logic "0" Input Current vs. Temperature



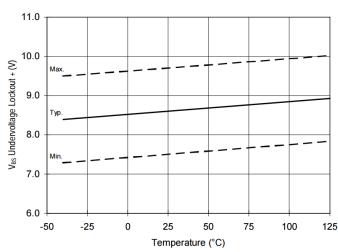
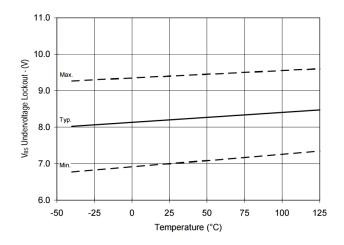


Figure 21B. Logic "0" Input Current vs. V_{DD} Voltage

Figure 22. V_{BS} Undervoltage (+) vs. Temperature



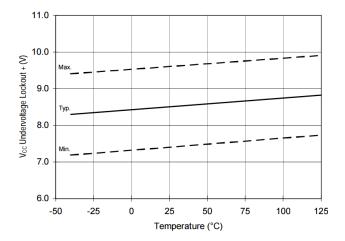
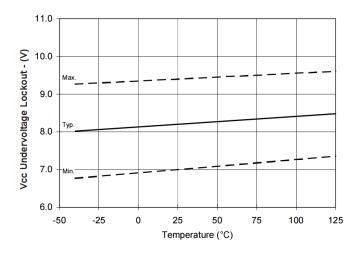


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

Figure 24. V_{CC} Undervoltage (+) vs. Temperature





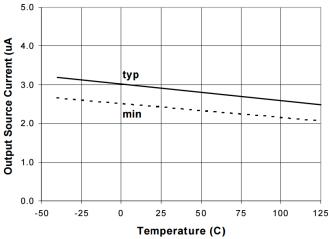


Figure 25. V_{CC} Undervoltage (-) vs. Temperature

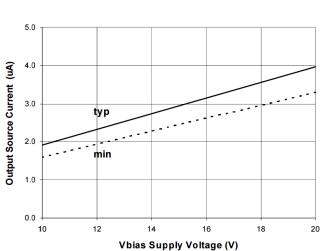


Figure 26A. Output Source Current vs. Temperature

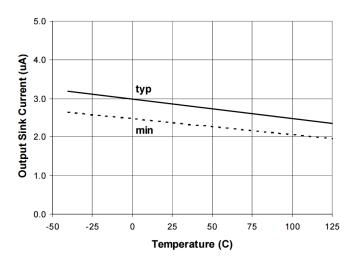


Figure 26B. Output Source Current vs. V_{BIAS} Voltage

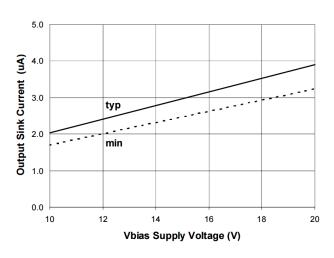


Figure 27B. Output Sink Current vs. V_{BIAS} Voltage

Figure 27A. Output Sink Current vs. Temperature

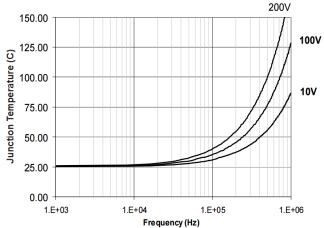


Figure 28. IR2010 Tj vs. Frequency R_{GATE} = 10 Ω , V_{CC} = 15V with IRFPE50



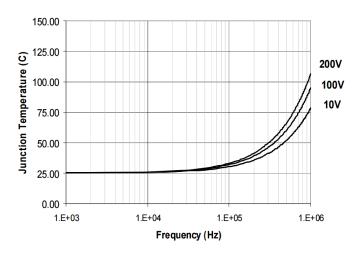


Figure 29. IR2010 Tj vs. Frequency $R_{GATE} = 16\Omega$, $V_{CC} = 15V$ with IRFBC40

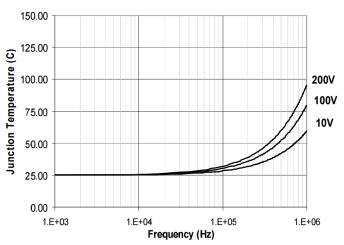


Figure 31. IR2010 Tj vs. Frequency $R_{GATE} = 33\Omega$, $V_{CC} = 15V$ with IRFBC20

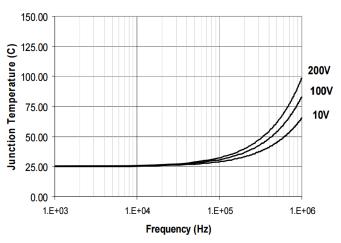


Figure 30. IR2010 Tj vs. Frequency $R_{GATE} = 22\Omega$, $V_{CC} = 15V$ with IRFBC30

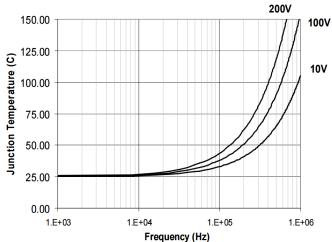


Figure 32. IR2010 Tj vs. Frequency $R_{GATE} = 10\Omega$, $V_{CC} = 15V$ with IRFBE50



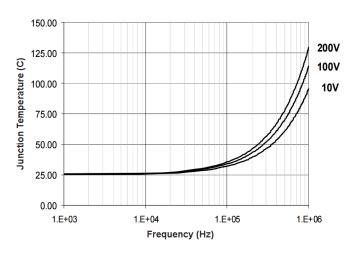


Figure 33. IR2010S Tj vs. Frequency $R_{GATE} = 16\Omega$, $V_{CC} = 15V$ with IRFBC40

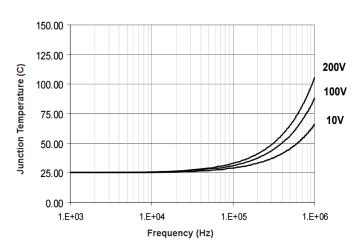


Figure 35. IR2010S Tj vs. Frequency $R_{GATE} = 33\Omega$, $V_{CC} = 15V$ with IRFBC20

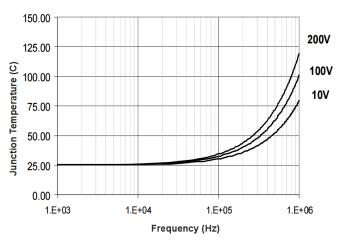
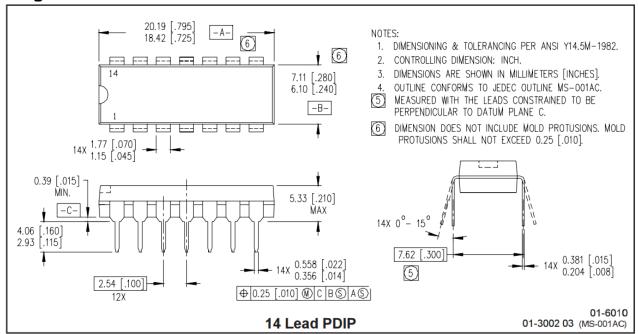
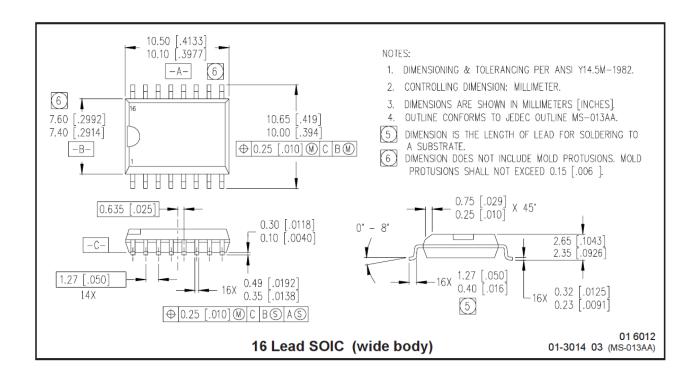


Figure 34. IR2010S Tj vs. Frequency $R_{GATE} = 22\Omega$, $V_{CC} = 15V$ with IRFBC30



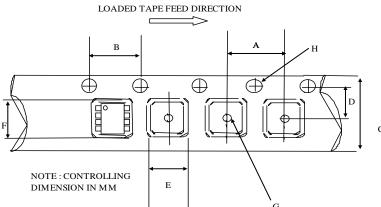
Package Details





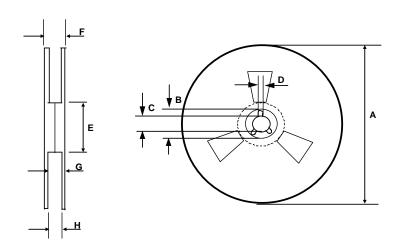


Tape and Reel Details



CARRIER TAPE DIMENSION FOR 16SOICW

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	Me	etric	Imperial		
Code	Min	Max	Min	Max	
Α	11.90	12.10	0.468	0.476	
В	3.90	4.10	0.153	0.161	
С	15.70	16.30	0.618	0.641	
D	7.40	7.60	0.291	0.299	
E	10.80	11.00	0.425	0.433	
F	10.60	10.80	0.417	0.425	
G	1.50	n/a	0.059	n/a	
Н	1.50	1.60	0.059	0.062	

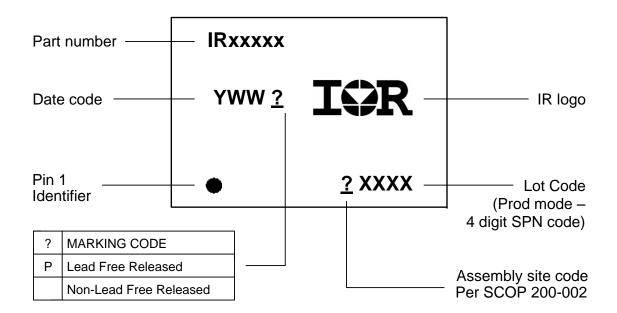


REEL DIMENSIONS FOR 16SOICW

	Me	etric	lmp	erial
Code	Min	Max	Min	Max
Α	329.60	330.25	12.976	13.001
В	20.95	21.45	0.824	0.844
С	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
Н	16.40	18.40	0.645	0.724



Part Marking Information





Qualification Information[†]

		Industrial ^{††} (per JEDEC JESD 47)			
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.			
Moisture Sensitivity Level	16-Lead SOIC WB	MSL3 ^{†††} (per IPC/JEDEC J-STD-020)			
RoHS Compliant		Yes			

- Qualification standards can be found at International Rectifier's web site http://www.irf.com/
- Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.
- ††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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> For technical support, please contact IR's Technical Assistance Center http://www.irf.com/technical-info/

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