

CoolMOS™ Power Transistor

Features

- New revolutionary high voltage technology
- Extreme dv/dt rated
- High peak current capability
- Fully qualified according to JEDEC¹⁾ for industrial applications
- Pb-free lead plating; RoHS compliant; Halogen free mold compound
- Ultra low gate charge
- Ultra low effective capacitances

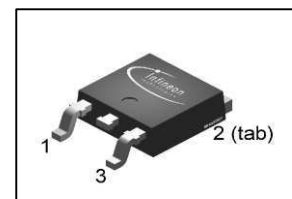
CoolMOS™ 800V designed for:

- Industrial application with high DC bulk voltage
- Switching Application (i.e. active clamp forward)

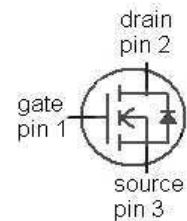
Product Summary

V_{DS}	800	V
$R_{DS(on)max}$ @ $T_j = 25^\circ\text{C}$	2.7	Ω
$Q_{g,typ}$	12	nC

PG-TO252-3



Type	Package	Marking
SPD02N80C3	PG-TO252-3	02N80C3



Maximum ratings, at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25^\circ\text{C}$	2	A
		$T_C=100^\circ\text{C}$	1.2	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25^\circ\text{C}$	6	
Avalanche energy, single pulse	E_{AS}	$I_D=1\text{ A}, V_{DD}=50\text{ V}$	90	mJ
Avalanche energy, repetitive t_{AR} ^{2),3)}	E_{AR}	$I_D=2\text{ A}, V_{DD}=50\text{ V}$	0.05	
Avalanche current, repetitive t_{AR} ^{2),3)}	I_{AR}		2	A
MOSFET dv/dt ruggedness	dv/dt	$V_{DS}=0\dots640\text{ V}$	50	V/ns
Gate source voltage	V_{GS}	static	± 20	V
		AC ($f>1\text{ Hz}$)	± 30	
Power dissipation	P_{tot}	$T_C=25^\circ\text{C}$	42	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	$^\circ\text{C}$

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous diode forward current	I_S	$T_C=25\text{ °C}$	2	A
Diode pulse current ²⁾	$I_{S,pulse}$		6	
Reverse diode dv/dt ⁴⁾	dv/dt		4	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	3	K/W
Thermal resistance, junction - ambient	R_{thJA}	SMD version, device on PCB, minimal footprint	-	-	62	
		SMD version, device on PCB, 6 cm ² cooling area ⁵⁾	-	35	-	
Soldering temperature, reflow soldering	T_{sold}	reflow MSL1	-	-	260	°C

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$	800	-	-	V
Avalanche breakdown voltage	$V_{(BR)DS}$	$V_{GS}=0\text{ V}$, $I_D=2\text{ A}$	-	870	-	
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=0.12\text{ mA}$	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=800\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	-	5	μA
		$V_{DS}=800\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$	-	25	-	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}$, $I_D=1.2\text{ A}$, $T_j=25\text{ °C}$	-	2.4	2.7	Ω
		$V_{GS}=10\text{ V}$, $I_D=1.2\text{ A}$, $T_j=150\text{ °C}$	-	6.5	-	
Gate resistance	R_G	$f=1\text{ MHz}$, open drain	-	1.2	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=100\text{ V},$ $f=1\text{ MHz}$	-	290	-	pF
Output capacitance	C_{oss}		-	13	-	
Effective output capacitance, energy related ⁶⁾	$C_{o(er)}$	$V_{GS}=0\text{ V}, V_{DS}=0\text{ V}$ to 480 V	-	11	-	
Effective output capacitance, time related ⁷⁾	$C_{o(tr)}$		-	26	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=400\text{ V},$ $V_{GS}=0/10\text{ V}, I_D=2\text{ A},$ $R_G=47\text{ }\Omega, T_j=25\text{ }^\circ\text{C}$	-	25	-	ns
Rise time	t_r		-	15	-	
Turn-off delay time	$t_{d(off)}$		-	72	-	
Fall time	t_f		-	18	-	

Gate Charge Characteristics

Gate to source charge	Q_{gs}	$V_{DD}=640\text{ V}, I_D=2\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	1.5	-	nC
Gate to drain charge	Q_{gd}		-	6	-	
Gate charge total	Q_g		-	12	16	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V

Reverse Diode

Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=I_S=2\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	1	1.2	V
Reverse recovery time	t_{rr}	$V_R=400\text{ V}, I_F=I_S=2\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	520	-	ns
Reverse recovery charge	Q_{rr}		-	2	-	μC
Peak reverse recovery current	I_{rrm}		-	6	-	A

¹⁾ J-STD20 and JESD22

²⁾ Pulse width t_p limited by $T_{j,max}$
³⁾ Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR} \cdot f$.

⁴⁾ $I_{SD}=I_D, di/dt=400\text{ A}/\mu\text{s}, V_{DClink}=400\text{ V}, V_{peak}<V_{(BR)DSS}, T_j<T_{j,max}$, identical low side and high side switch

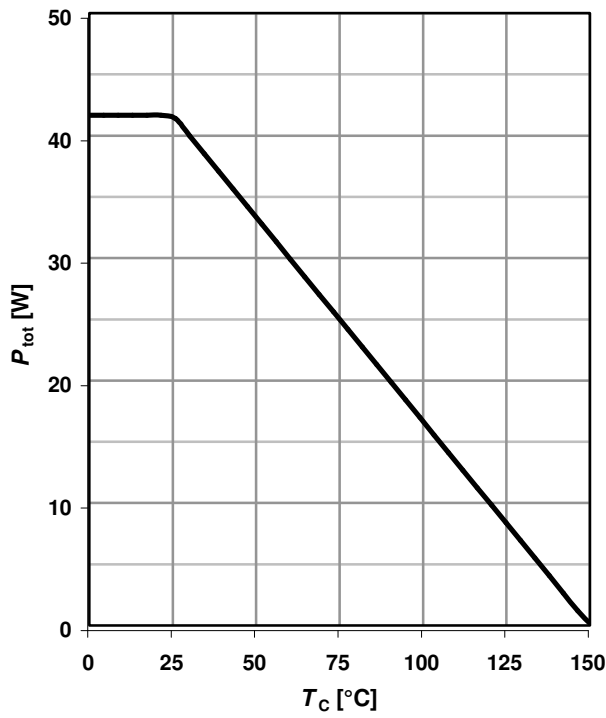
⁵⁾ Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air

⁶⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁷⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

1 Power dissipation

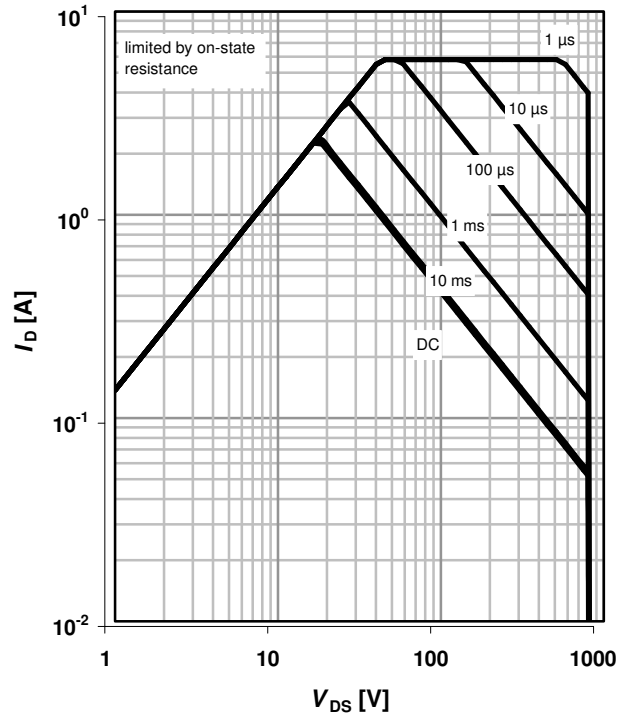
$P_{tot}=f(T_C)$



2 Safe operating area

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

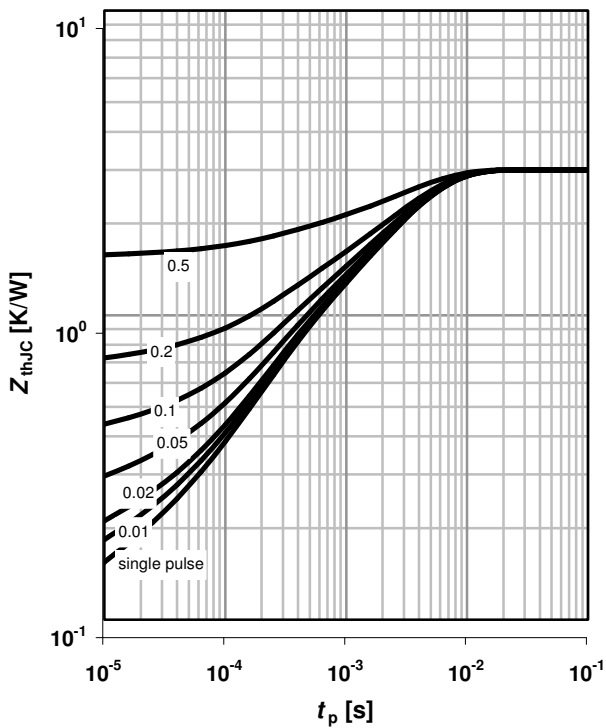
parameter: t_p



3 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

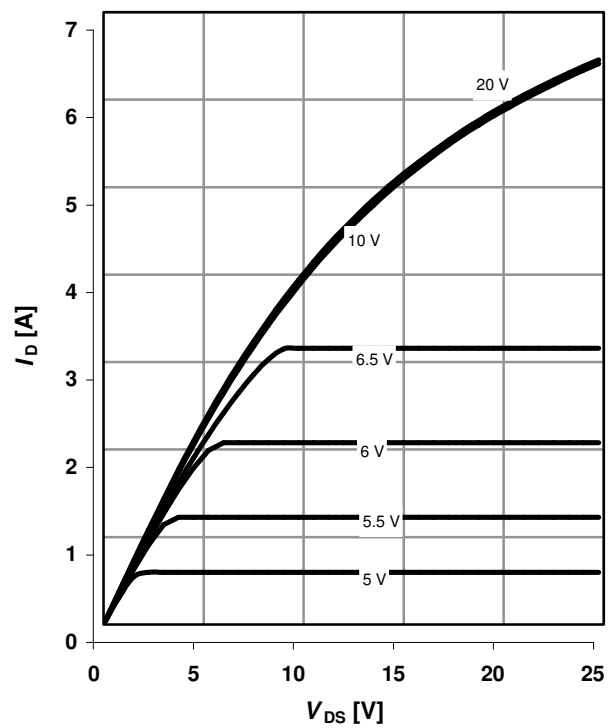
parameter: $D=t_p/T$



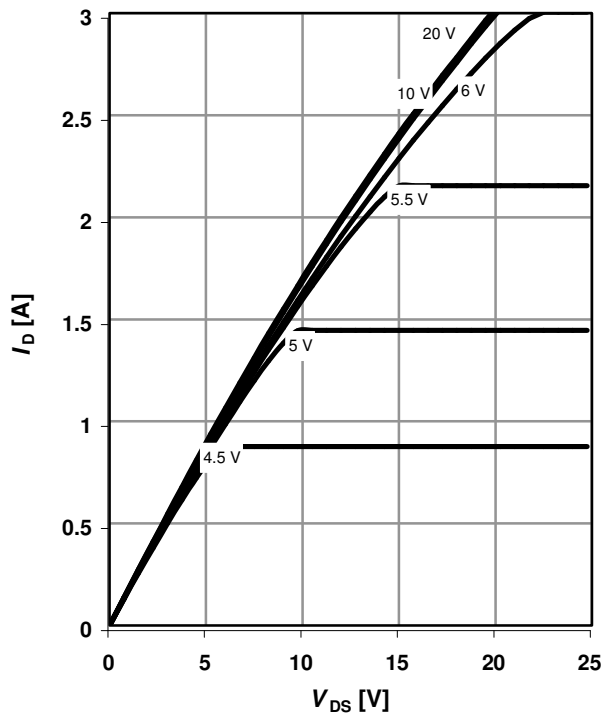
4 Typ. output characteristics

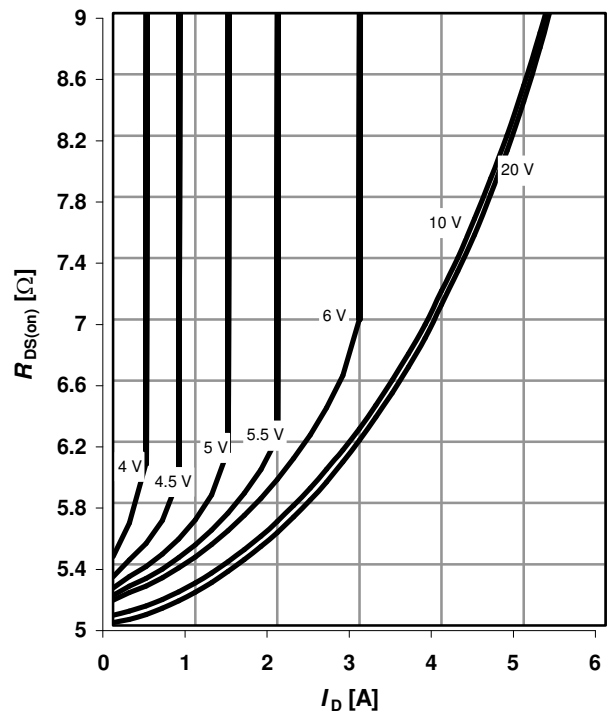
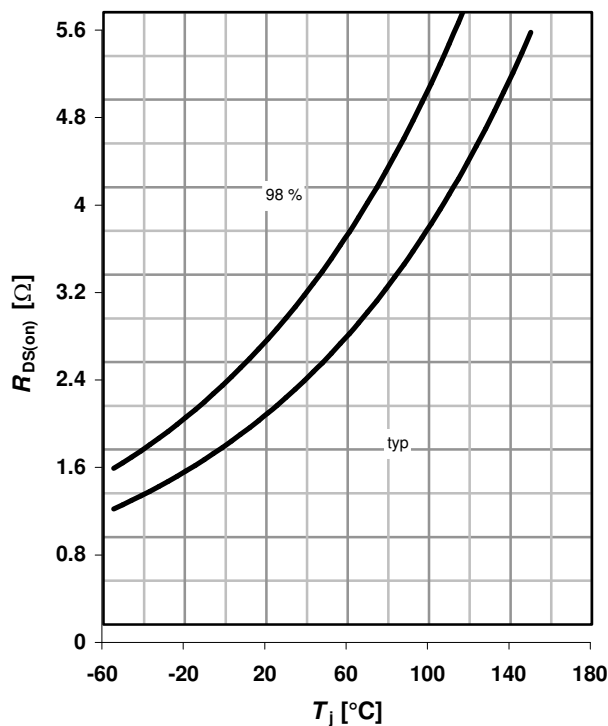
$I_D=f(V_{DS}); T_j=25\text{ °C}; t_p=10\text{ μs}$

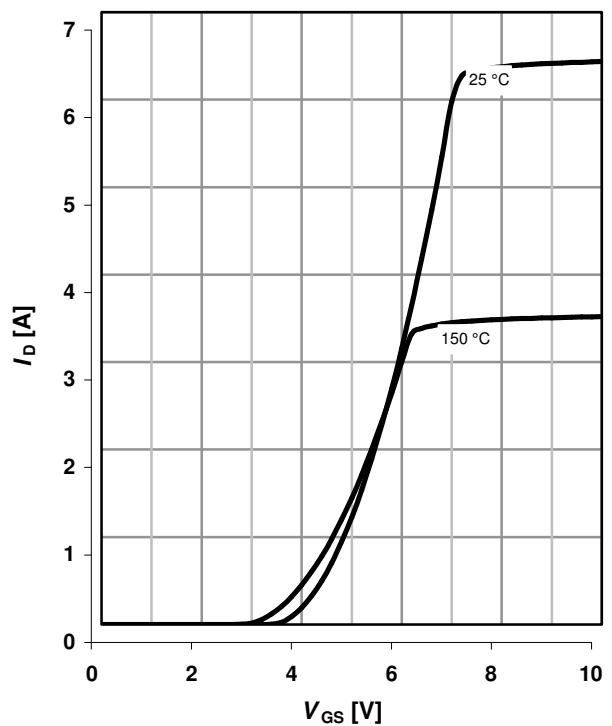
parameter: V_{GS}



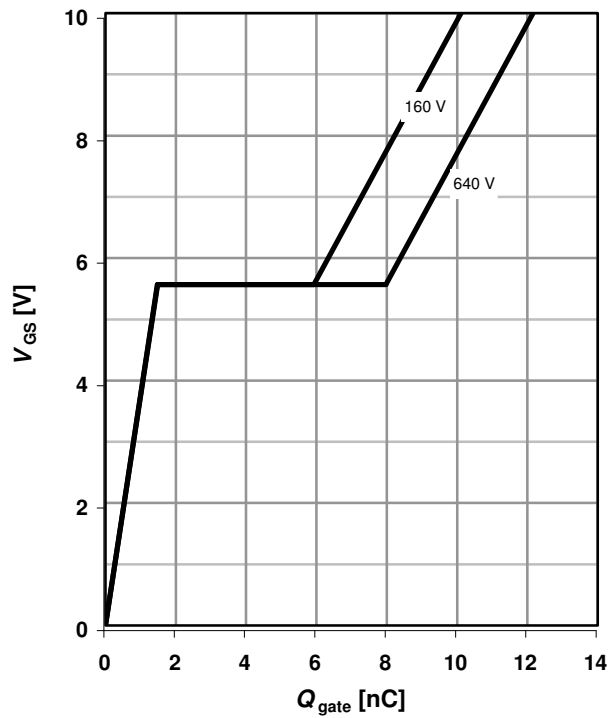
5 Typ. output characteristics
 $I_D = f(V_{DS}); T_j = 150\text{ °C}; t_p = 10\text{ }\mu\text{s}$

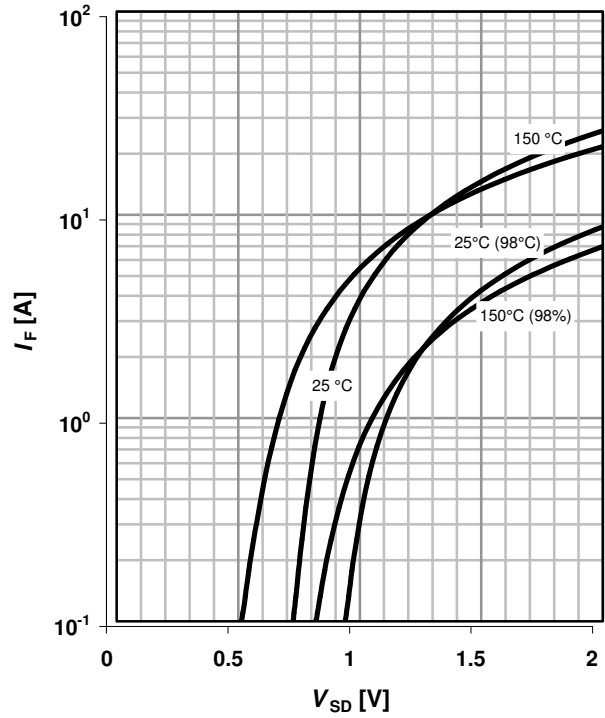
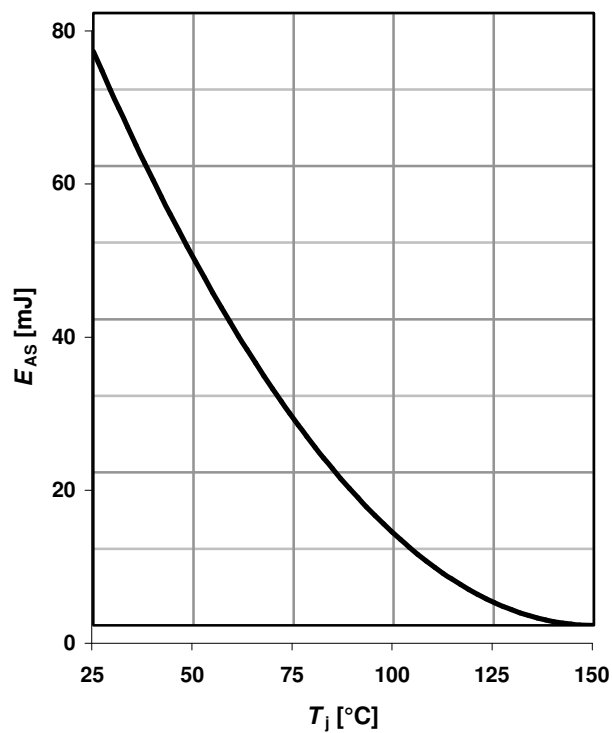
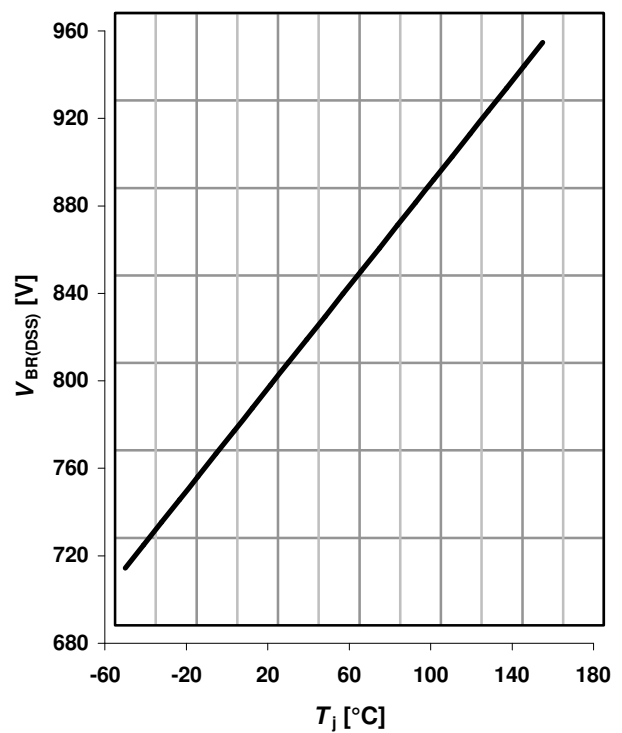
 parameter: V_{GS}

6 Typ. drain-source on-state resistance
 $R_{DS(on)} = f(I_D); T_j = 150\text{ °C}$

 parameter: V_{GS}

7 Drain-source on-state resistance
 $R_{DS(on)} = f(T_j); I_D = 1.2\text{ A}; V_{GS} = 10\text{ V}$

8 Typ. transfer characteristics
 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; t_p = 10\text{ }\mu\text{s}$

 parameter: T_j


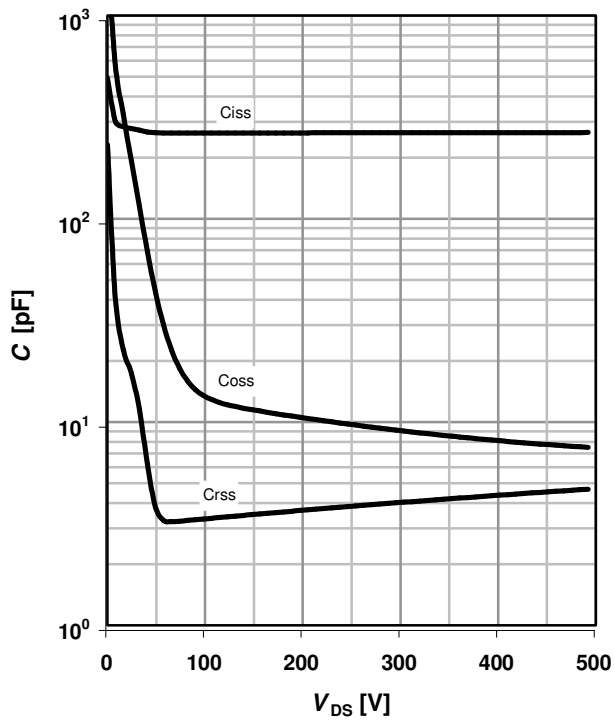
9 Typ. gate charge
 $V_{GS}=f(Q_{gate}); I_D=2\text{ A pulsed}$

 parameter: V_{DD}

10 Forward characteristics of reverse diode
 $I_F=f(V_{SD}); t_p=10\ \mu\text{s}$

 parameter: T_j

11 Avalanche energy
 $E_{AS}=f(T_j); I_D=1\text{ A}; V_{DD}=50\text{ V}$

12 Drain-source breakdown voltage
 $V_{BR(DSS)}=f(T_j); I_D=0.25\text{ mA}$


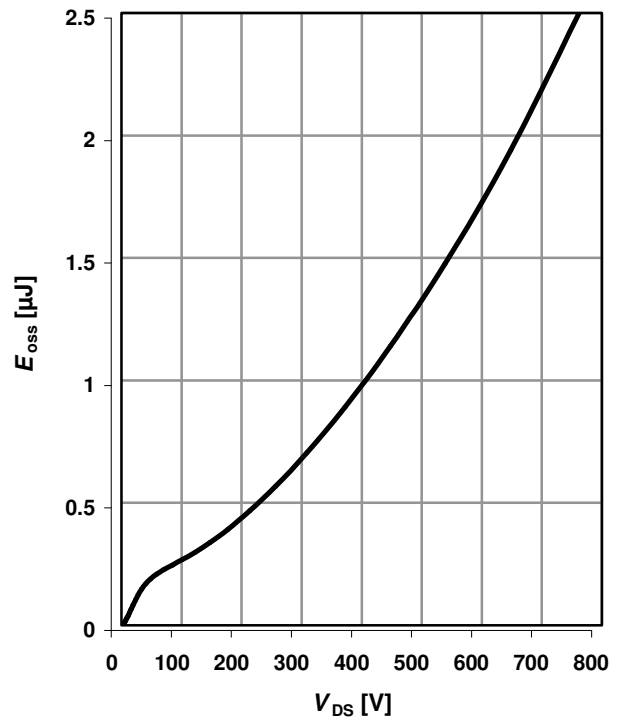
13 Typ. capacitances

$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

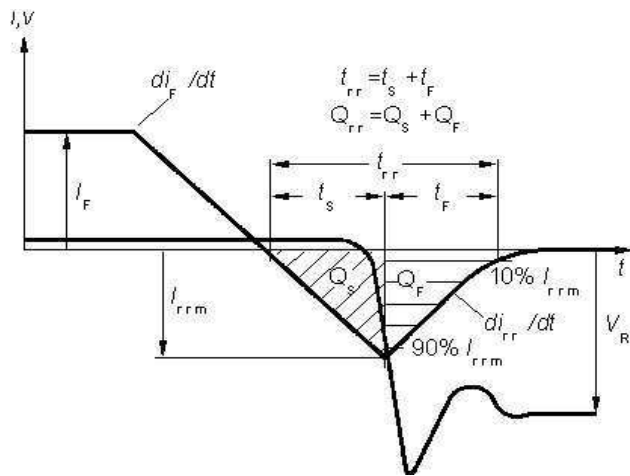


14 Typ. Coss stored energy

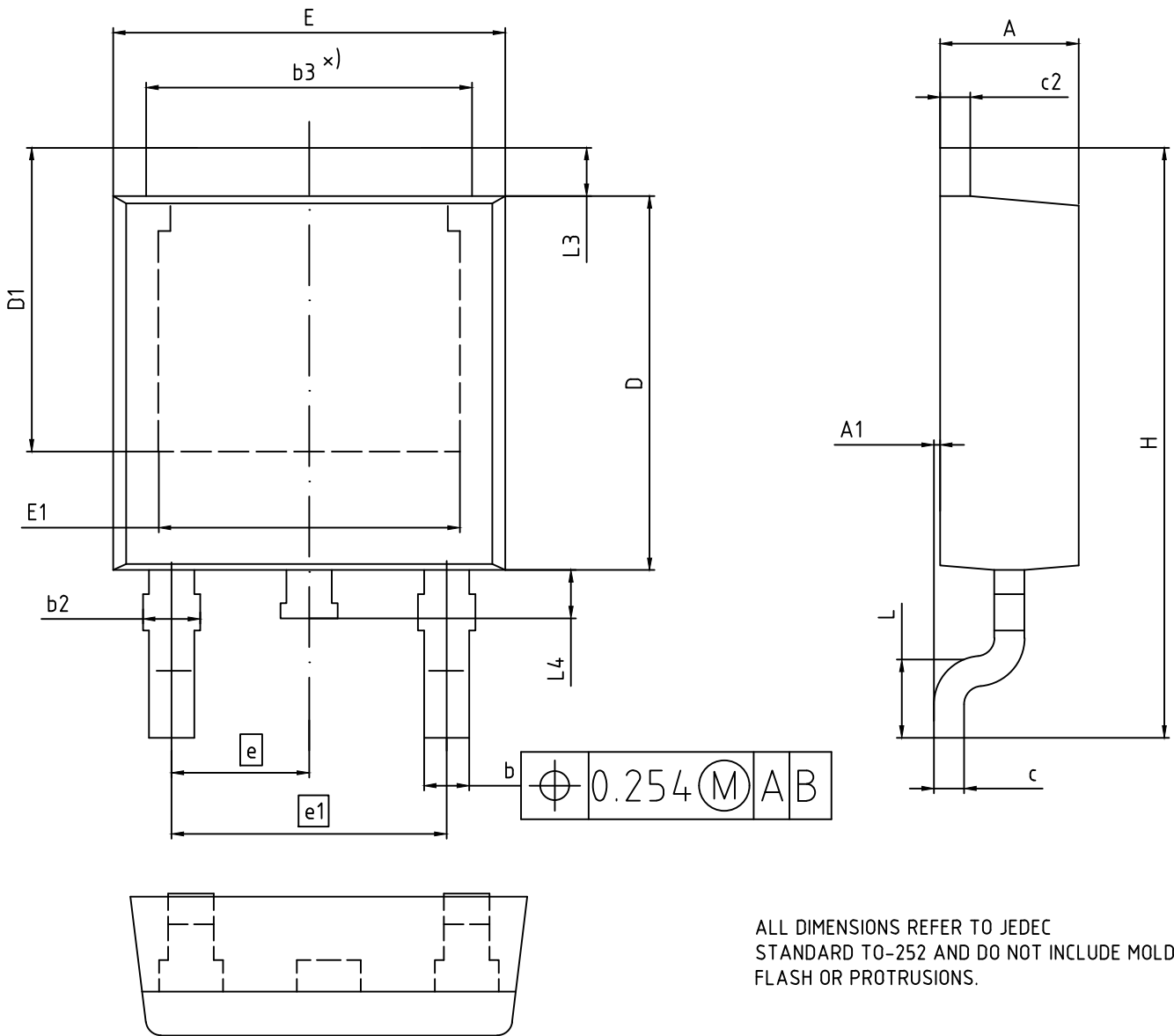
$E_{oss}=f(V_{DS})$



Definition of diode switching characteristics



PG-TO252-3-1: Outline , PG-TO-252-3-11 (D-PAK), PG-TO-252-3-21 (D-PAK)



ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b2	0.65	1.15
b3	4.95	5.50
c	0.46	0.61
c2	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L3	0.89	1.27
L4	0.51	1.02

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Revision History

SPD02N80C3

Revision: 2020-05-26, Rev. 2.94

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.93	2016-04-19	Non-halogen free version discontinued (creation:2016-04-13)
2.94	2020-05-26	Update package outline

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