

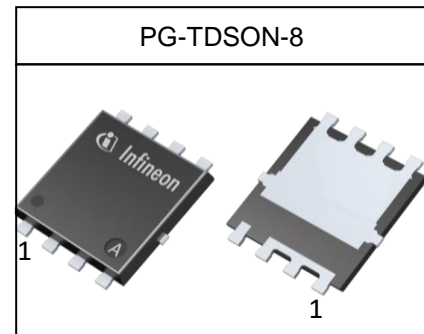
OptiMOS™-5 Power-Transistor

Features

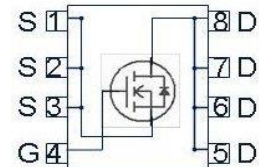
- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal level
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- Green product (RoHS compliant)
- 100% Avalanche tested
- Feasible for automatic optical inspection (AOI)

Product Summary

V_{DS}	100	V
$R_{DS(on)}$	6.2	mΩ
I_D	90	A



Type	Package	Marking
IAUC90N10S5N062	PG-TDSON-8	5N10N062


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}, V_{GS}=10\text{V}$	90	A
		$T_C=100\text{ °C}, V_{GS}=10\text{V}$	66	
Pulsed drain current ¹⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	360	
Avalanche energy, single pulse ¹⁾	E_{AS}	$I_D=45\text{A}$	112	mJ
Avalanche current, single pulse	I_{AS}	-	47	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}, T_J=175\text{ °C}$	115	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics¹⁾						
Thermal resistance, junction - case	R_{thJC}	-	-	-	1.3	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	6 cm ² cooling area ²⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=59\mu A$	2.2	3.0	3.8	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V, T_j=25\text{ °C}$	-	-	1	μA
		$V_{DS}=100V, V_{GS}=0V, T_j=125\text{ °C}^{1)}$	-	-	20	
Gate-source leakage current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=6V, I_D=23A$	-	6.5	7.8	m Ω
		$V_{GS}=10V, I_D=45A$	-	5.2	6.2	
Gate resistance ¹⁾	R_G		-	1	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics¹⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=50\text{ V},$ $f=1\text{ MHz}$	-	2519	3275	pF
Output capacitance	C_{oss}		-	403	524	
Reverse transfer capacitance	C_{rss}		-	20.5	31	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V},$ $I_D=90\text{ A}, R_G=3.5\Omega$	-	6	-	ns
Rise time	t_r		-	2	-	
Turn-off delay time	$t_{d(off)}$		-	10	-	
Fall time	t_f		-	8	-	

Gate Charge characteristics¹⁾

Gate to source charge	Q_{gs}	$V_{DD}=50\text{ V}, I_D=45\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	12	16	nC
Gate to drain charge	Q_{gd}		-	7.6	11.4	
Gate charge total	Q_g		-	36	48	
Gate plateau voltage	$V_{plateau}$		-	4.7	-	V

Reverse Diode

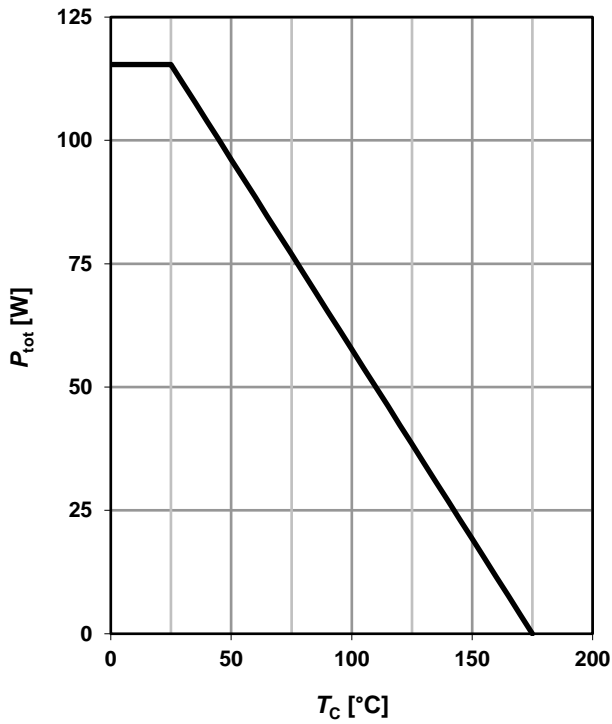
Diode continuous forward current ¹⁾	I_S	$T_C=25^\circ\text{C}$	-	-	90	A
Diode pulse current ¹⁾	$I_{S,pulse}$		-	-	360	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=45\text{ A},$ $T_j=25^\circ\text{C}$	-	0.9	1.1	V
Reverse recovery time ¹⁾	t_{rr}	$V_R=50\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	47	-	ns
Reverse recovery charge ¹⁾	Q_{rr}		-	61	-	nC

¹⁾ Defined by design. Not subject to production test.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

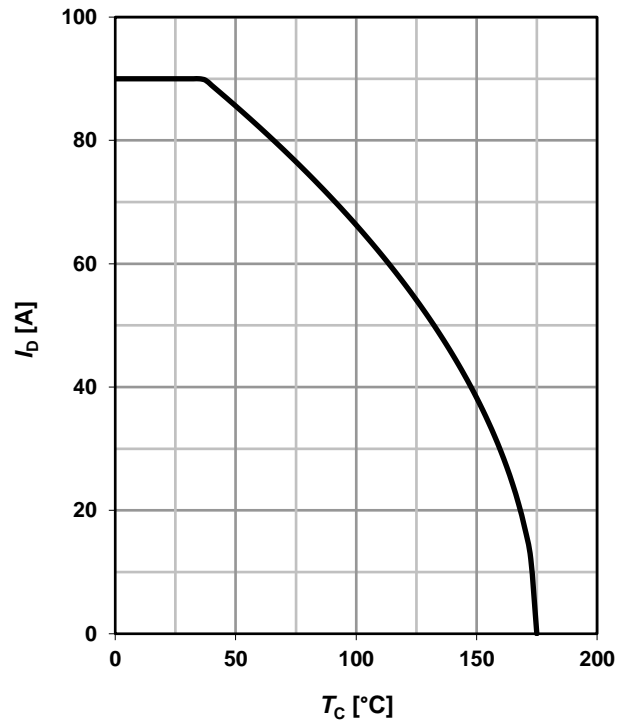
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \geq 6\text{ V}$



2 Drain current

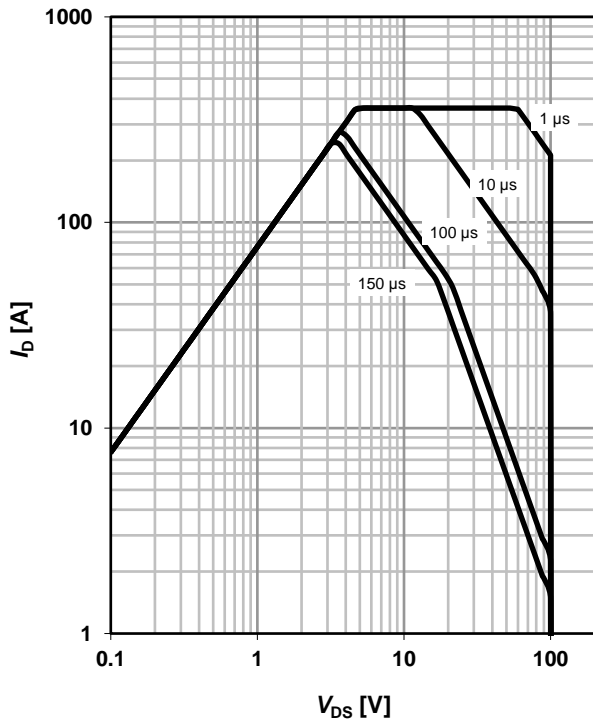
$I_D = f(T_C); V_{GS} \geq 6\text{ V}$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25\text{ °C}; D = 0$

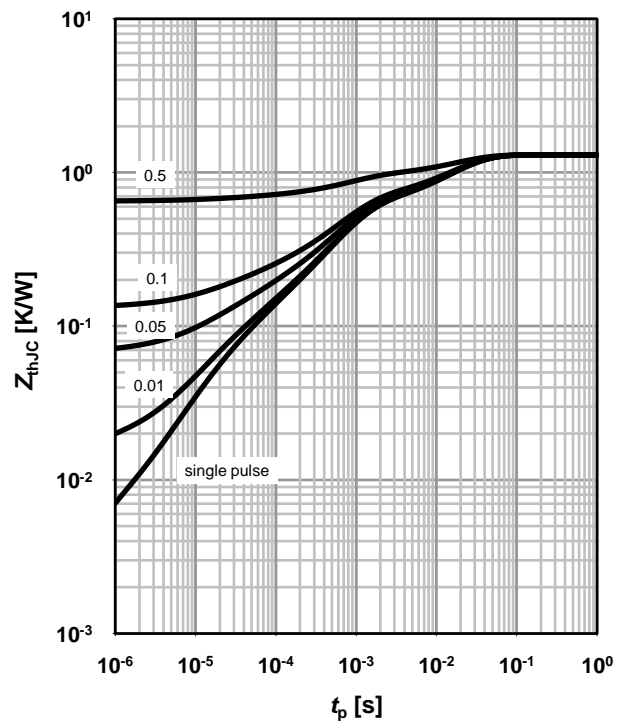
parameter: t_p



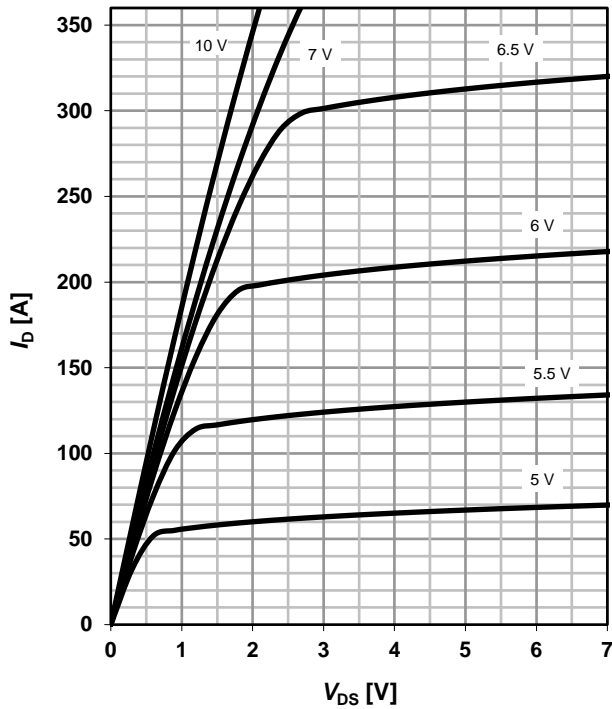
4 Max. transient thermal impedance

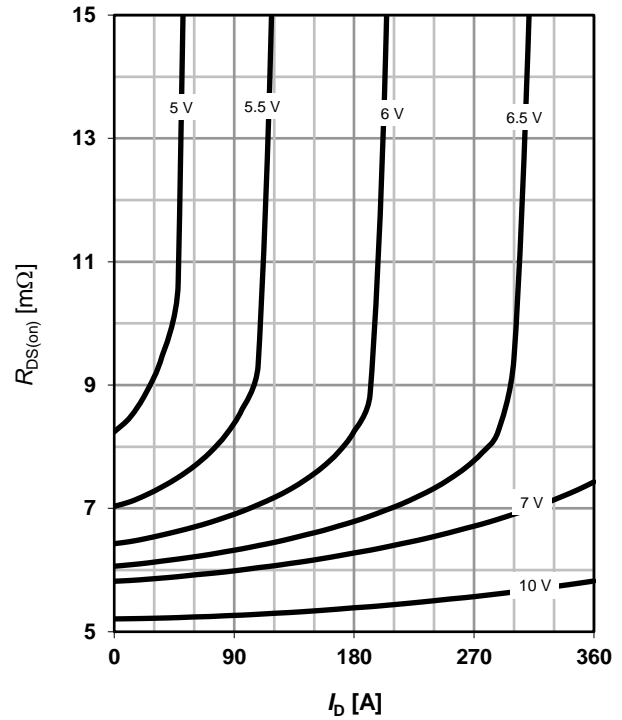
$Z_{thJC} = f(t_p)$

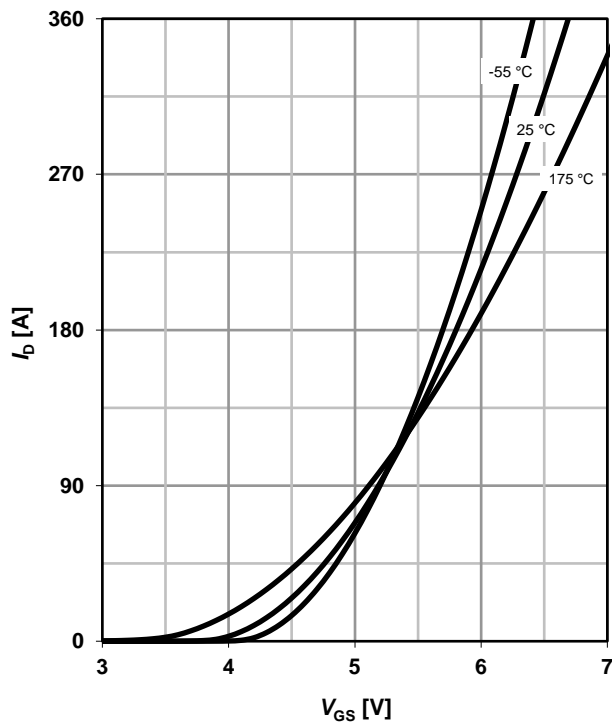
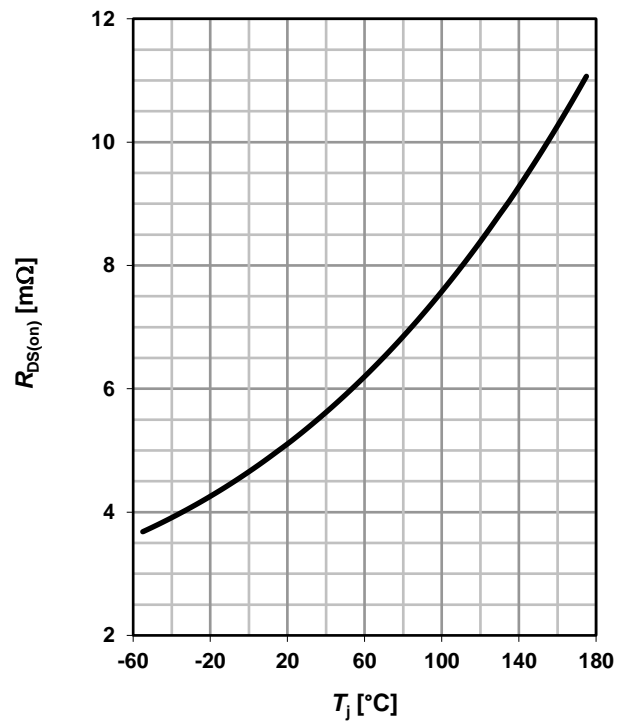
parameter: $D = t_p/T$



5 Typ. output characteristics
 $I_D = f(V_{DS}); T_j = 25\text{ °C}$

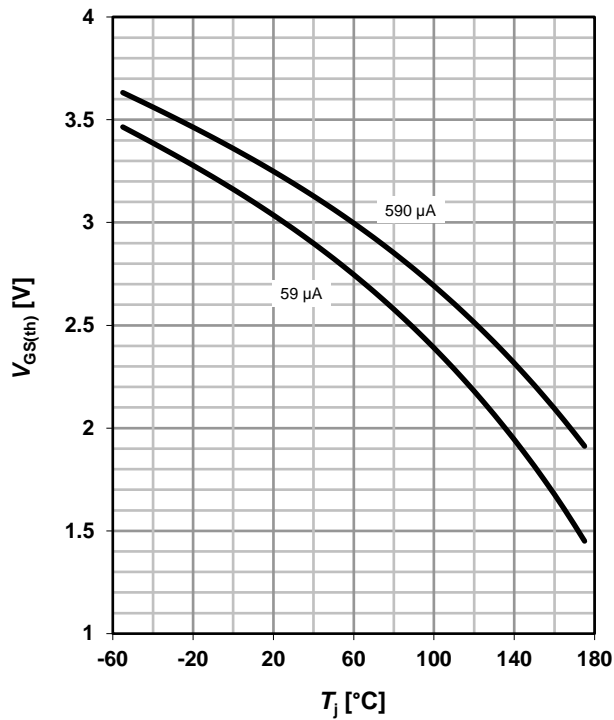
 parameter: V_{GS}

6 Typ. drain-source on-state resistance
 $R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

 parameter: V_{GS}

7 Typ. transfer characteristics
 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

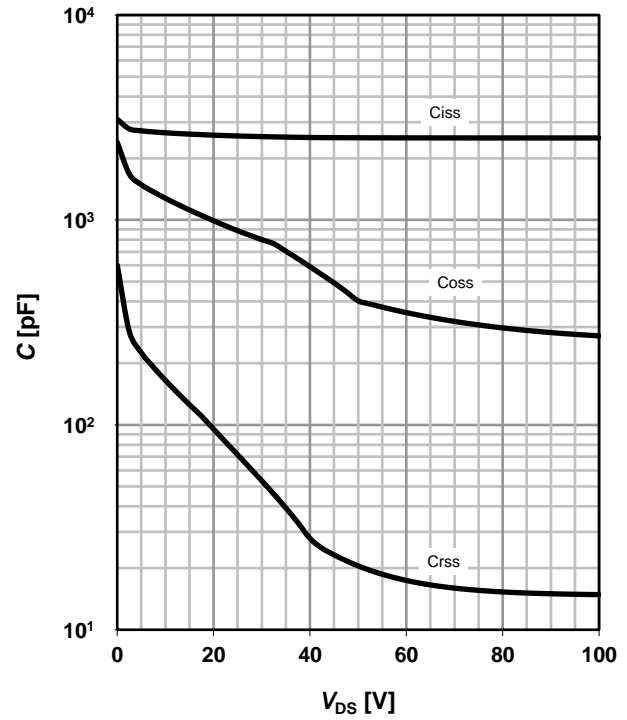
 parameter: T_j

8 Typ. drain-source on-state resistance
 $R_{DS(on)} = f(T_j); I_D = 45\text{ A}; V_{GS} = 10\text{ V}$


9 Typ. gate threshold voltage

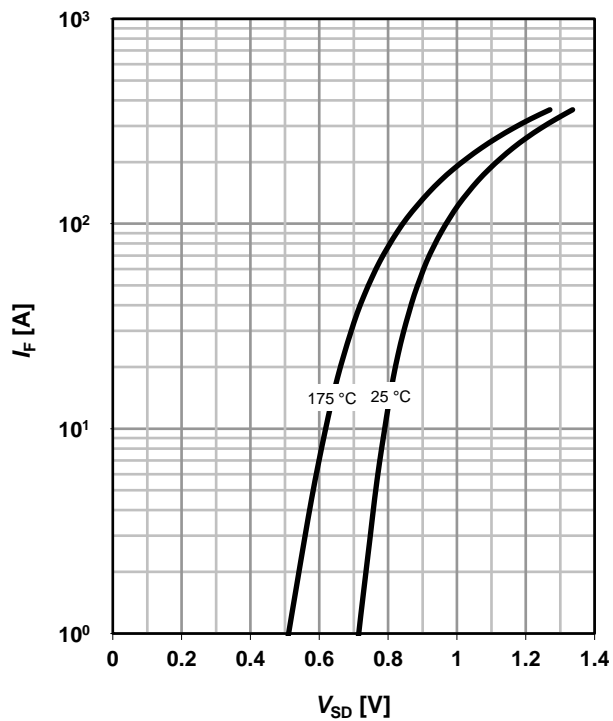
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

 parameter: I_D

10 Typ. capacitances

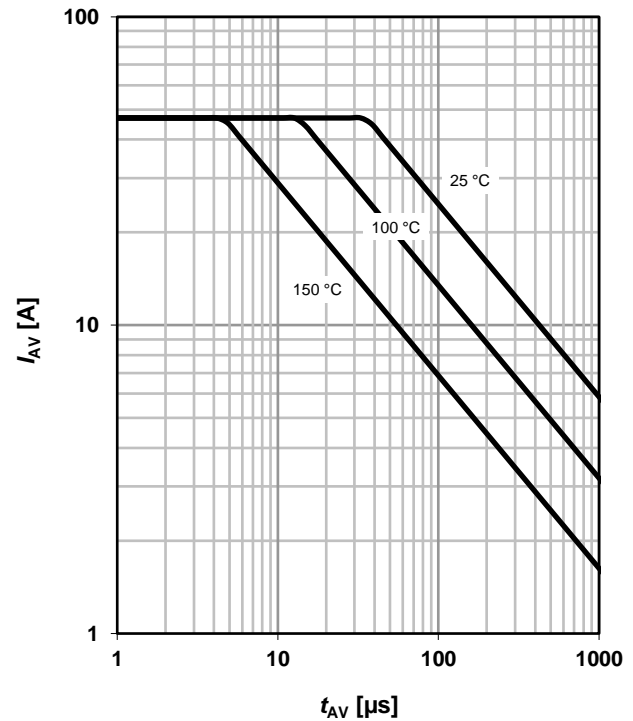
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$


11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

 parameter: T_j

12 Typ. avalanche characteristics

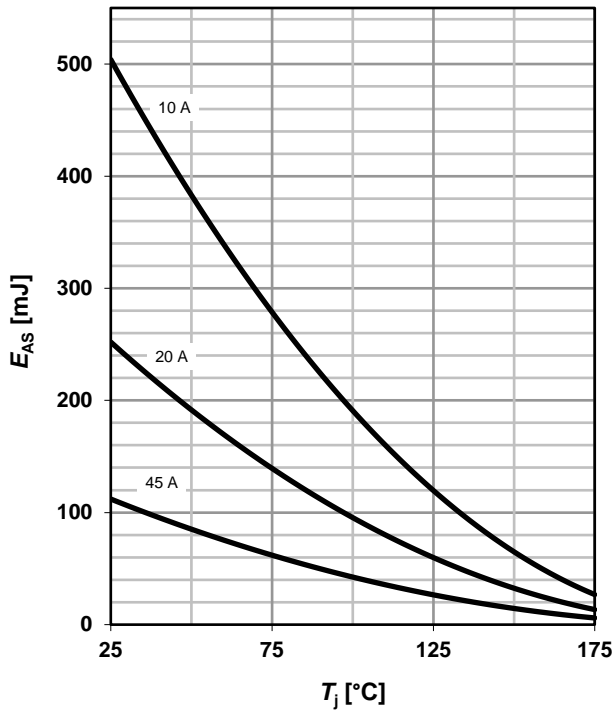
$$I_{AS} = f(t_{AV})$$

 parameter: $T_{j(start)}$


13 Typical avalanche energy

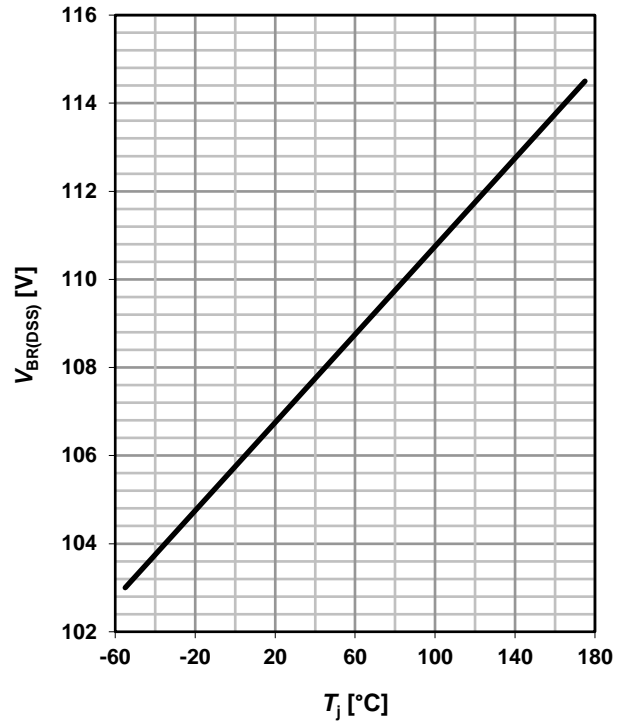
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

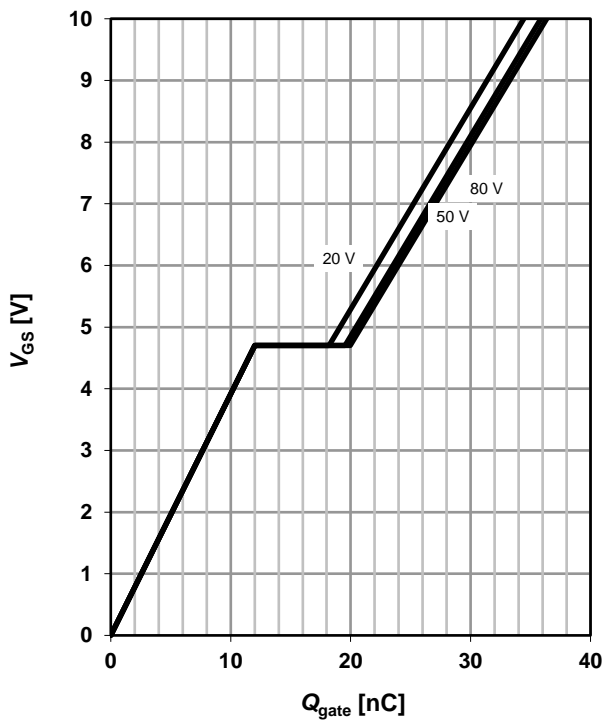
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



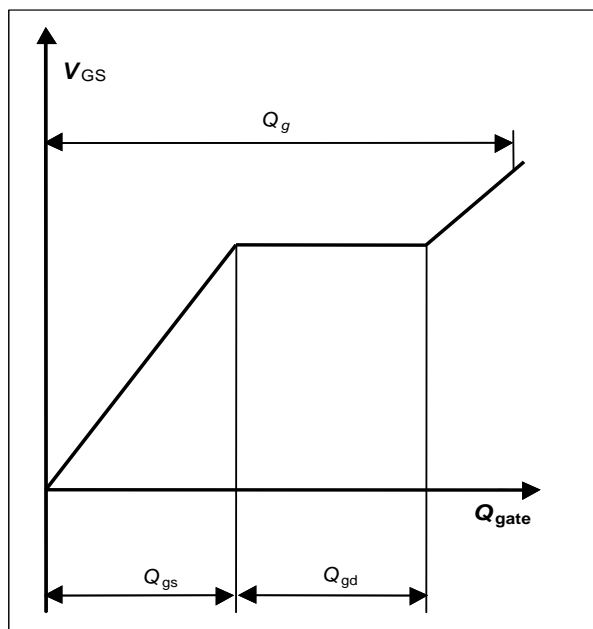
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 45 \text{ A pulsed}$$

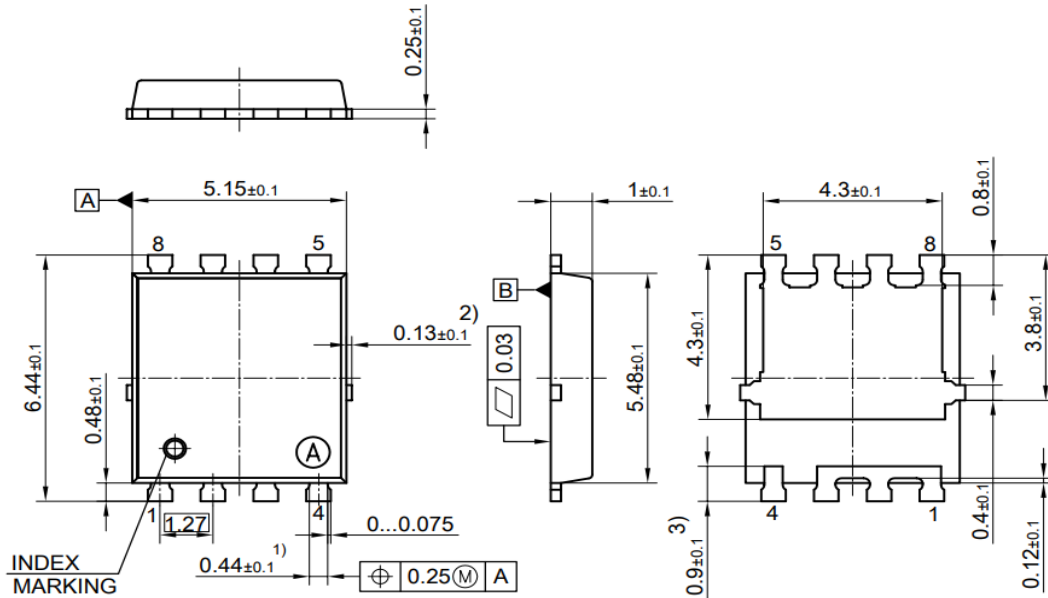
parameter: V_{DD}



16 Gate charge waveforms

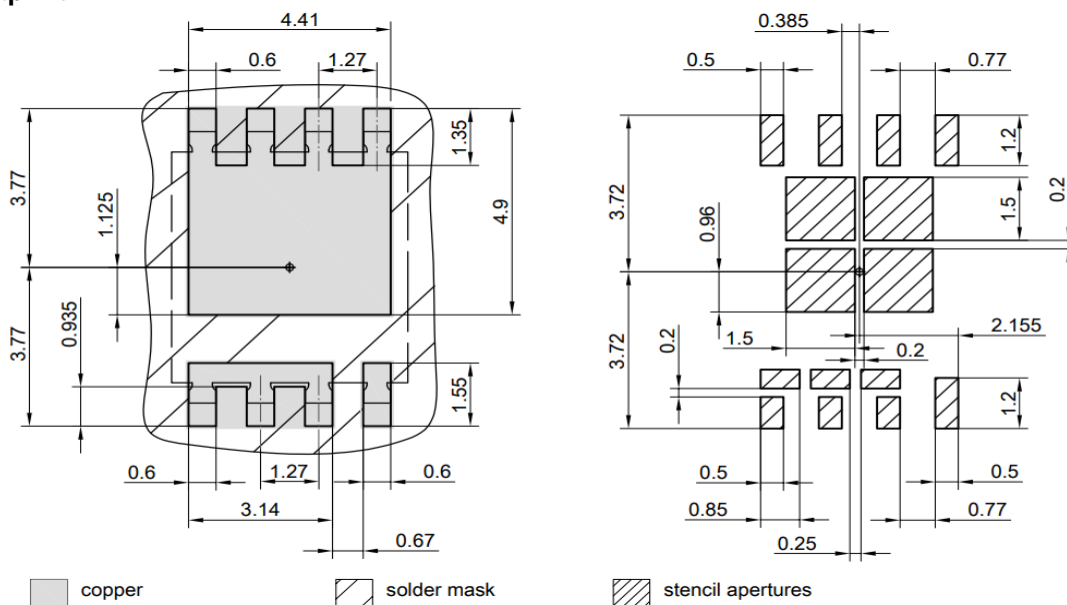


PG-TDSON-8: Outline



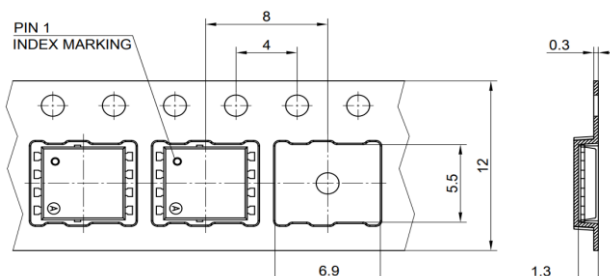
- 1) EXCLUDE MOLD FLASH
 - 2) REMOVAL ON MOLD GATE, INTRUSION 0.1MM AND PROTRUSION 0.1MM
 - 3) LEAD LENGTH UP TO ANTI FLASH LINE
 - 4) ALL METAL SURFACE ARE PLATED, EXCEPT AREA OF CUT
- ALL DIMENSIONS ARE IN UNITS MM
 THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 []

Footprint



Dimensions in mm

Packaging



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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.0	23.07.2019	Final Data Sheet