PD-97843

IRHNJ9A7130

100V, N-CHANNEL
R9 TECHNOLOGY

RADIATION HARDENED POWER MOSFET SURFACE MOUNT (SMD-0.5)

SMD-0.5

Product Summary

Part Number	Radiation Level	RDS(on)	I_D
IRHNJ9A7130	100 kRads (Si)	34mΩ	35A
IRHNJ9A3130	300 kRads (Si)	34mΩ	35A

Description

IR HiRel R9 technology provides superior power MOSFETs for space applications. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 90MeV/(mg/cm^2). Their combination of low RDS(on) and faster switching times reduces the power losses and increases power density in today's high speed switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features

- Low RDS(on)
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Ceramic package
- Light Weight
- Surface Mount
- ESD Rating: Class 2 per MIL-STD-750, Method 1020

Absolute Maximum Ratings — Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	35	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	22	
I_{DM}	Pulsed Drain Current ①	140	
P_D @T_C = 25°C	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	58	mJ
I_{AR}	Avalanche Current ①	35	A
E_{AR}	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	13	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Package Mounting Surface Temperature	300 (for 5s)	
	Weight	1.0 (Typical)	g

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.1	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	34	mΩ	V_{GS} = 12V, I_D = 22A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-8.9	—	mV/°C	
Gfs	Forward Transconductance	14	—	—	S	V_{DS} = 15V, I_D = 22A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	V_{DS} = 80V, V_{GS} = 0V
		—	—	10		V_{DS} = 80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	48	nC	I_D = 35A
Q_{GS}	Gate-to-Source Charge	—	—	25		V_{DS} = 50V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	9.0		V_{GS} = 12V
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	V_{DD} = 50V
tr	Rise Time	—	—	56		I_D = 35A
$t_{d(off)}$	Turn-Off Delay Time	—	—	38		R_G = 7.5Ω
t_f	Fall Time	—	—	27		V_{GS} = 12V
Ls +L_D	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	1800	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	440	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	3.3	—		f = 1.0MHz
R_G	Gate Resistance	—	1.0	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	35	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	140		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 35A, V_{GS} = 0V④
t_{rr}	Reverse Recovery Time	—	—	210	ns	T_J = 25°C, I_F = 35A, V_{DD} ≤ 25V
Q_{rr}	Reverse Recovery Charge	—	—	1.2	μC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.67	°C/W

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 100V, starting T_J = 25°C, L = 95μH, Peak I_L = 35A, V_{GS} = 20V

③ I_{SD} ≤ 35A, di/dt ≤ 980A/μs, V_{DD} ≤ 100V, T_J ≤ 150°C

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.** 80 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 300 kRads (Si) [1]		Units	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	——	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	——	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	——	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	——	1.0	µA	V_{DS} = 80V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	——	36	mΩ	V_{GS} = 12V, I_D = 22A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (SMD-0.5)	——	34	mΩ	V_{GS} = 12V, I_D = 22A
V_{SD}	Diode Forward Voltage	——	1.2	V	V_{GS} = 0V, I_D = 35A

1. Part numbers IRHNJ9A7130 and IRHNJ9A3130

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	VDS (V)			
			@ VGS = 0V	@ VGS = -1V	@ VGS = -5V	@ VGS = -10V
37 ± 5%	417 ± 7.5%	50 ± 7.5%	100	100	100	100
59.8 ± 5%	753 ± 7.5%	60 ± 7.5%	100	100	100	100
89.8 ± 5%	1515 ± 7.5%	82 ± 7.5%	100	100	——	——

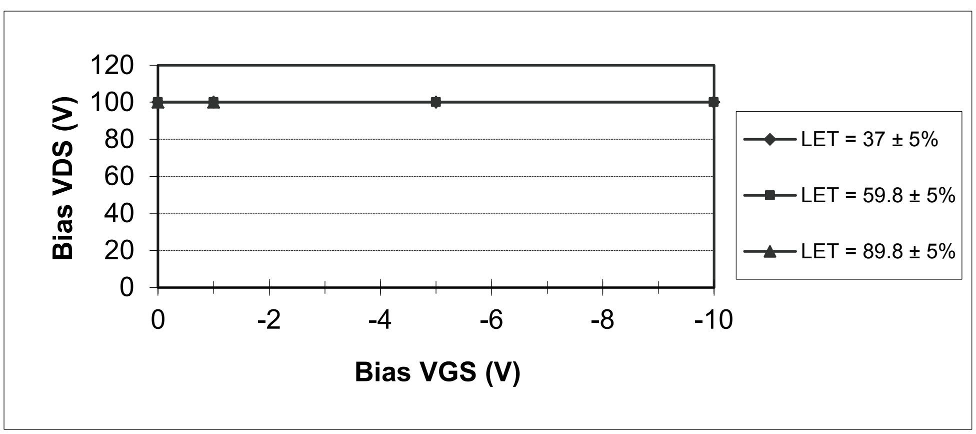


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

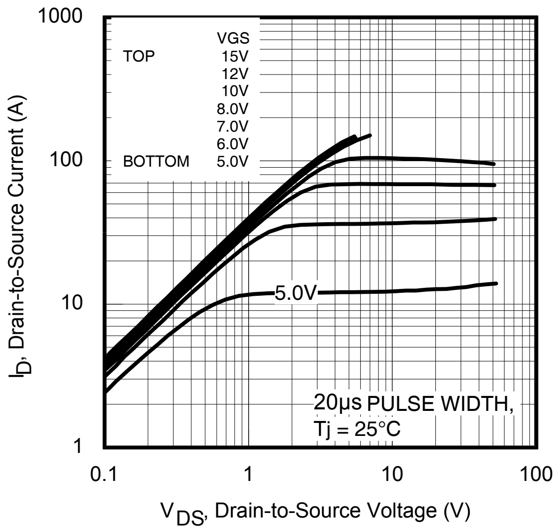


Fig 1. Typical Output Characteristics

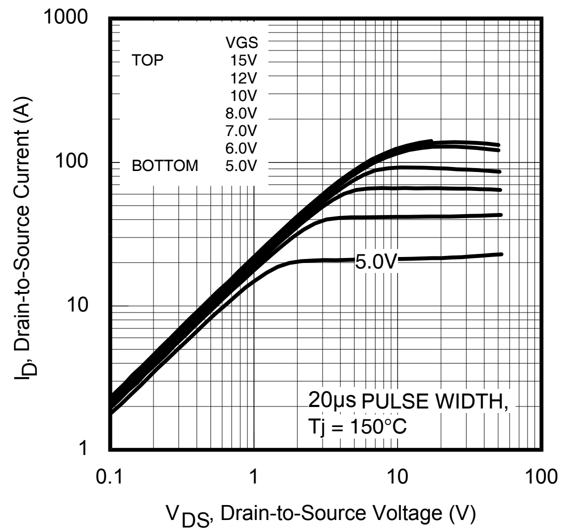


Fig 2. Typical Output Characteristics

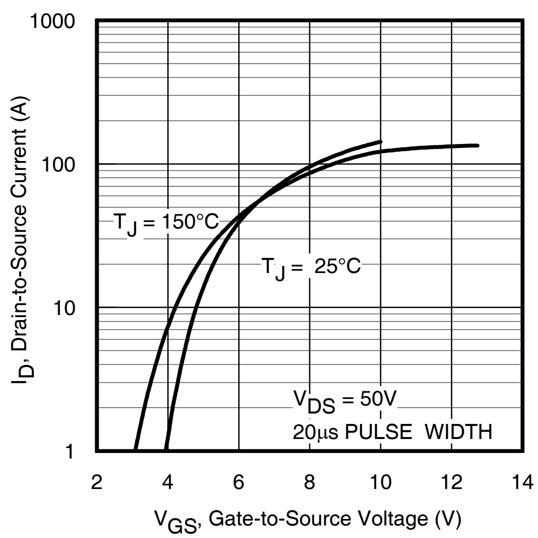


Fig 3. Typical Transfer Characteristics

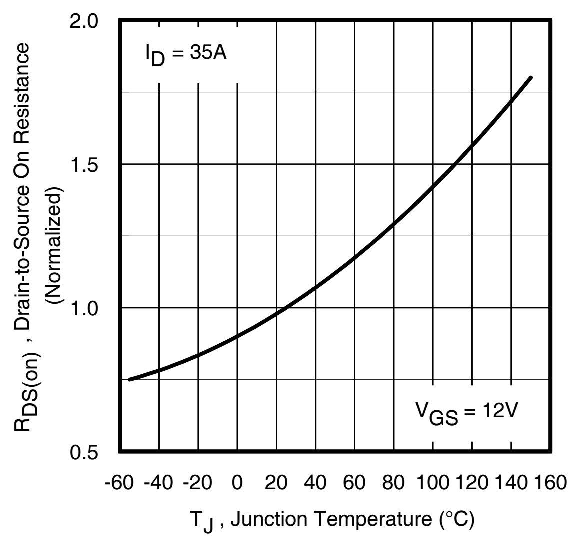


Fig 4. Normalized On-Resistance Vs. Temperature

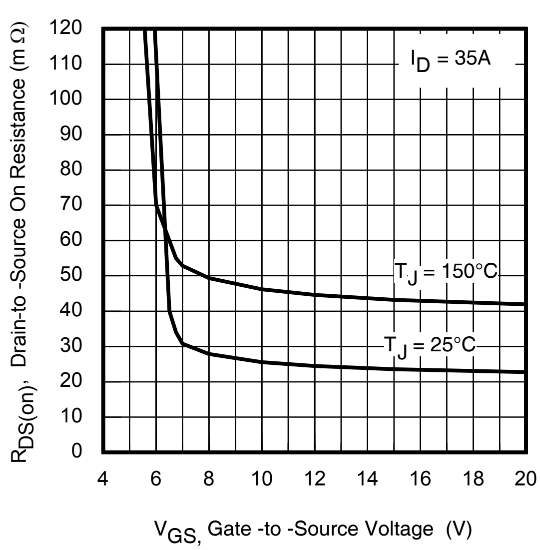


Fig 5. Typical On-Resistance Vs Gate Voltage

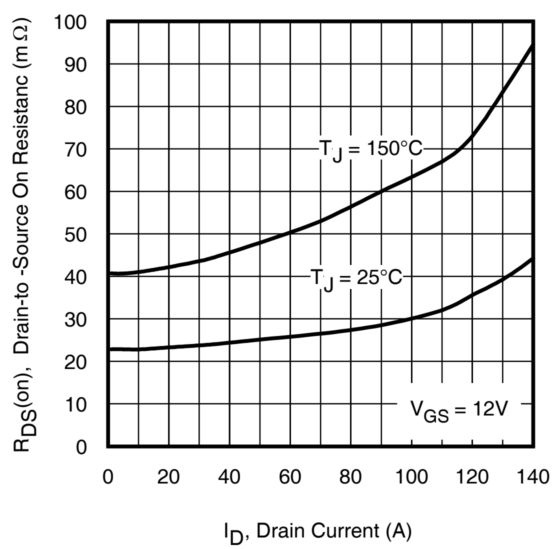


Fig 6. Typical On-Resistance Vs Drain Current

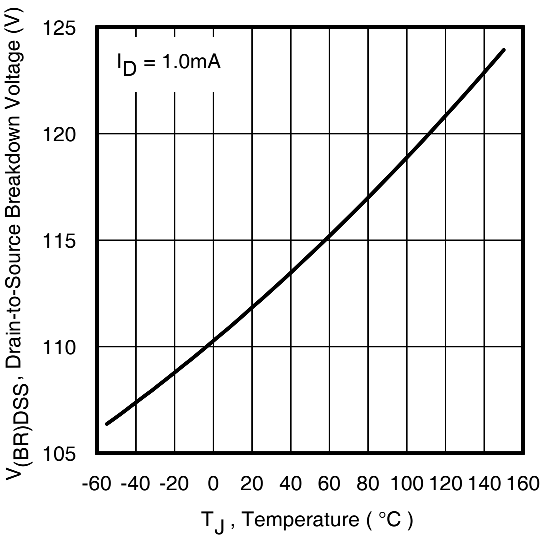


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

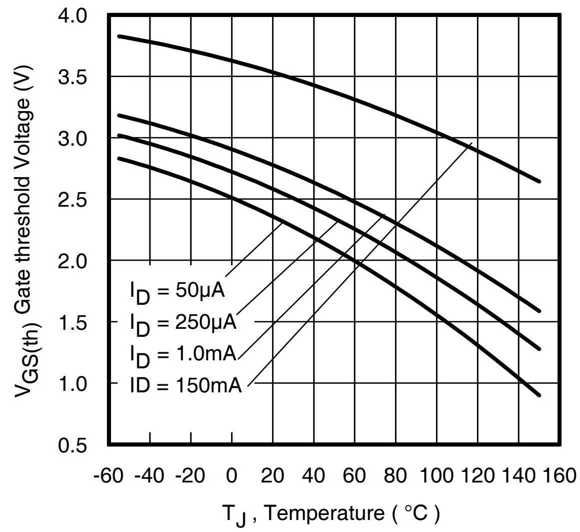


Fig 8. Typical Threshold Voltage Vs Temperature

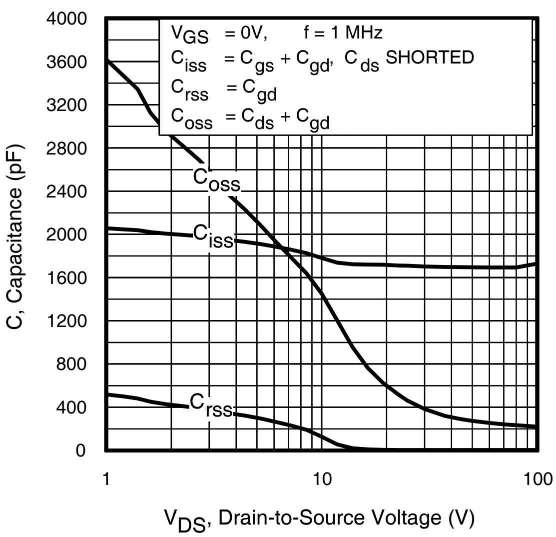


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

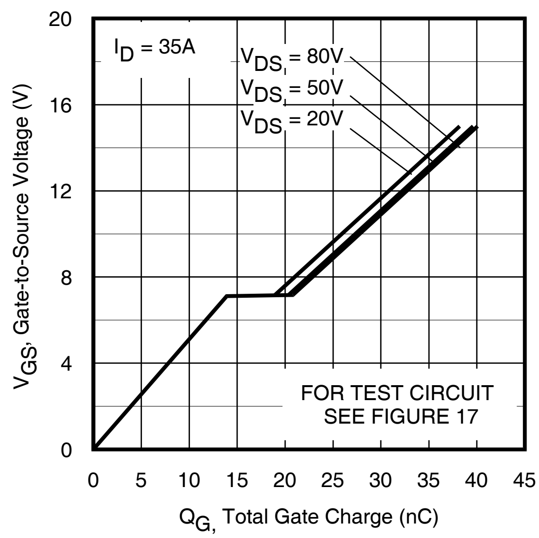


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

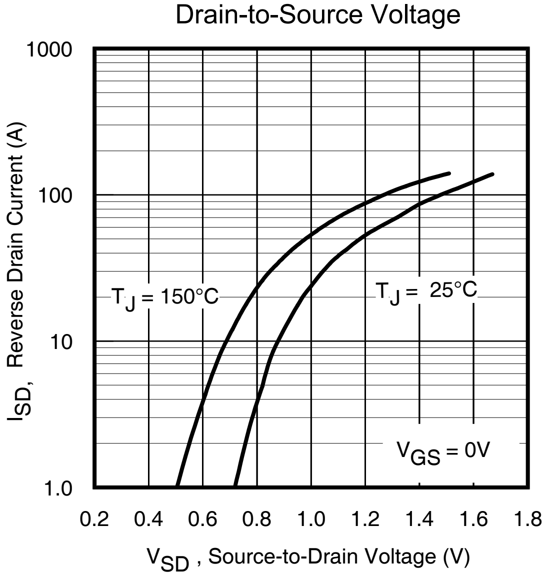


Fig 11. Typical Source-Drain Diode Forward Voltage

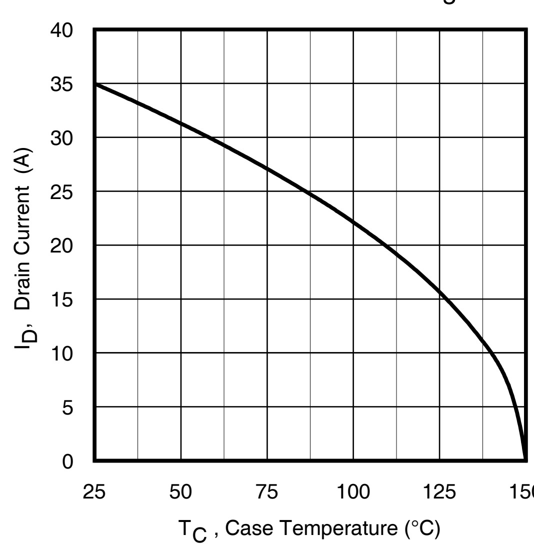


Fig 12. Maximum Drain Current Vs.Case Temperature

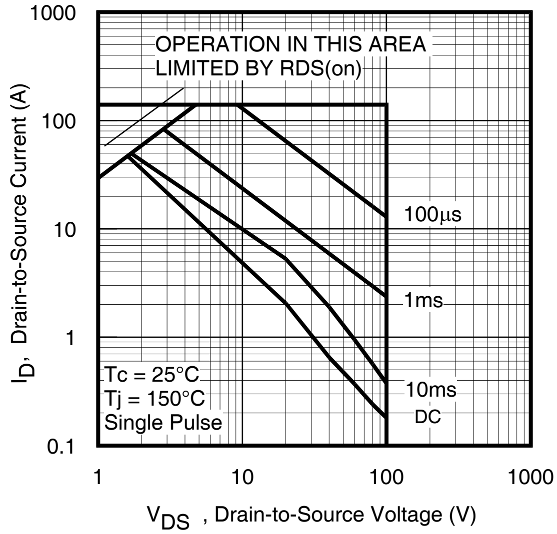


Fig 13. Maximum Safe Operating Area

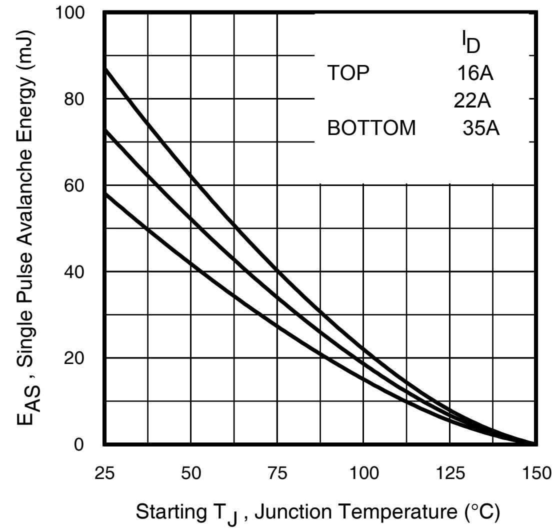


Fig 14. Maximum Avalanche Energy Vs. Drain Current

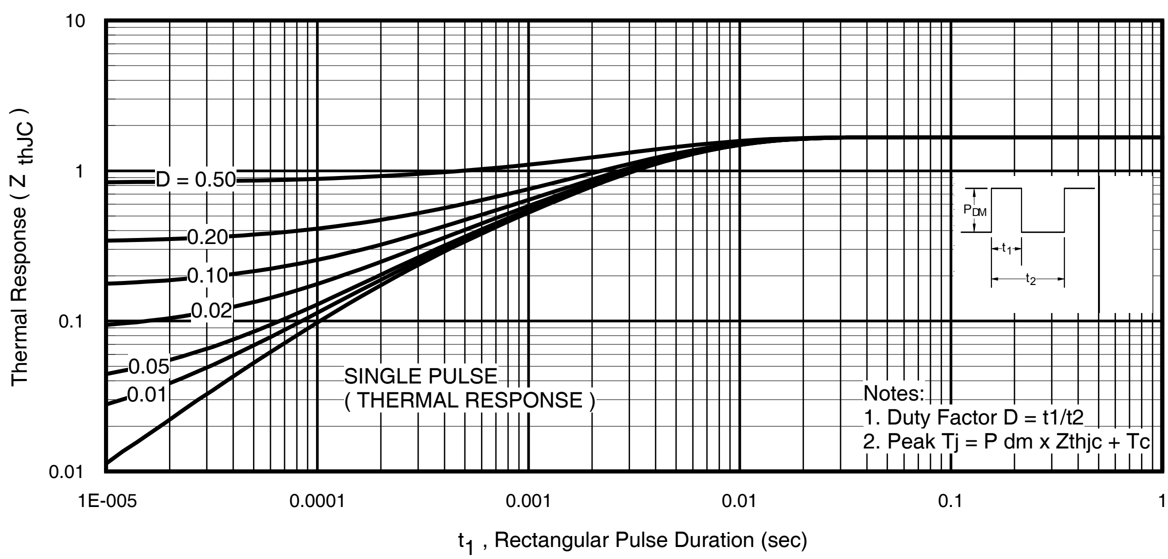


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

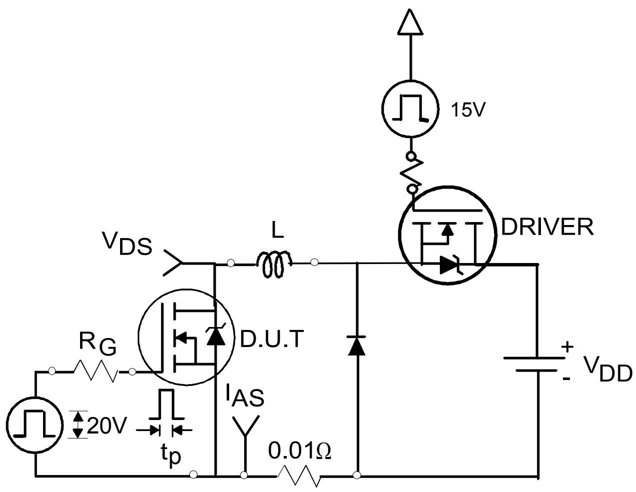


Fig 16a. Unclamped Inductive Test Circuit

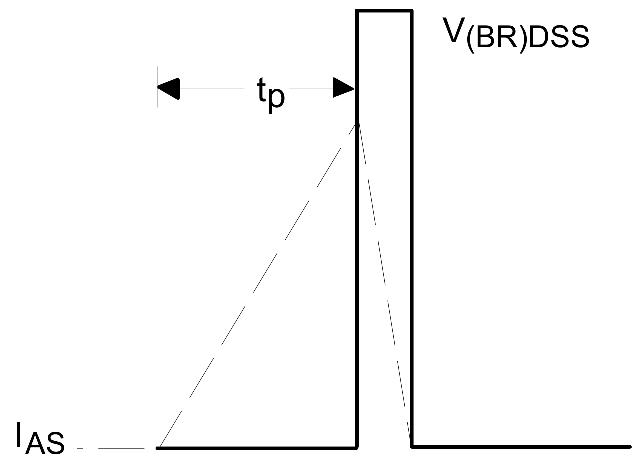


Fig 16b. Unclamped Inductive Waveforms

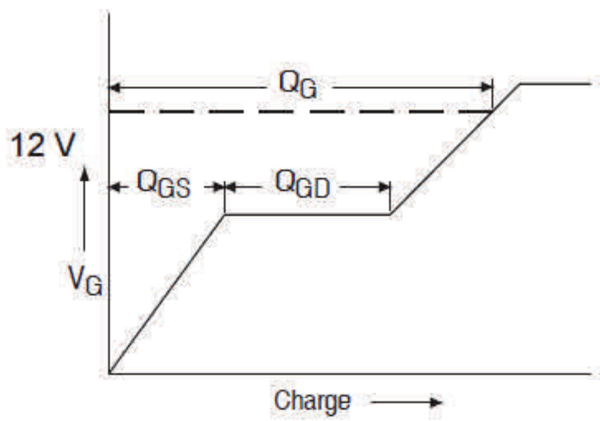


Fig 17a. Gate Charge Waveform

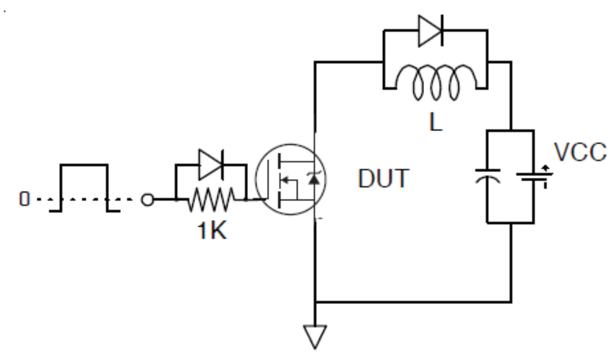


Fig 17b. Gate Charge Test Circuit

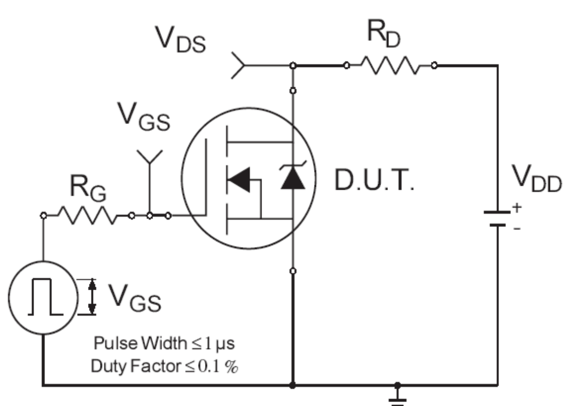


Fig 18a. Switching Time Test Circuit

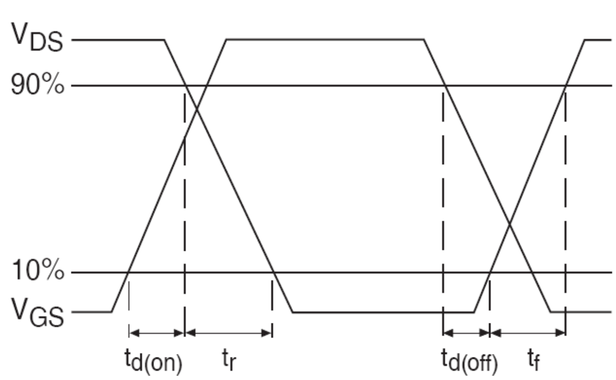
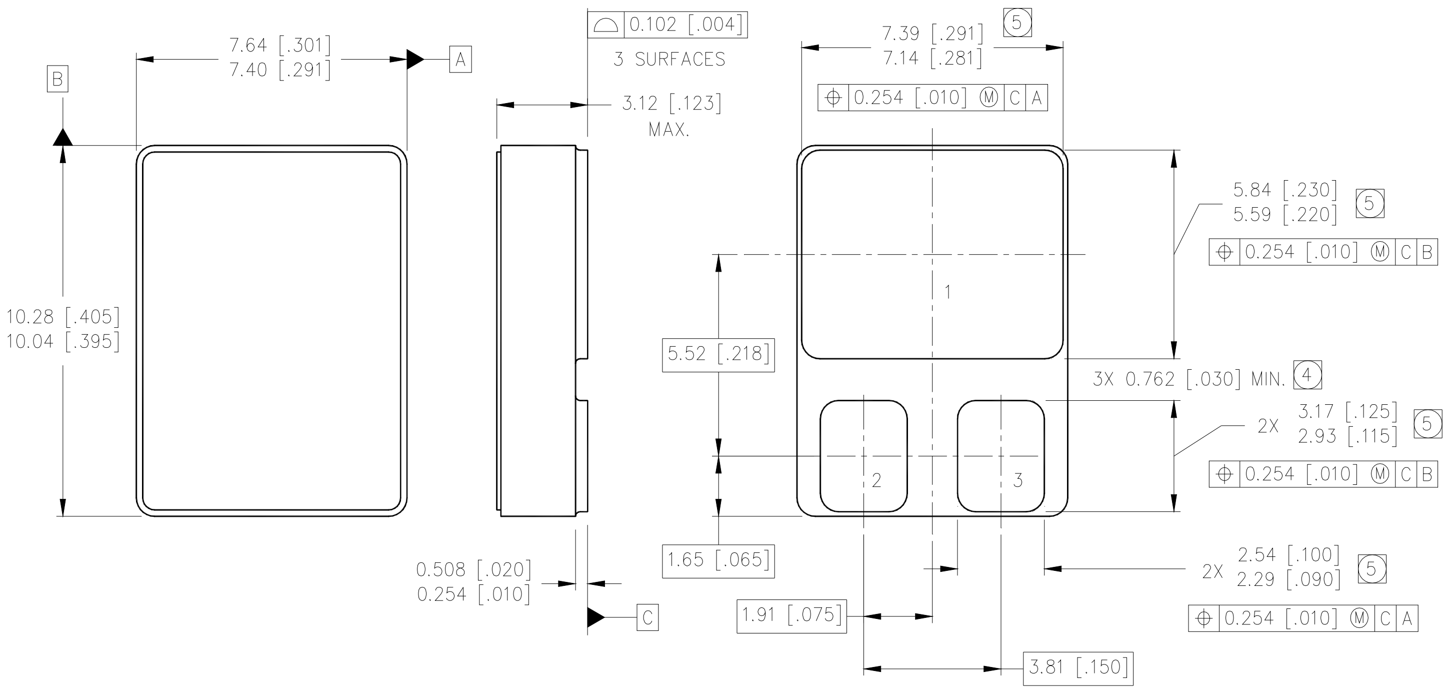


Fig 18b. Switching Time Waveforms

Case Outline and Dimensions - SMD-0.5



NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. DIMENSION INCLUDES METALLIZATION FLASH.
5. DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

MOSFET
1 = DRAIN
2 = GATE
3 = SOURCE

An Infineon Technologies Company
IR HiRel Headquarters: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA Tel: (310) 252-7105
IR HiRel Leominster: 205 Crawford St., Leominster, Massachusetts 01453, USA Tel: (978) 534-5776
IR HiRel San Jose: 2520 Junction Avenue, San Jose, California 95134, USA Tel: (408) 434-5000
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