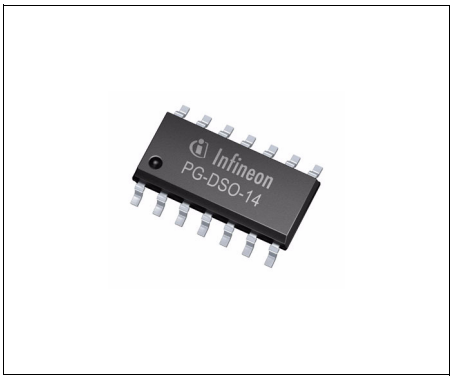
TLE7278-2

Low Dropout Voltage Regulator

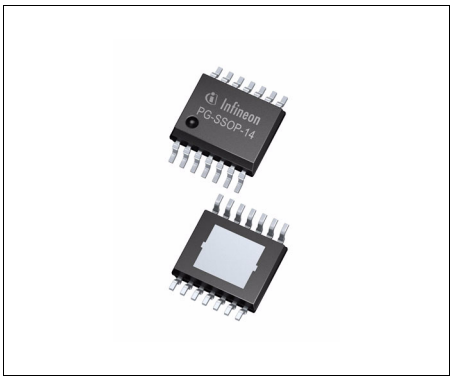
Automotive Power

Never stop thinking

1 Overview



PG-DSO-14



PG-SSOP-14 Exposed Pad

Features

- Output Voltage 5 V, 3.3 V or 2.6 V
- Output Voltage Tolerance ±2%
- Output Current Up To 180 mA
- Ultra Low Quiescent Current Consumption < 36 µA
- Enable Function
- Very Low Dropout voltage
- Reset With Adjustable Power-On Delay
- Standard Watchdog With Current Dependent Deactivation
- Output Current Limitation
- Wide Operation Range Up To 45 V
- Wide Temperature Range From -40 °C To 150 °C
- Overtemperature Shutdown
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE7278-2 is a monolithic integrated voltage regulator with integrated standard watchdog and reset dedicated for microcontroller supplies under harsh automotive environment conditions. The watchdog circuit is deactivated for very low loads at the device's output (e.g. microcontroller in standby mode).

Due to its ultra low quiescent current the TLE7278-2 is perfectly suited for applications that are permanently connected to battery. In addition, the regulator can be shut down via the Enable input causing the current consumption to drop below 3 µA. The TLE7278-2 is equipped with an overtemperature shutdown and an output current limitation protecting the device against overload, short circuit and overtemperature. It operates in the wide junction temperature range from -40 °C to 150 °C.

Type	Package	Marking
TLE7278-2GV50	PG-DSO-14	TLE7278-2GV50
TLE7278-2GV33	PG-DSO-14	TLE7278-2GV33
TLE7278-2GV26	PG-DSO-14	TLE7278-2GV26
TLE7278-2EV50	PG-SSOP-14 Exposed Pad	7278 V50

2 Block Diagram

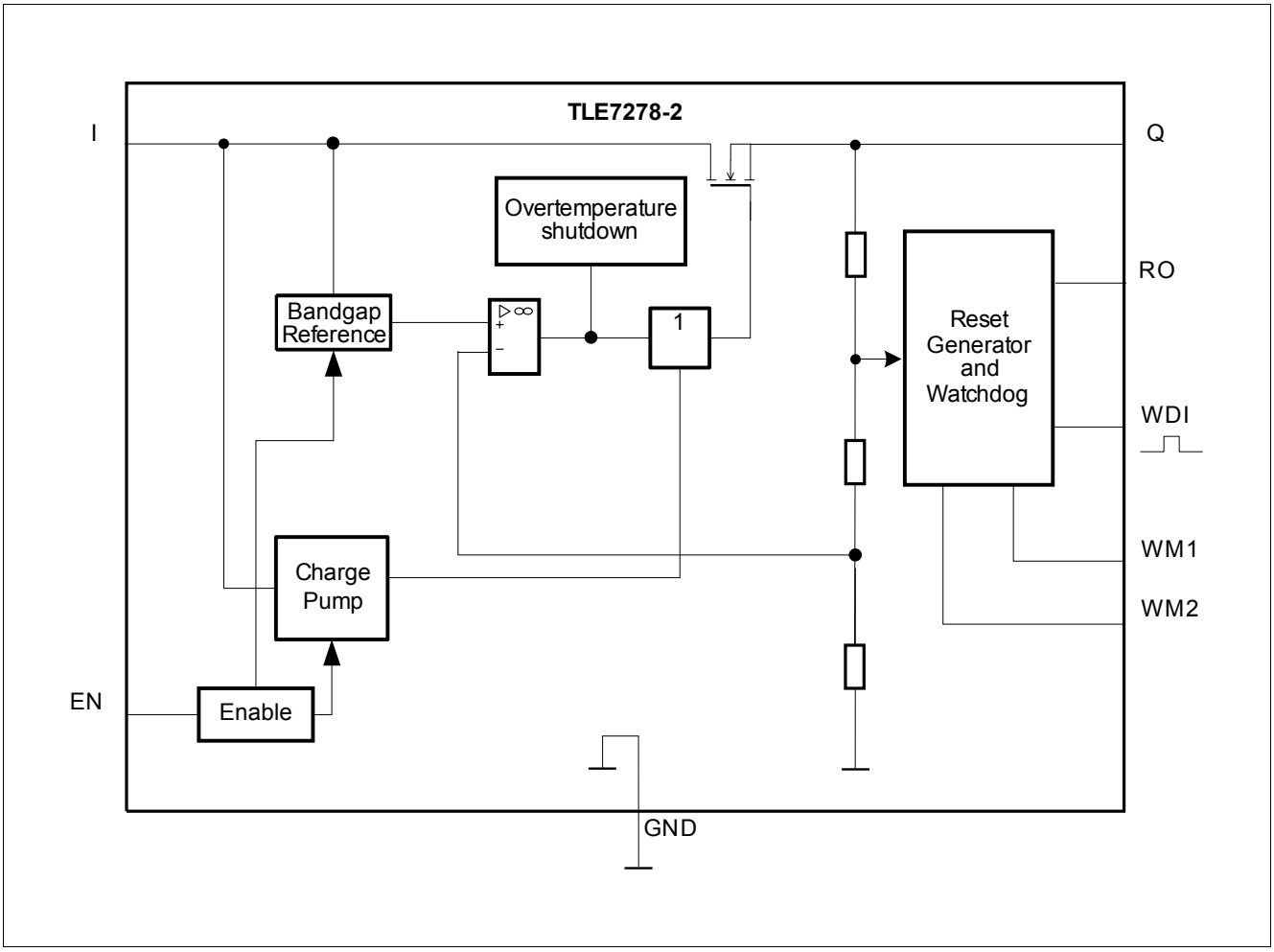


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment (PG-DSO-14)

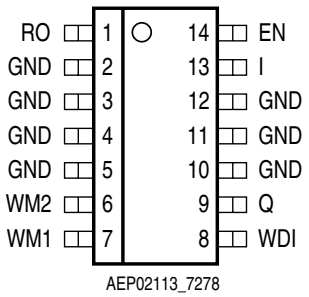


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions (PG-DSO-14)

Pin	Symbol	Function
1	RO	**Reset Output** TLE7278-2GV33, TLE7278-2GV26: open drain output; TLE7278-2GV50: integrated 20 kΩ pull-up resistor
2-5, 10-12	GND	**Ground** connect pin 2 and 3 to GND; connect pin 4-5, 10-12 to PCB heat sink area with GND potential
7	WM1	**Watchdog Mode Bit 1** watchdog and Reset mode selection, see **Figure 5**; connect to Q or GND
6	WM2	**Watchdog Mode Bit 2** watchdog and reset mode selection, see **Figure 5**; connect to Q or GND
8	WDI	**Watchdog Input** trigger input for watchdog pulses; pull down to GND if not needed and turn off the watchdog with WM1 and WM2 pin
9	Q	**Output Voltage** block to GND with a ceramic capacitor close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in **"Functional Range" on Page 7**
13	I	**Input Voltage** block to ground directly at the IC with a 100 nF ceramic capacitor
14	EN	**Enable Input** low level disables the IC; integrated pull-down resistor to GND

3.3 Pin Assignments (PG-SSOP-14 Exposed Pad)

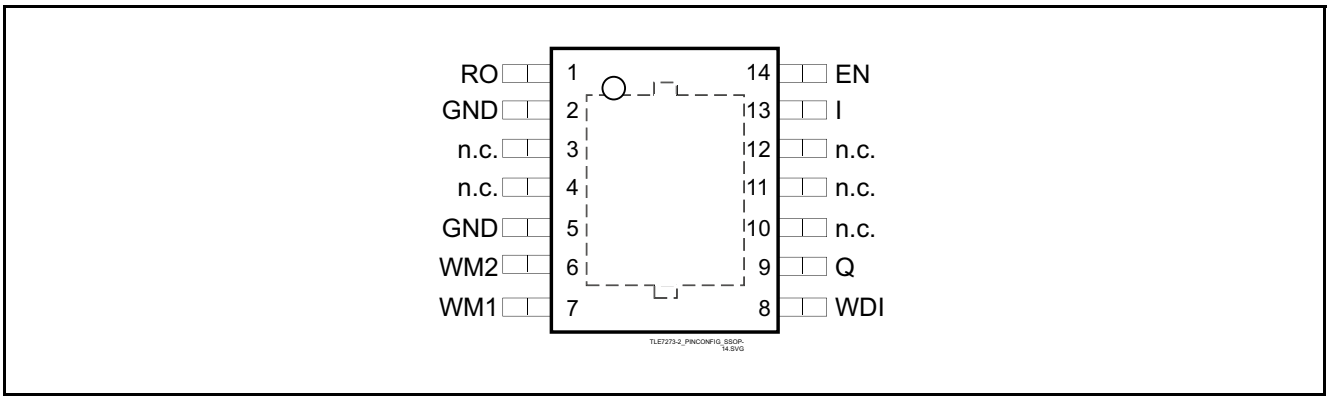


Figure 3 Pin Assignment PG-SSOP-14 Exposed Pad (top view)

3.4 Pin Definitions and Functions (PG-SSOP-14 Exposed Pad)

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1	RO	**Reset Output** integrated 20 kΩ pull-up resistor; leave open if not needed
2, 5	GND	**Ground** connect to GND
3, 4, 10, 11, 12	n.c.	**not connected** leave open or connect to GND
6	WM2	**Watchdog Mode Bit 2** watchdog and reset mode selection, see **Figure 5**; connect to Q or GND
7	WM1	**Watchdog Mode Bit 1** watchdog and Reset mode selection, see **Figure 5**; connect to Q or GND
8	WDI	**Watchdog Input** trigger input for watchdog pulses; pull down to GND if not needed and turn off the watchdog with WM1 and WM2 pin
9	Q	**Output Voltage** block to GND with a ceramic capacitor close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in **"Functional Range" on Page 7**
13	I	**Input Voltage** block to ground directly at the IC with a 100 nF ceramic capacitor
14	EN	**Enable Input** low level disables the IC; integrated pull-down resistor
Pad	–	**Exposed Pad** connect to heatsink area; connect to GND on PCB

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Input I						
4.1.1	Voltage	V_I	-0.3	45	V	–
Output Q, Reset Output RO, Watchdog Mode 2						
4.1.2	Voltage	V_Q	-0.3	5.5	V	permanent
4.1.3	Voltage	V_Q	-0.3	6.2	V	t < 10 s[2)]
Enable Input EN						
4.1.4	Voltage	V_{EN}	-1	45	V	–
4.1.5	Current	I_{EN}	-1	1	mA	–
Watchdog Input WDI						
4.1.6	Voltage	V_{RO}	-1	7	V	permanent
Watchdog Mode 1						
4.1.7	Voltage	V_{WM1}	-0.3	5.5	V	permanent
4.1.8	Voltage	V_{WM1}	-0.3	6.2	V	t < 10 s[2)]
4.1.9	Current	I_{WM1}	-5	5	mA	–
ESD Susceptibility						
4.1.10	Human Body Model (HBM)[3)]	Voltage	–	3	kV	–
4.1.11	Charge Device Model (CDM)[4)]	Voltage	–	1.5	kV	–
Temperatures						
4.1.12	Junction temperature	T_j	-40	150	°C	–
4.1.13	Storage temperature	T_{stg}	-50	150	°C	–

1) not subject to production test, specified by design

2) exposure to these absolute maximum ratings for extended periods (t > 10 s) may affect device reliability

3) ESD HBM Test according to JEDEC JESD22-A114

4) ESD CDM Test according AEC/ESDA ESD-STM5.3.1-1999

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Input voltage	V_I	5.5	45	V	TLE7278-2GV50, TLE7278-2EV50
4.2.2			4.2	45	V	TLE7278-2GV33
4.2.3			4.5	45	V	TLE7278-2GV26
4.2.4	Output Capacitor's Requirements for Stability	C_Q	470	–	nF	–[1]
		$ESR(C_Q)$	–	3	Ω	–[2]
4.2.5	Junction Temperature	T_j	-40	150	°C	–

1) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) relevant ESR value at f = 10 kHz

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Package PG-DSO-14							
4.3.1	Junction to Soldering Point[1]	R_{thJSP}	–	30	–	K/W	measured to group of pins 3, 4, 5, 10, 11, 12
4.3.2	Junction to Ambient[1]	R_{thJA}	–	53	–	K/W	[2]
4.3.3			–	105	–	K/W	footprint only[3]
4.3.4			–	74	–	K/W	300 mm² heatsink area on PCB[3]
4.3.5			–	65	–	K/W	600 mm² heatsink area on PCB[3]
Package PG-SSOP-14 Exposed Pad							
4.3.6	Junction to Case[1]	R_{thJC}	–	14	–	K/W	measured to exposed pad
4.3.7	Junction to Ambient[1]	R_{thJA}	–	47	–	K/W	[2]
4.3.8			–	141	–	K/W	footprint only[3]
4.3.9			–	66	–	K/W	300 mm² heatsink area on PCB[3]
4.3.10			–	56	–	K/W	600 mm² heatsink area on PCB[3]

1) not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 x 70µm Cu).

5 Block Description and Electrical Characteristics

5.1 Circuit Description

5.1.1 Power On Reset and Reset Output

For an output voltage level $V_Q \geq 1$ V the reset output is hold low. When the level of V_Q reaches the reset threshold V_{RT}, the signal at RO remains low for the power-up reset delay time t_{RD}. The reset function and timing is illustrated in **Figure 4**. The reset reaction time t_{RR} avoids wrong triggering caused by short “glitches” on the V_Q-line. In case of V_Q power down ($V_Q < V_{RT}$ for $t > t_{RR}$) a logic low signal is generated at the pin RO to reset an external micro controller.

The TLE7278-2GV50 and TLE7278-2EV50 feature an integrated pull-up resistor on the reset output while the TLE7278-2GV33 and TLE7278-2GV26 have an open drain output requiring an external pull-up resistor. When connected to a voltage level of V_{ext} = 5 V, a recommended value for this external resistor is ≥ 5.6 kΩ.

But it’s also possible calculating its value by using the following formula, based on the reset sink current (Example: external pull-up resistor connected to V_{ext} = 5 V):

$R_{extmin} = \Delta V / I_{RO} = (V_{ext} - V_{ROmin}) / I_{RO}$ = (5 V - 0.25 V) / 1.0 mA = 4.75 kΩ

At low output voltage levels $V_Q < 1$ V the integrated pull-up resistor of the TLE7278-2GV50 is switched off setting the reset output high ohmic.

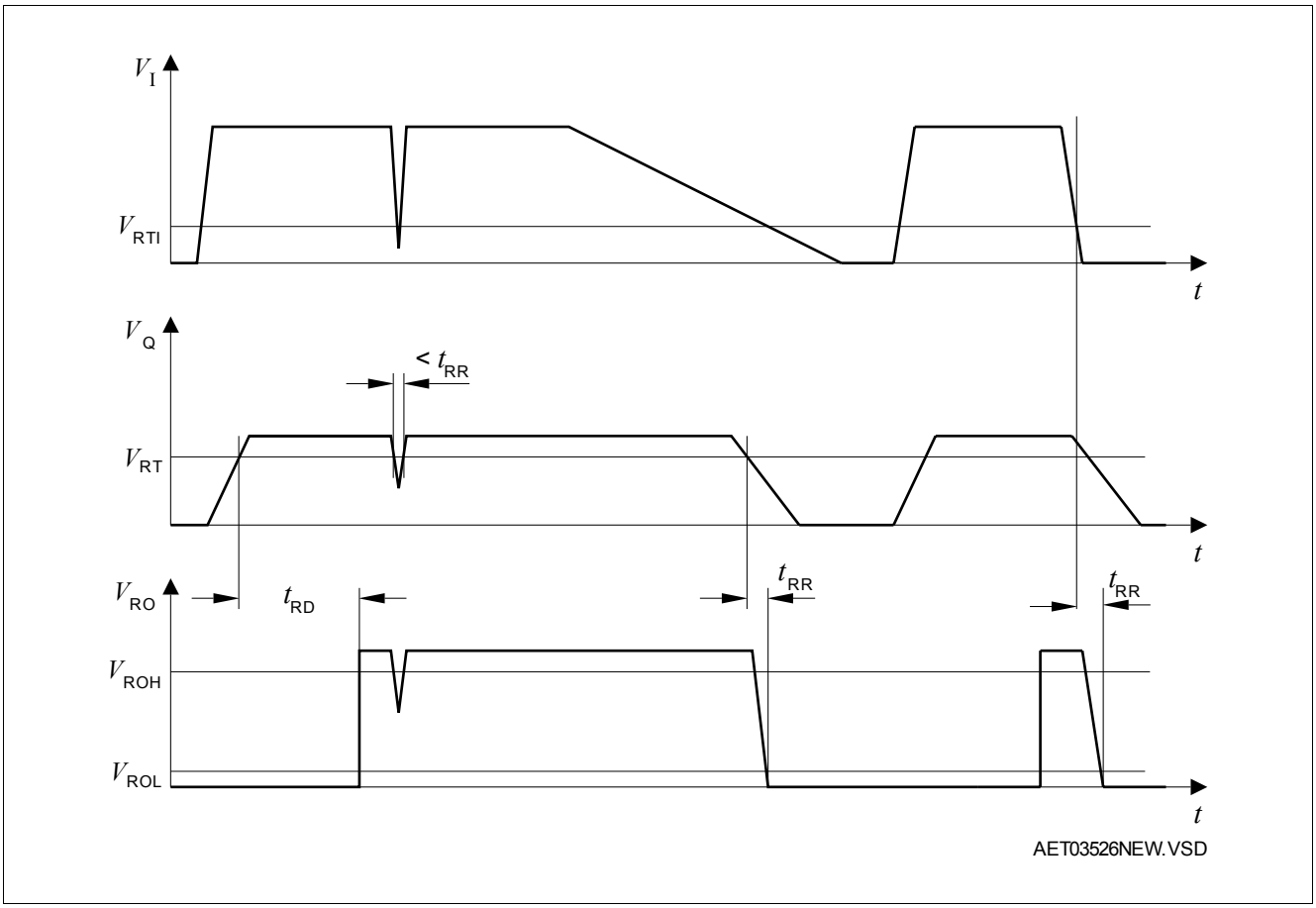


Figure 4 Reset Function and Timing Diagram

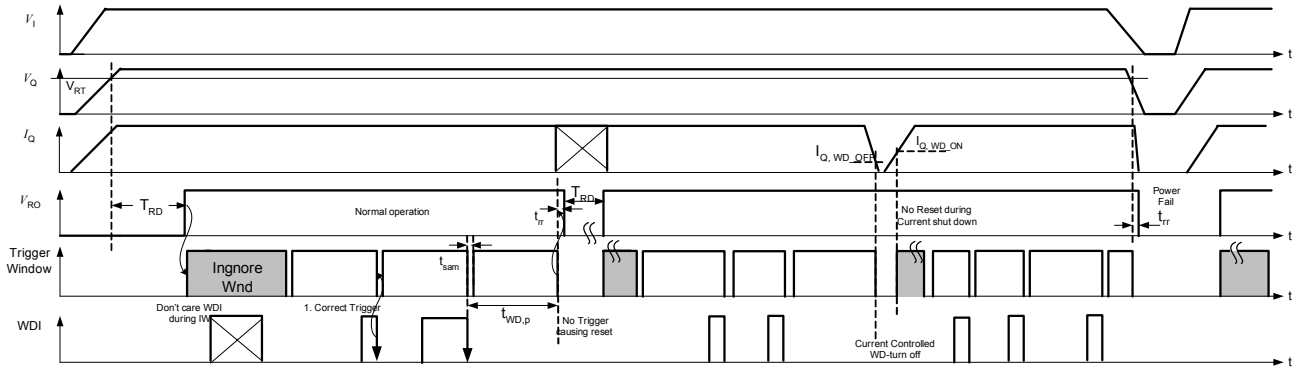
5.1.2 Watchdog Operation

The watchdog uses a fraction of the charge pump oscillator's clock signal as timebase. The watchdog timebase can be adjusted using the pins WM1 and WM2 (see **Figure 5**). The watchdog can be turned off setting WM1 and WM2 to high level. The timing values used this text refer to typ. values with WM1 and WM2 connected to GND (fast watchdog and reset timing).

If the timebase is switched by changing the condition on the WM pins, the new timing is valid from the beginning of the new period on. From this time on, the frequency on the WDI pin must be adapted.

Figure 5 shows the state diagram of the watchdog (WD) and the mode selection. After power-on, the reset output signal at the RO pin (microcontroller reset) is kept LOW for the reset delay time T_{RD} of typ. 16 ms. With the LOW to HIGH transition of the signal at RO the device starts the ignore window time t_{CW} (32 ms). Next the WD starts the Watchdog Period (time frame within a trigger at WDI must occur). From now on the timing of the signal on WDI from the micro controller must correspond the WD-Period $t_{WD,p}$ correspondent the electrical characteristics and based on the setting on the WM pins. A Re-Trigger of the WD-Period is done with a HIGH-to-LOW Transient at the WDI-pin within the set $t_{WD,p}$.

A HIGH to LOW transition of the watchdog trigger signal on pin WDI is taken as a trigger. To avoid wrong triggering due to parasitic glitches two HIGH samples followed by two LOW samples (sample period t_{sam} typ. 0.5 ms) are decoded as a valid trigger. A reset is generated (RO goes LOW) if there is no trigger pulse during the Watchdog Period.



WM1	L	L	H	H
WM2	L	H	L	H
Watchdog Mode	Fast	Slow	Fast	Off
Reset Mode	Fast	Slow	Slow	Slow

7278 Timing

Figure 5 Watchdog Timing Diagram, Watchdog and Reset Modes

5.2 Electrical Characteristics

Electrical Characteristics

V_I = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Output Q							
5.2.1	Output voltage	V_Q	4.90	5.00	5.10	V	TLE7278-2GV50, TLE7278-2EV50 1 mA < I_Q < 180 mA 6 V < V_I < 16 V
5.2.2	Output voltage	V_Q	4.90	5.00	5.10	V	TLE7278-2GV50, TLE7278-2EV50 I_Q = 10 mA 6 V < V_I < 45 V
5.2.3	Output voltage	V_Q	3.234	3.30	3.366	V	TLE7278-2GV33 1 mA < I_Q < 180 mA 4.5 V < V_I < 16 V
5.2.4	Output voltage	V_Q	3.234	3.30	3.366	V	TLE7278-2GV33 I_Q = 10 mA 4.5 V < V_I < 45 V
5.2.5	Output voltage	V_Q	2.548	2.60	2.652	V	TLE7278-2GV26 1 mA < I_Q < 180 mA 4.5 V < V_I < 16 V
5.2.6	Output voltage	V_Q	2.548	2.60	2.652	V	TLE7278-2GV26 I_Q = 10 mA 4.5 V < V_I < 45 V
5.2.7	Output current limitation	I_Q	200	–	500	mA	V_Q = 2.0 V
			200	–	600	mA	V_Q = 0 V
5.2.8	Dropout Voltage; V_{DR} = V_I - V_Q	V_{DR}	–	250	500	mV	I_Q = 180 mA[1)] TLE7278-2GV50, TLE7278-2EV50
5.2.9	Load regulation	$\Delta V_{Q,Lo}$	–	50	90	mV	1 mA < I_Q < 180 mA
5.2.10	Line regulation	$\Delta V_{Q,Li}$	–	10	50	mV	I_Q = 1 mA; 10 V < V_I < 32 V
5.2.11	Power-Supply-Ripple-Rejection	$PSRR$	–	60	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
5.2.12	Reverse Output Current Clamping	$V_{Q,REV}$	–	–	5.5	V	$I_{Q,REV}$ = -1 mA; V_{EN} = 0 V
Current Consumption							
5.2.13	Quiescent current; I_q = I_I - I_Q	I_q	–	28	36	µA	I_Q = 100 µA; T_j < 80 °C
5.2.14	Quiescent current; Disabled	I_q	–	1	3	µA	V_{EN} = 0 V; T_j < 80 °C
Enable Input EN							
5.2.15	High Level Input Voltage	$V_{EN,H}$	3.0	–	–	V	V_Q on

Electrical Characteristics (cont'd)

V_I = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.16	Low Level Input Voltage	$V_{EN,L}$	–	–	0.5	V	V_Q = 0.02 V; I_Q = 5 mA; T_j < 125 °C
5.2.17			–	–	0.3	V	V_Q = 0.02 V I_Q = 5 mA
5.2.18	High Level Input Current	$I_{EN,H}$	–	3	4	µA	V_{EN} = 5 V
Watchdog Mode Bit 1							
5.2.19	High Level Input Voltage	$V_{WM1,H}$	4.00	–	–	V	TLE7278-2GV50, TLE7278-2EV50
5.2.20			2.65	–	–	V	TLE7278-2GV33
5.2.21			2.30	–	–	V	TLE7278-2GV26
5.2.22	Low Level Input Voltage	$V_{WM1,L}$	–	–	0.80	V	–
Watchdog Mode Bit 2							
5.2.23	High Level Input Voltage	$V_{WM2,H}$	4.00	–	–	V	TLE7278-2GV50, TLE7278-2EV50
5.2.24			2.65	–	–	V	TLE7278-2GV33
5.2.25			2.30	–	–	V	TLE7278-2GV26
5.2.26	Low Level Input Voltage	$V_{WM2,L}$	–	–	0.80	V	–
Watchdog Input WDI							
5.2.27	High Level Input Voltage	$V_{WDI,H}$	4.0	–	–	V	TLE7278-2GV50, TLE7278-2EV50
5.2.28			2.65	–	–	V	TLE7278-2GV33
5.2.29			2.30	–	–	V	TLE7278-2GV26
5.2.30	Low Level Input Voltage	$V_{WDI,L}$	–	–	0.80	V	–
5.2.31	High Level Input Current	$I_{WDI,H}$	–	3	4	µA	V_{WDI} = 5 V
5.2.32	Low Level Input Current	$I_{WDI,L}$	–	0.5	1	µA	V_{WDI} = 0 V; T_j < 80 °C
5.2.33	Watchdog sampling time	t_{sam}	0.40	0.50	0.60	ms	fast watchdog timing
			0.80	1.00	1.20	ms	slow watchdog timing
5.2.34	Ignore window time	t_{OW}	25.6	32.0	38.4	ms	fast watchdog timing
			51.2	64.0	76.8	ms	slow watchdog timing
5.2.35	Watchdog Period	$t_{WD,p}$	25.6	32	38.4	ms	fast watchdog timing
			51.2	64	76.8	ms	slow watchdog timing
5.2.36	Watchdog deactivation current threshold	I_{Q,WD_off}	0.5	–	–	mA	I_Q decreasing $V_I > V_{I,WD\_on} > 6.0$ V for TLE7278-2GV50, TLE7278-2EV50 $V_I > V_{I,WD\_on} > 4.5$ V for TLE7278-2GV33, TLE7278-2GV26

Electrical Characteristics (cont'd)

V_I = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.37	Watchdog activation current threshold	I_{Q,WD_on}	–	–	5	mA	I_Q increasing $V_I > V_{I,WD\_on} > 6.0$ V for TLE7278-2GV50, TLE7278-2EV50 $V_I > V_{I,WD\_on} > 4.5$ V for TLE7278-2GV33, TLE7278-2GV26
Reset Output RO							
5.2.38	Output Voltage Reset Switching Threshold	V_{RT}	4.50	4.60	4.70	V	TLE7278-2GV50, TLE7278-2EV50 V_Q decreasing
5.2.39			3.00	3.07	3.13	V	TLE7278-2GV33[2)] V_Q decreasing
5.2.40			2.35	2.38	2.45	V	TLE7278-2GV26[2)] V_Q decreasing
5.2.41	Input Voltage Reset Switching Threshold	V_{RT_VI}	–	3.9	4.0	V	TLE7278-2GV26[2)] TLE7278-2GV33[2)] $V_Q > V_{RT}$, V_I decreasing
5.2.42	Reset Hysteresis	V_{RH}	–	45	–	mV	TLE7278-2GV26
5.2.43			–	60	–	mV	TLE7278-2GV33
5.2.44			–	90	–	mV	TLE7278-2GV50, TLE7278-2EV50
5.2.45	Maximum Reset Sink Current	I_{RO}	1.75	–	–	mA	TLE7278-2GV50, TLE7278-2EV50 V_Q = 4.5 V, V_{RO} = 0.25 V
5.2.46			1.3	–	–	mA	TLE7278-2GV33 V_Q = 3.0 V, V_{RO} = 0.25 V
5.2.47			1.0	–	–	mA	TLE7278-2GV26 V_Q = 2.35 V, V_{RO} = 0.25 V
5.2.48	Reset output low voltage	V_{ROL}	–	0.15	0.25	V	$V_Q \geq 1$ V; $I_{RO} < 200$ µA
5.2.49	Reset high voltage	V_{ROH}	4.5	–	–	V	TLE7278-2GV50, TLE7278-2EV50
5.2.50	Reset high leakage current	I_{ROLK}	–	–	1	µA	TLE7278-2GV33 TLE7278-2GV26

Electrical Characteristics (cont'd)

V_I = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

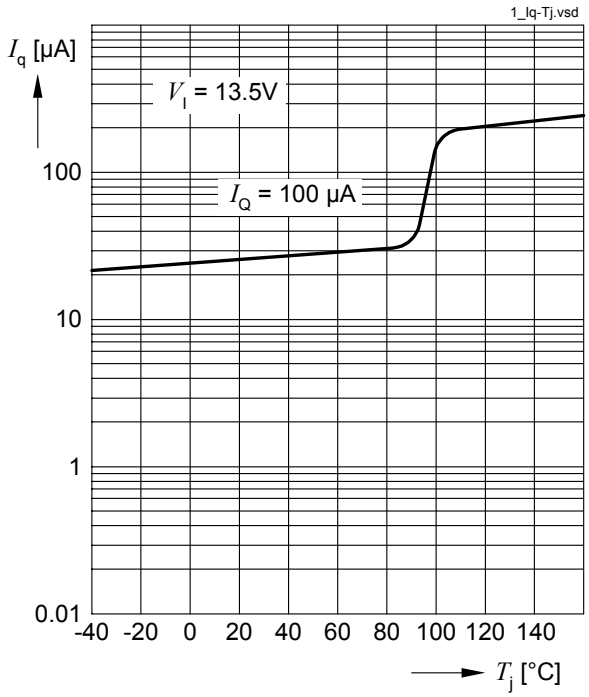
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.51	Integrated reset pull-up resistor	R_{RO}	10	20	40	kΩ	TLE7278-2GV50, TLE7278-2EV50 internally connected to V_Q
5.2.52	Power-on Reset delay time	T_{RD}	12.8	16.0	19.2	ms	fast reset timing
			25.6	32.0	38.4	ms	slow reset timing
5.2.53	Reset Reaction Time	T_{RR}	–	4	12	µs	–

1) measured when the output voltage has dropped 100 mV from the nominal Value obtained at V_I = 13.5 V

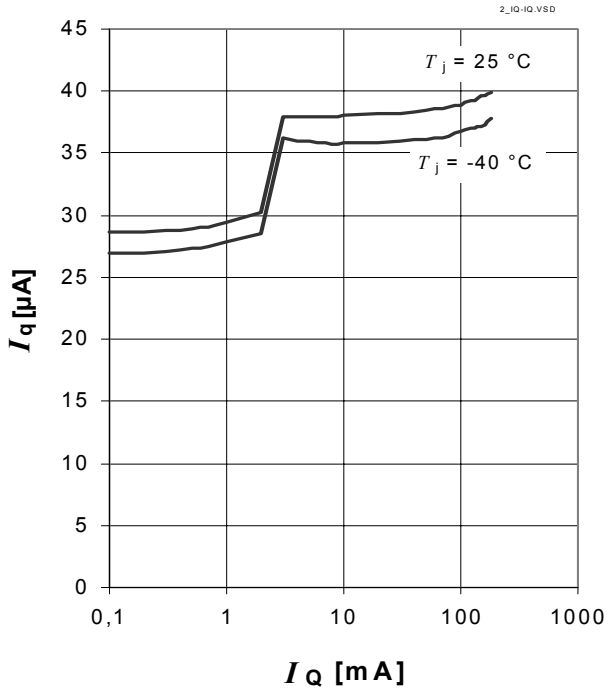
2) reset output triggered when output voltage V_Q is lower than output voltage reset switching threshold V_{RT} or is also triggered, when input voltage is decreasing to V_I < 4.0 V and V_Q > V_{RT}

Typical Performance Characteristics

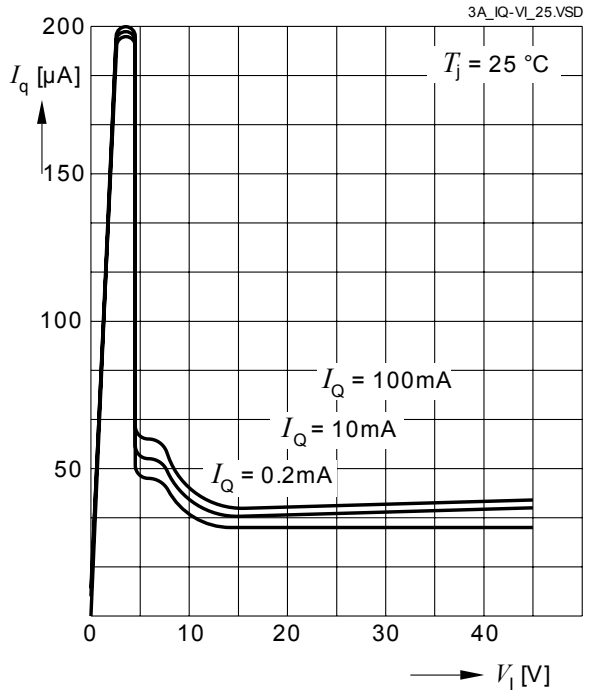
Current Consumption I_q versus Junction Temperature T_j (EN=ON)



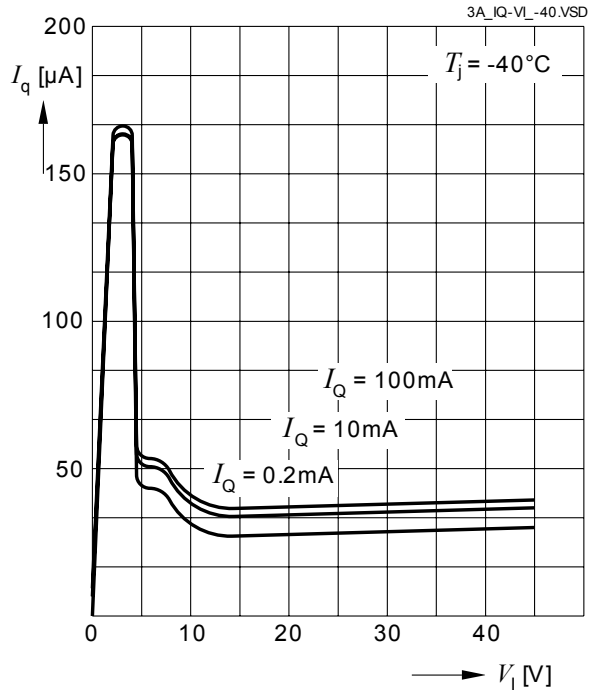
Current Consumption I_q versus Output Current I_Q (EN=ON)



Current Consumption I_q versus Input Voltage V_I at T_j=25°C (EN=ON)

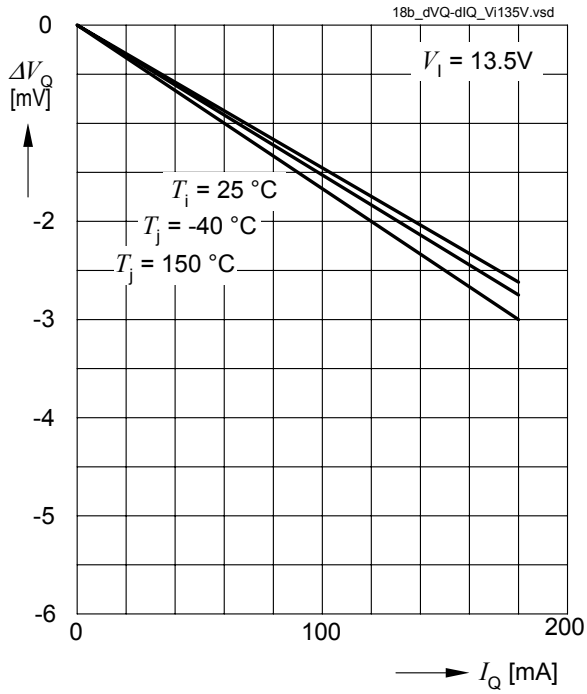


Current Consumption I_q versus Input Voltage V_I at T_j=-40°C (EN=ON)

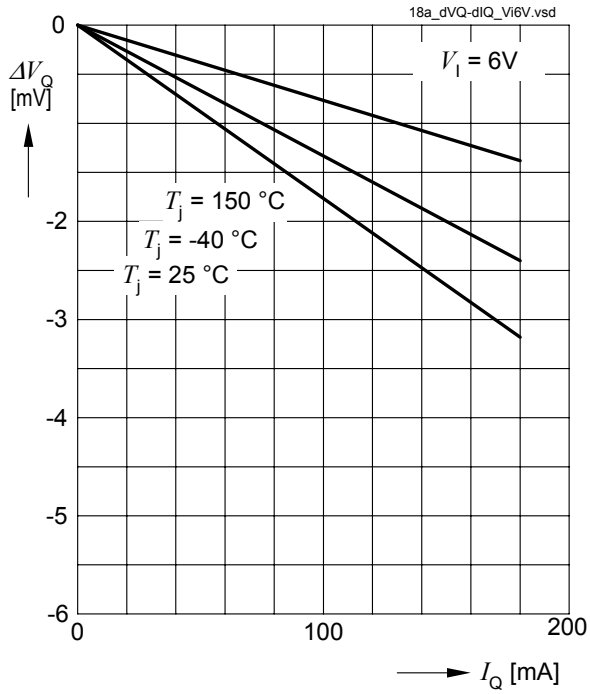


Typical Performance Characteristics (cont´d)

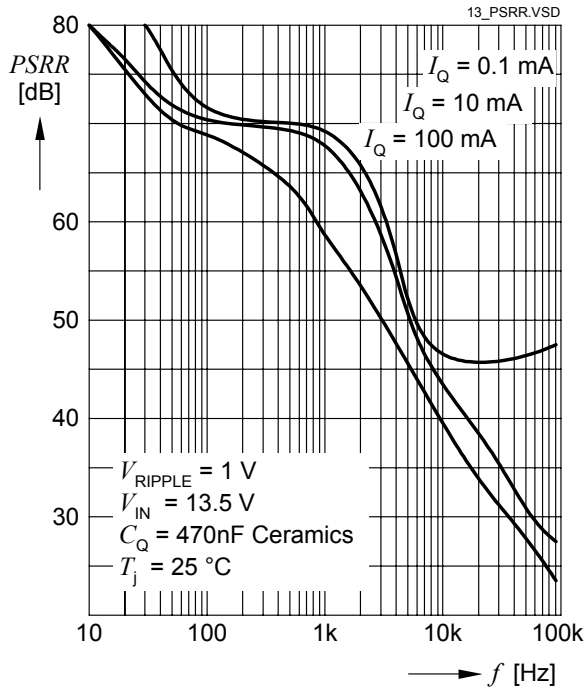
Load Regulation dV_Q versus Output Current Change dI_Q



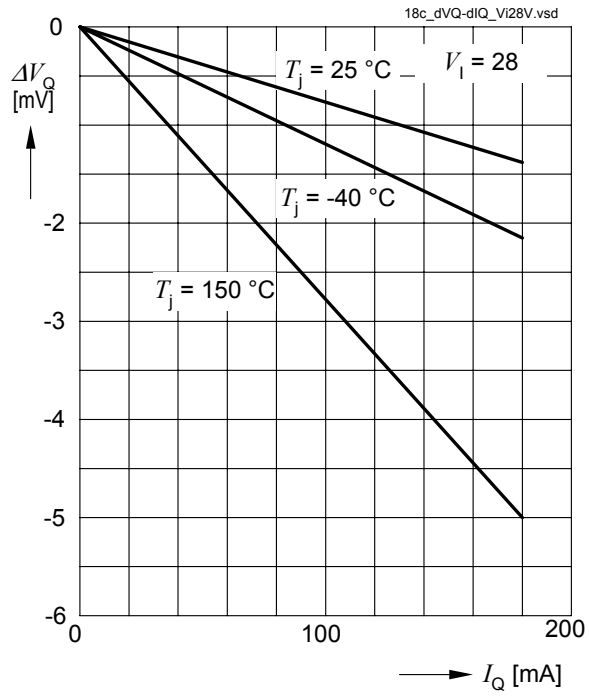
Load Regulation dV_Q versus Output Current Change dI_Q



Power Supply Ripple Rejection *PSRR*

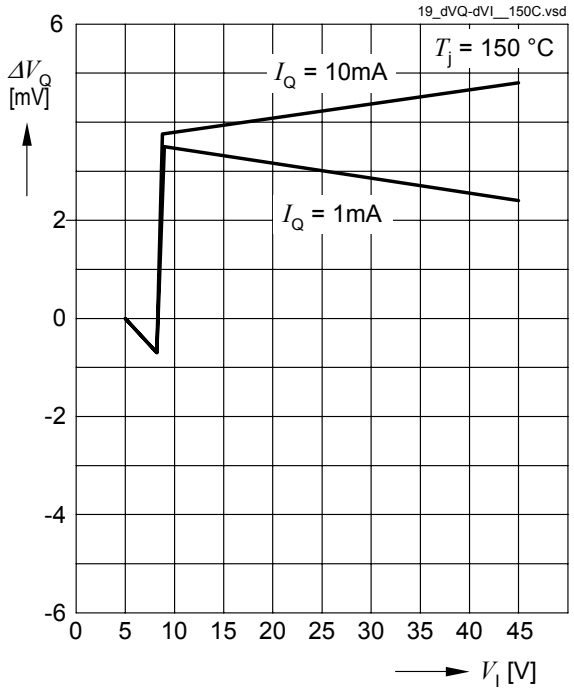


Load Regulation dV_Q versus Output Current Change dI_Q

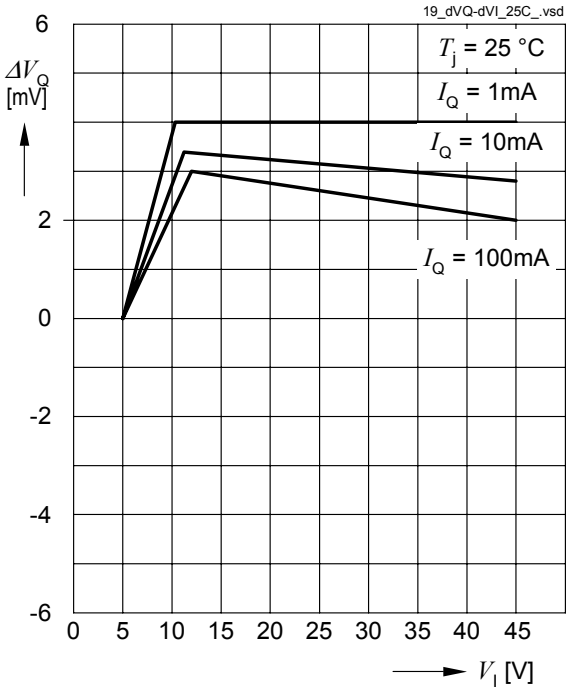


Typical Performance Characteristics (cont´d)

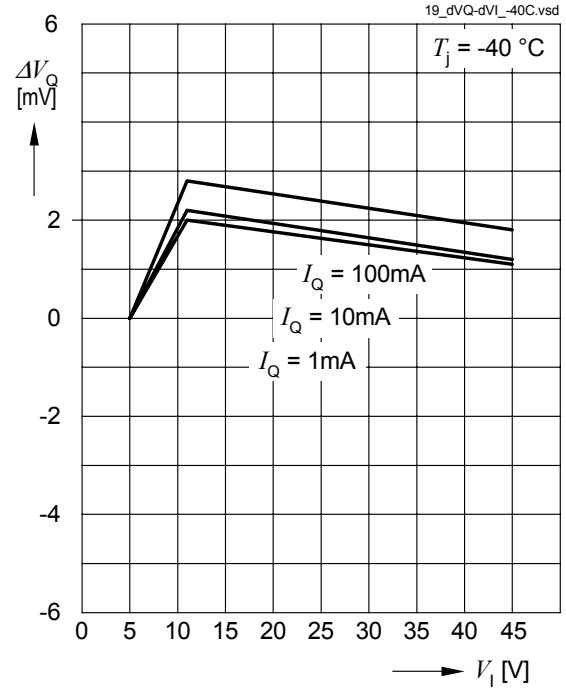
Line Regulation dV_Q versus Input Voltage Change dV_I



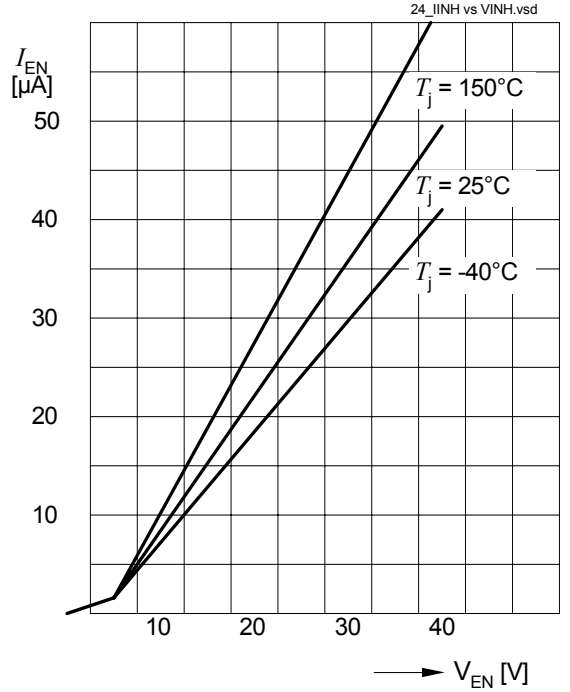
Line Regulation dV_Q versus Input Voltage Change dV_I



Line Regulation dV_Q versus Input Voltage Change dV_I

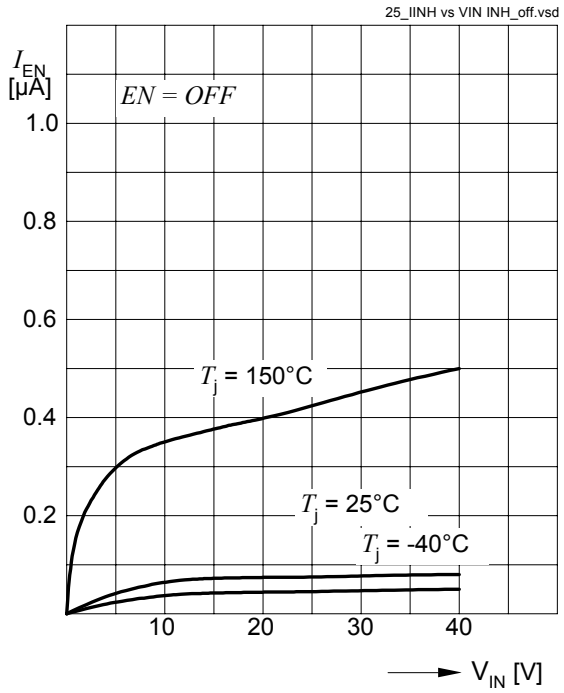


Enable Input Current I_{EN} versus Enable Input Voltage V_{EN}

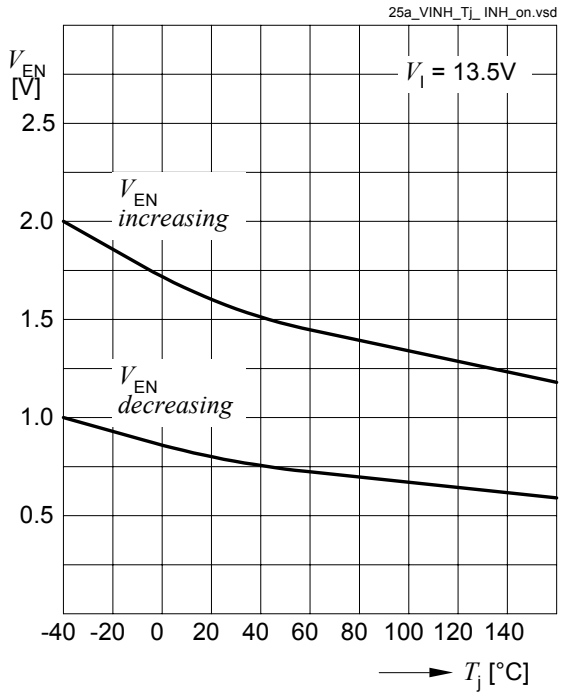


Typical Performance Characteristics (cont´d)

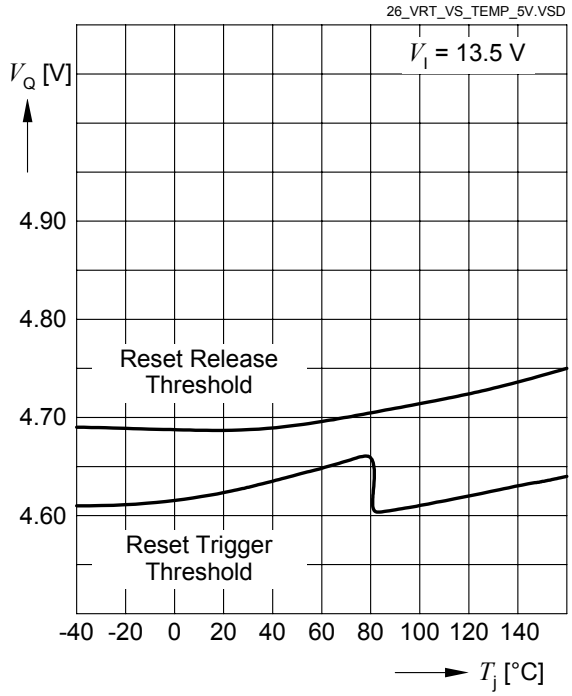
Enable Input Current I_{EN} versus Input Voltage V_I, EN=Off



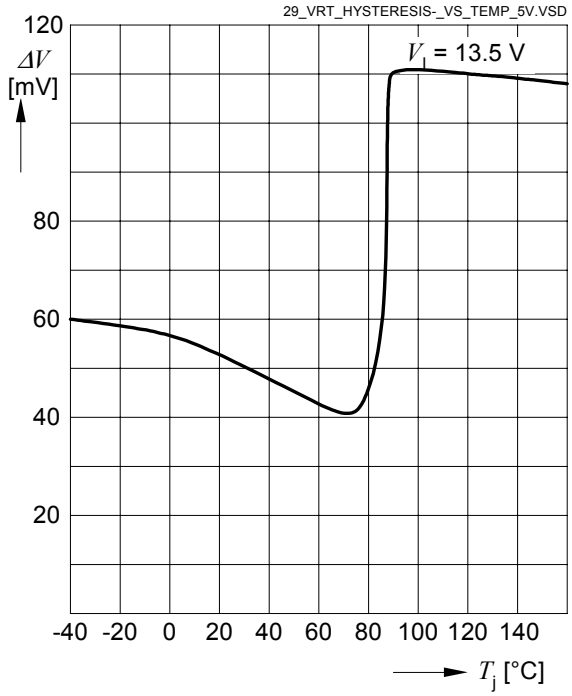
Enable High Level / Low Level Input Voltage $V_{EN,H}$ / $V_{EN,L}$ versus Junction Temperature T_j



Reset Threshold V_{RT} versus Junction Temperature T_j (5V-Version)

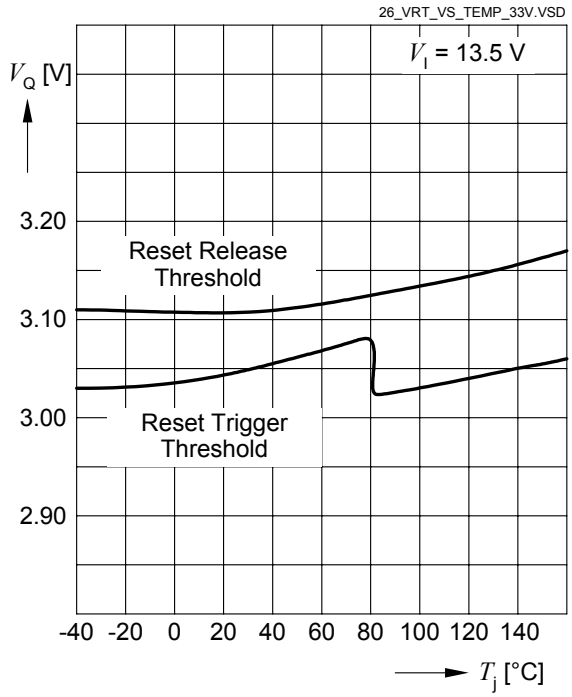


Reset Hysteresis versus Junction Temperature T_j (5V-Version)

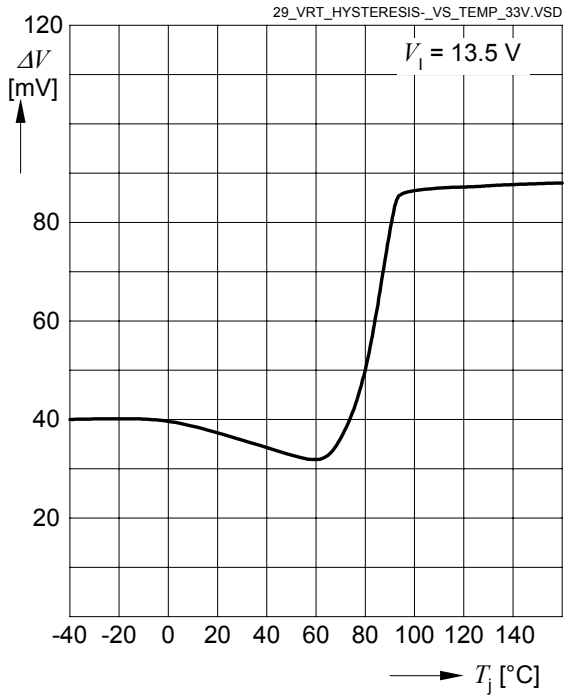


Typical Performance Characteristics (cont´d)

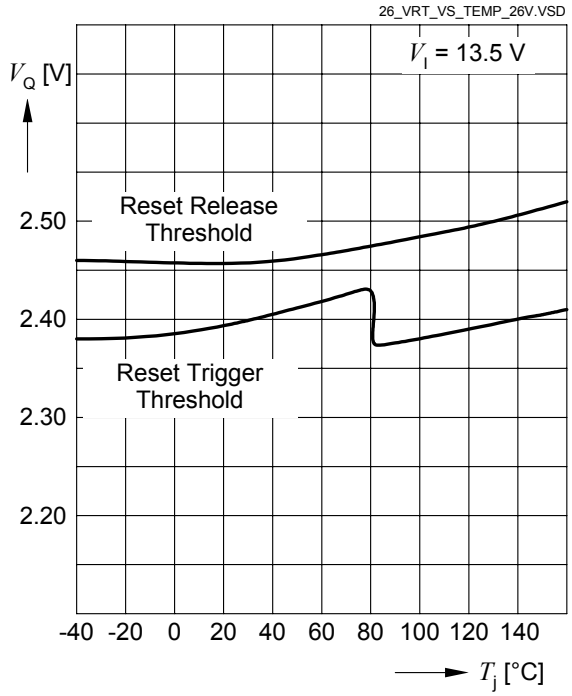
Reset Threshold V_{RT} versus Junction Temperature T_j (3.3V-Version)



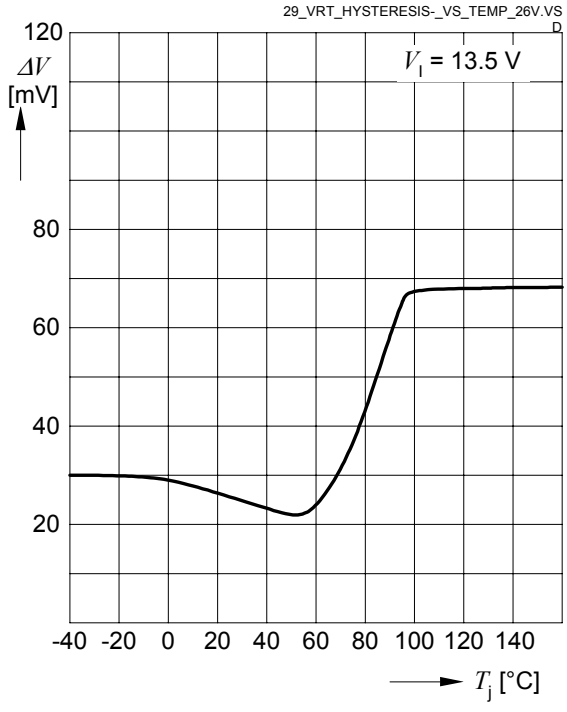
Reset Hysteresis versus Junction Temperature T_j (3.3V-Version)



Reset Threshold V_{RT} versus Junction Temperature T_j (2.6V-Version)

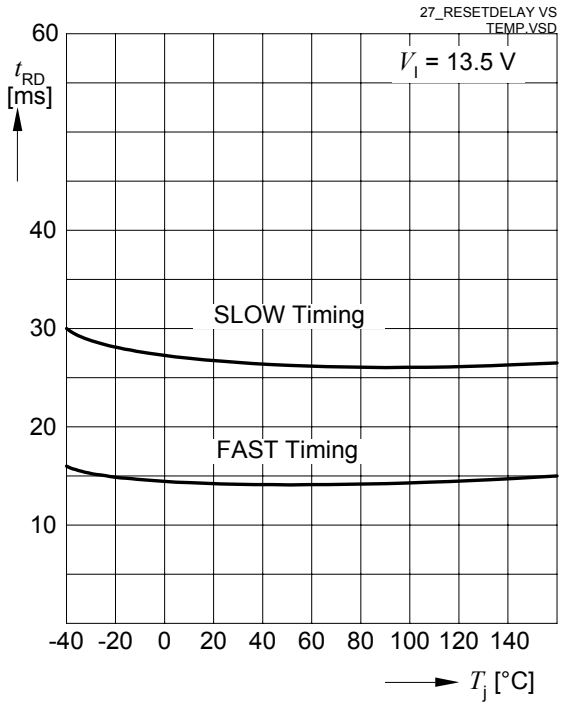


Reset Hysteresis versus Junction Temperature T_j (2.6V-Version)

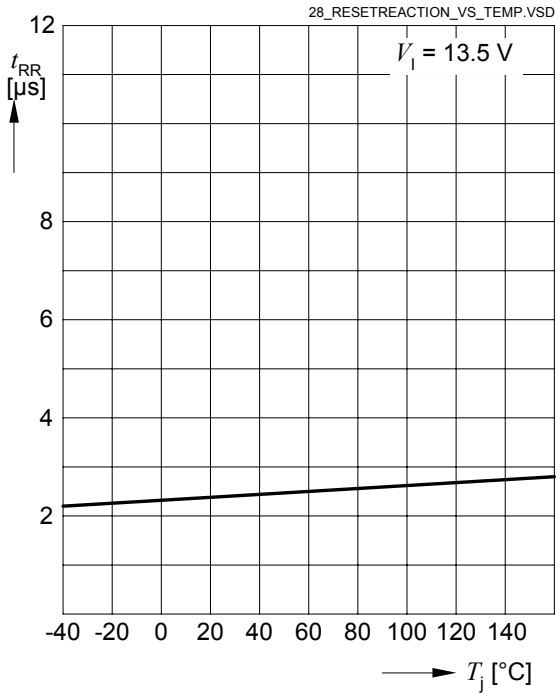


Typical Performance Characteristics (cont´d)

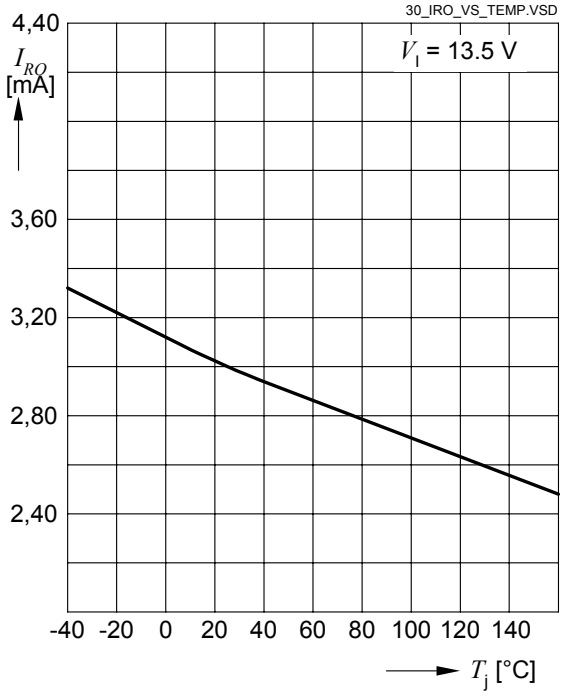
Reset Delay t_{RD} Time versus Junction Temperature T_j



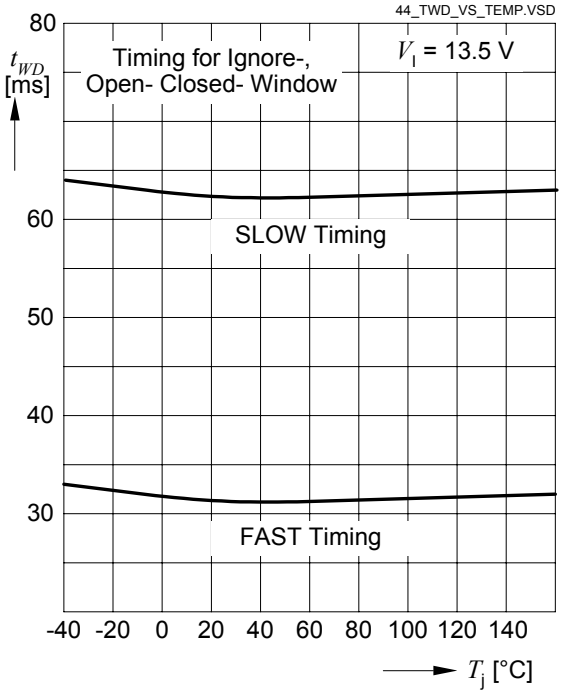
Reset Reaction Time t_{rr} versus Junction Temperature T_j



Reset Output Sink Current I_{RO} versus Junction Temperature T_j

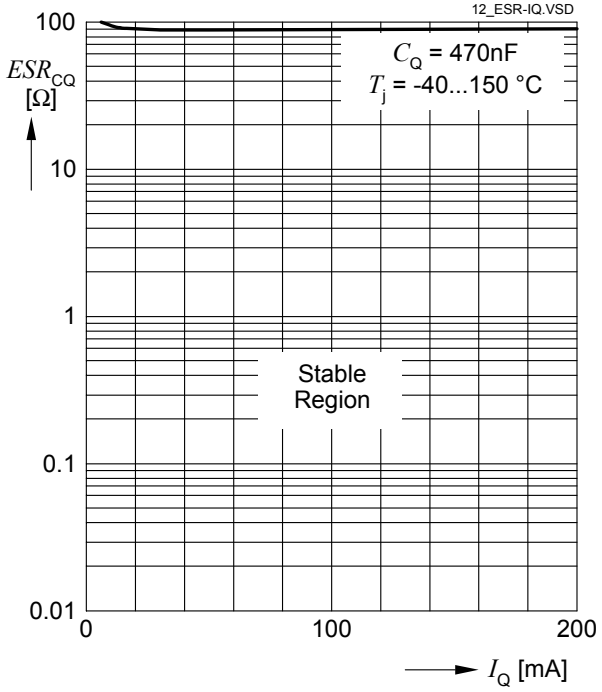


Watchdog Timing t_{WD} versus Junction Temperature T_j



Typical Performance Characteristics (cont´d)

Region of Stability $ESR(C_Q)$ versus Output Current I_Q



6 Package Outlines

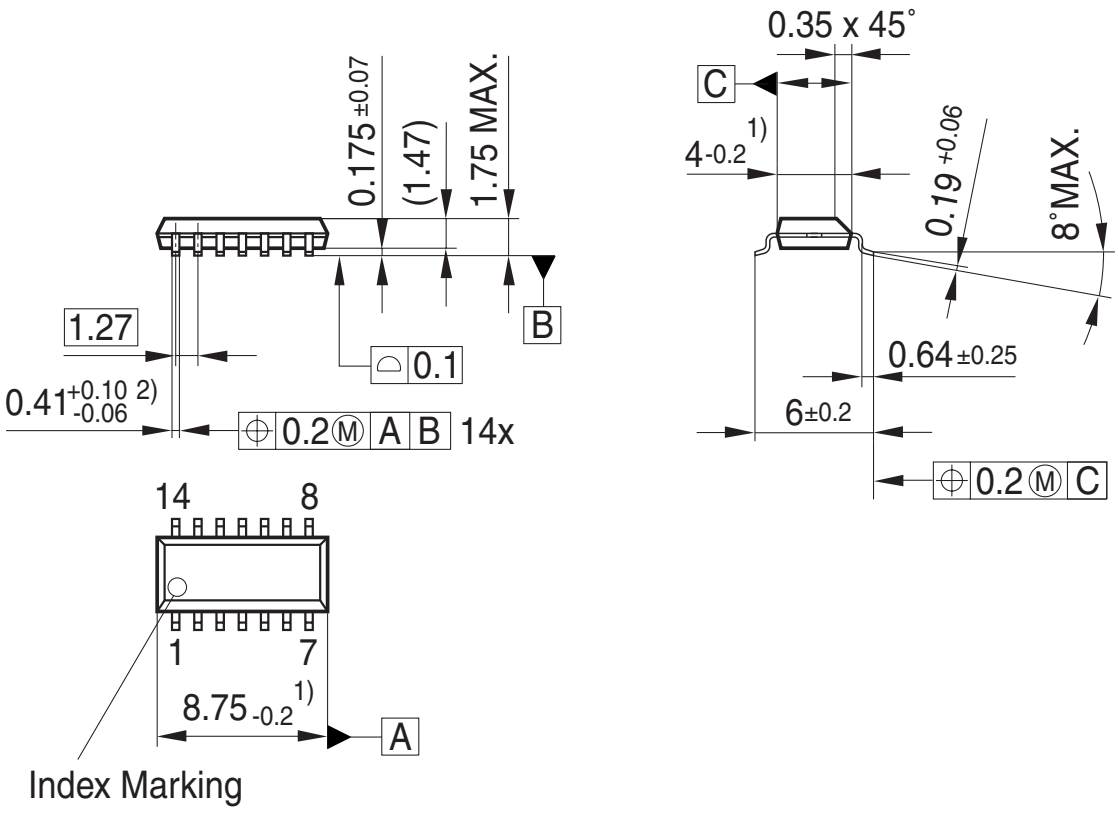


Figure 6 **PG-DSO-14** (Plastic/Plastic Green - Dual Small Outline Package)

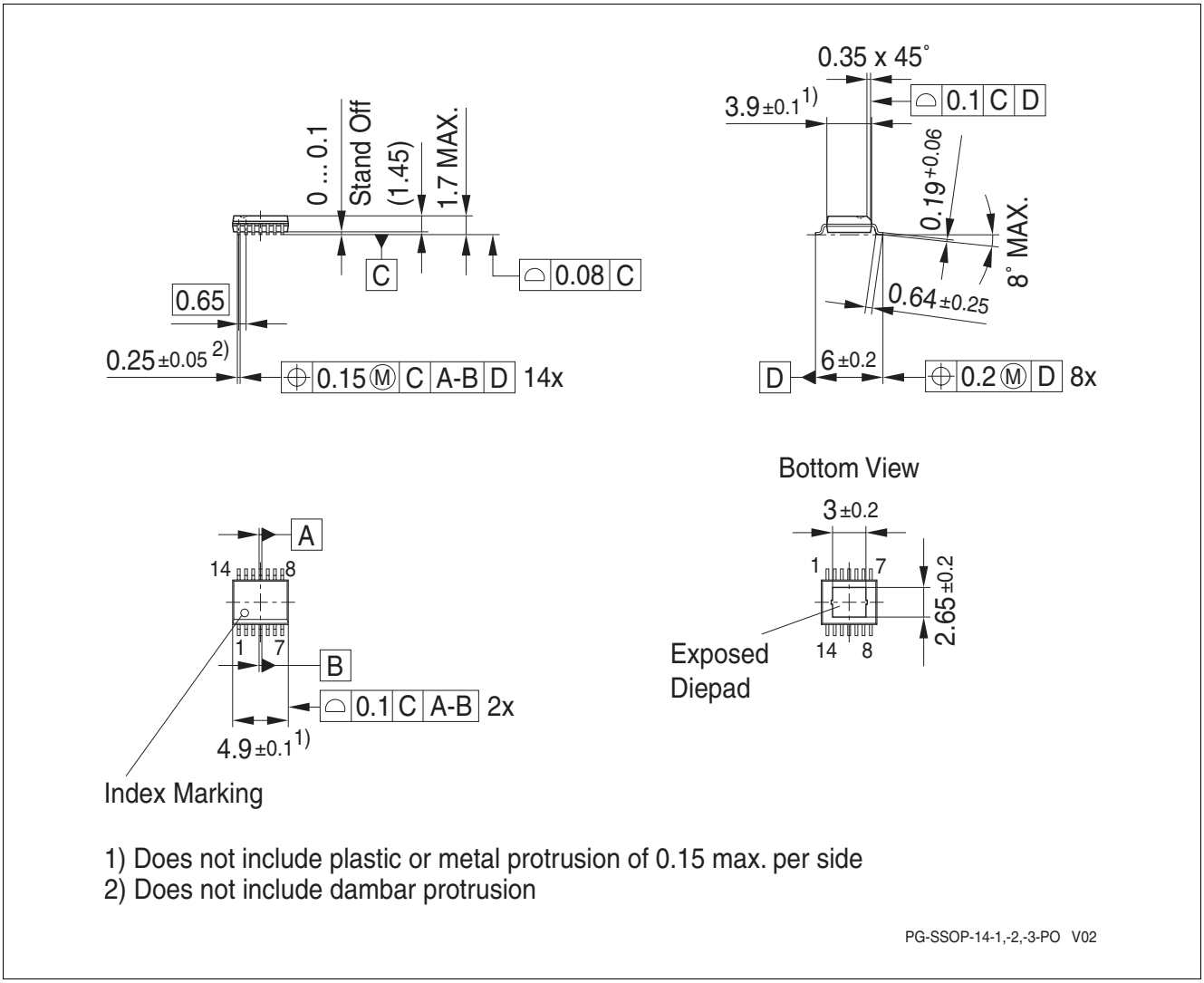


Figure 7 PG-SSOP-14 Exposed Pad

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

7 Revision History

Revision	Date	Changes
1.2	2009-04-28	2.6V version, 5V version in PG-SSOP-14 package and all related description added:
		In **"Features" on Page 2** "or 2.6V" added
		In **"Features" on Page 2** package drawing for PG-DSO-14 updated, package drawing for PG-SSOP-14 added
		In **"Overview" on Page 2** in table at the bottom types "TLE7278-2GV26" and TLE7278-2EV50" added
		In **Table 3.2 "Pin Definitions and Functions (PG-DSO-14)" on Page 4** in description for Pin 1 ", TLE7273-2GV26" added
		In **"Pin Assignment (PG-DSO-14)" on Page 4** "(PG-DSO-14)" added; In **"Pin Definitions and Functions (PG-DSO-14)" on Page 4** "(PG-DSO-14)" added;
		In **Table 3.2 "Pin Definitions and Functions (PG-DSO-14)" on Page 4** in description for pin 8 "; pull down to GND if not needed and turn off the watchdog with WM1 and WM2 pin" added
		"Pin Assignments (PG-SSOP-14 Exposed Pad)" on Page 5 and **"Pin Definitions and Functions (PG-SSOP-14 Exposed Pad)" on Page 5** added
		In **"Functional Range" on Page 7 Item 4.2.3** added, in **Item 4.2.1** ", TLE7278-2EV50" added
		In **Table 4.3 "Thermal Resistance" on Page 7** above **Item 4.3.1** line with "Package PG-DSO-14" and values for PG-SSOP-14 package added: **Item 4.3.6**, **Item 4.3.7**, **Item 4.3.8**, **Item 4.3.9** and **Item 4.3.10** added
		In **"Power On Reset and Reset Output" on Page 8** "and TLE7278-2EV50" in description added
		In **"Electrical Characteristics" on Page 10** all specific items for 2.6V version added: **Item 5.2.5**, **Item 5.2.6**, **Item 5.2.21**, **Item 5.2.25**, **Item 5.2.29**, **Item 5.2.40**, **Item 5.2.42** and **Item 5.2.47** added; In **Item 5.2.36**, **Item 5.2.37**, **Item 5.2.41** and **Item 5.2.50** conditions for 2.6V version added; In **Item 5.2.1**, **Item 5.2.2**, **Item 5.2.8**, **Item 5.2.19**, **Item 5.2.23**, **Item 5.2.27**, **Item 5.2.36**, **Item 5.2.37**, **Item 5.2.38**, **Item 5.2.44**, **Item 5.2.45**, **Item 5.2.49** and **Item 5.2.51** in conditions ", TLE7278-2EV50" added
		In **"Typical Performance Characteristics" on Page 14** Graphs **"Reset Threshold VRT versus Junction Temperature Tj (3.3V-Version)" on Page 18**, **"Reset Hysteresis versus Junction Temperature Tj (3.3V-Version)" on Page 18**, **"Reset Threshold VRT versus Junction Temperature Tj (2.6V-Version)" on Page 18** and **"Reset Hysteresis versus Junction Temperature Tj (2.6V-Version)" on Page 18** added
		In **"Package Outlines" on Page 21** Outlines for PG-SSOP-14 package added: **Figure 7**

Revision	Date	Changes
1.1	2008-07-25	3.3V version and all related description added:
		In **“Features” on Page 2**“ 3.3V” added
		In **“Overview” on Page 2** in table at the bottom type “TLE7273-2GV33” added
		In **“Pin Definitions and Functions (PG-DSO-14)” on Page 4** in description for Pin 1 “TLE7273-2GV33: open drain output;” added
		In **“Functional Range” on Page 7 Item 4.2.2** added
		In **“Power On Reset and Reset Output” on Page 8** description for dimensioning external pull-up resistor at RO added;
		In **“Electrical Characteristics” on Page 10** all specific Items for 3.3V version added: **Item 5.2.3**, **Item 5.2.4**, **Item 5.2.20**, **Item 5.2.24**, **Item 5.2.28**, **Item 5.2.39**, **Item 5.2.41**, **Item 5.2.43**, **Item 5.2.46** and **Item 5.2.50** added; In **Item 5.2.36** and **Item 5.2.37** Conditions for 3.3V version added;
1.0	2008-04-10	final version data sheet

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