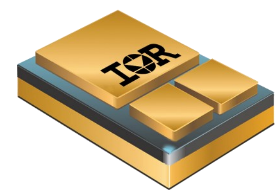
PD-97302G

IRHLNJ797034
JANSR2N7624U3

RADIATION HARDENED
LOGIC LEVEL POWER MOSFET
SURFACE MOUNT (SMD-0.5)

60V, P-CHANNEL
REF: MIL-PRF-19500/757
R7 TECHNOLOGY



SMD-0.5

Product Summary

Part Number	Radiation Level	RDS(on)	I_D	QPL Part Number
IRHLNJ797034	100 kRads(Si)	0.072Ω	-22A*	JANSR2N7624U3
IRHLNJ793034	300 kRads(Si)	0.072Ω	-22A*	JANSF2N7624U3

Description

IR HiRel R7 Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.
The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Features

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Package
- Surface Mount
- Light Weight
- ESD Rating: Class 1C per MIL-STD-750, Method 1020

Absolute Maximum Ratings — Pre-Irradiation

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = -4.5V, T_C = 25°C	Continuous Drain Current	-22*	
I_{D2} @ V_{GS} = -4.5V, T_C = 100°C	Continuous Drain Current	-14.9	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current ①	-88	
P_D @ T_C = 25°C	Maximum Power Dissipation	57	W
	Linear Derating Factor	0.45	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy ②	79	mJ
I_{AR}	Avalanche Current ①	-22	A
E_{AR}	Repetitive Avalanche Energy ①	5.7	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-12.3	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	1.0 (Typical)	g

* Current is limited by package

For Footnotes refer to the page 2.

Pre-Irradiation

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V_{GS} = 0V, I_D = -250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.055	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.072	Ω	V_{GS} = -4.5V, I_{D2} = -14.9A ④
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-2.0	V	V_{DS} = V_{GS}, I_D = -250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	3.5	—	mV/°C	
Gfs	Forward Transconductance	16	—	—	S	V_{DS} = -10V, I_{D2} = -14.9A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	μA	V_{DS} = -48V, V_{GS} = 0V
		—	—	-15		V_{DS} = -48V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -10V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 10V
Q_G	Total Gate Charge	—	—	36	nC	I_{D1} = -22A
Q_{GS}	Gate-to-Source Charge	—	—	10		V_{DS} = -30V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	18		V_{GS} = -4.5V
$t_{d(on)}$	Turn-On Delay Time	—	—	32	ns	V_{DD} = -30V
tr	Rise Time	—	—	250		I_{D1} = -22A
$t_{d(off)}$	Turn-Off Delay Time	—	—	100		R_G = 7.5Ω
t_f	Fall Time	—	—	102		V_{GS} = -5.0V
$L_S + L_D$	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	2261	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	583	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	91	—		f = 1.0MHz
R_G	Gate Resistance	—	—	20	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-22*	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-88		
V_{SD}	Diode Forward Voltage	—	—	-5.0	V	T_J = 25°C, I_S = -22A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	110	ns	T_J = 25°C, I_F = -22A,
Q_{rr}	Reverse Recovery Charge	—	—	132	nC	$V_{DD} \leq$ -50V, di/dt = -100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

* Current is limited by package

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	2.2	°C/W

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = -25V, starting T_J = 25°C, L = 0.32mH, Peak I_L = -22A, V_{GS} = -10V

③ $I_{SD} \leq$ -22A, di/dt $\leq$ -350A/μs, $V_{DD} \leq$ -60V, $T_J \leq$ 150°C

④ Pulse width $\leq$ 300 μs; Duty Cycle $\leq$ 2%

⑤ Total Dose Irradiation with V_{GS} Bias. -10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑥ Total Dose Irradiation with V_{DS} Bias. -48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	Up to 300 kRads (Si)[1]		Units	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	——	V	V_{GS} = 0V, I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	-2.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate-to-Source Leakage Forward	——	-100	nA	V_{GS} = -10V
I_{GSS}	Gate-to-Source Leakage Reverse	——	100	nA	V_{GS} = 10V
I_{DSS}	Zero Gate Voltage Drain Current	——	-1.0	μA	V_{DS} = -48V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	——	0.076	Ω	V_{GS} = -4.5V, I_{D2} = -14.9A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (SMD-0.5)	——	0.072	Ω	V_{GS} = -4.5V, I_{D2} = -14.9A
V_{SD}	Diode Forward Voltage ④	——	-5.0	V	V_{GS} = 0V, I_S = -22A

[1] Part numbers IRHLNJ797034 (JANSR2N7624U3) and IRHLNJ793034 (JANSF2N7624U3)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm²))	Energy (MeV)	Range (μm)	V_{DS} (V)					
			@VGS= 0V	@VGS= 2V	@VGS= 4V	@VGS= 5V	@VGS= 6V	@VGS= 7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	-60	-60	-60	-60	-60	-40
62 ± 5%	355 ± 7.5%	33 ± 7.5%	-60	-60	-60	-60	-60	——
85 ± 5%	380 ± 10%	29± 7.5%	-60	-60	-60	-60	——	——

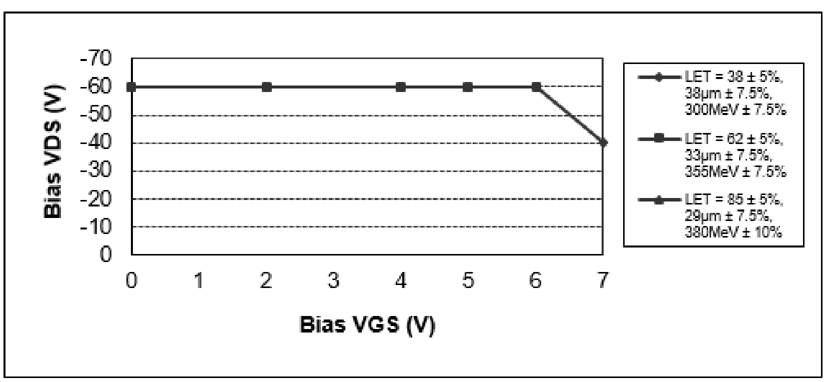


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

Pre-Irradiation

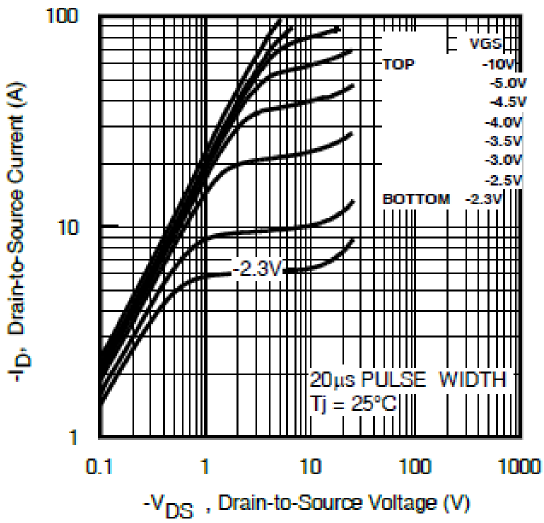


Fig 1. Typical Output Characteristics

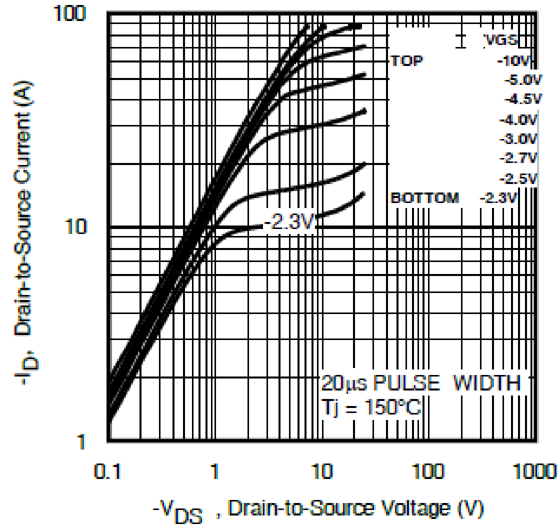


Fig 2. Typical Output Characteristics

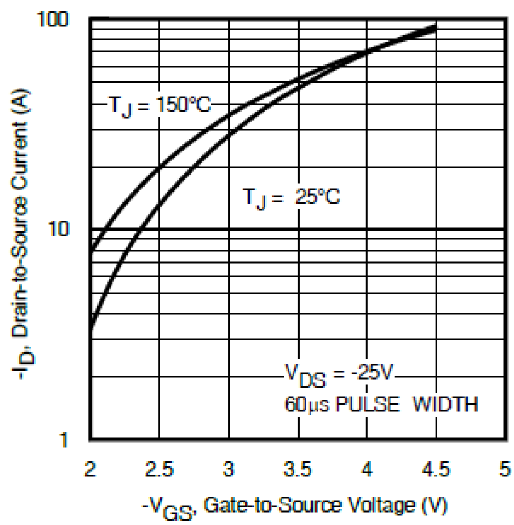


Fig 3. Typical Transfer Characteristics

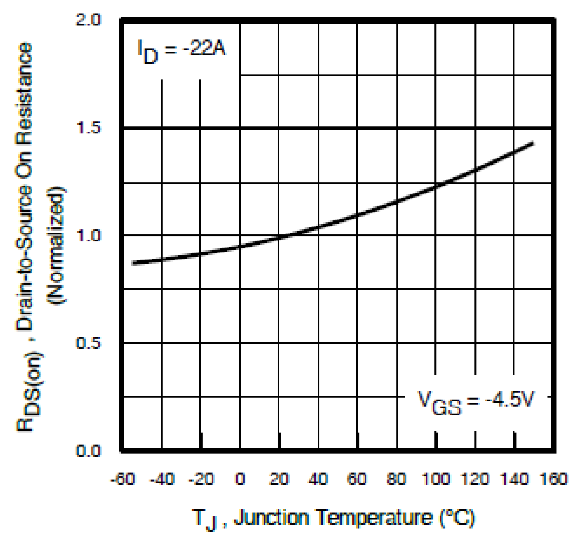


Fig 4. Normalized On-Resistance Vs. Temperature

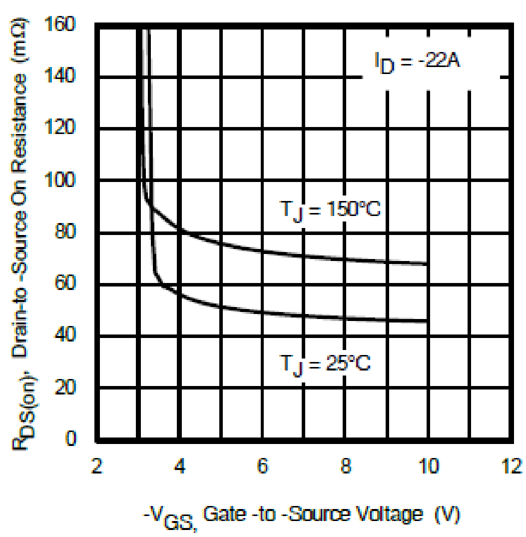


Fig 5. Typical On-Resistance Vs Gate Voltage

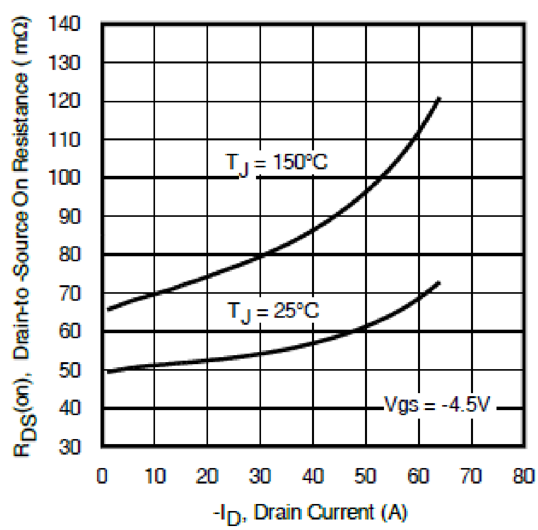


Fig 6. Typical On-Resistance Vs Drain Current

Pre-Irradiation

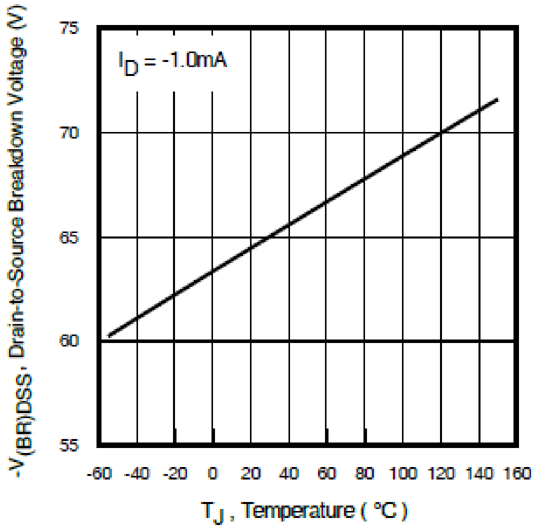


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

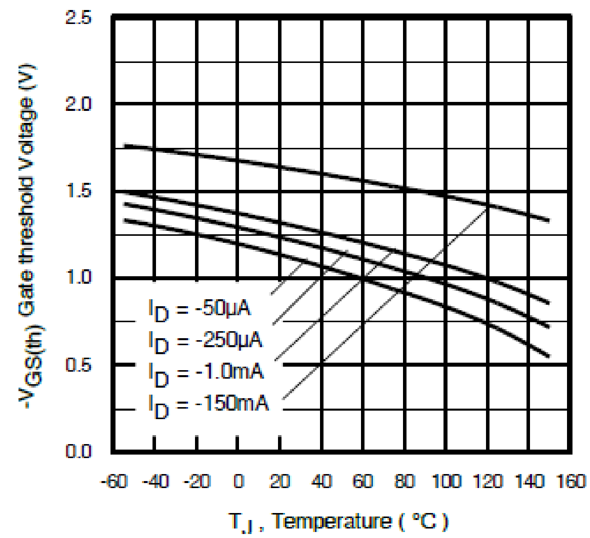


Fig 8. Typical Threshold Voltage Vs Temperature

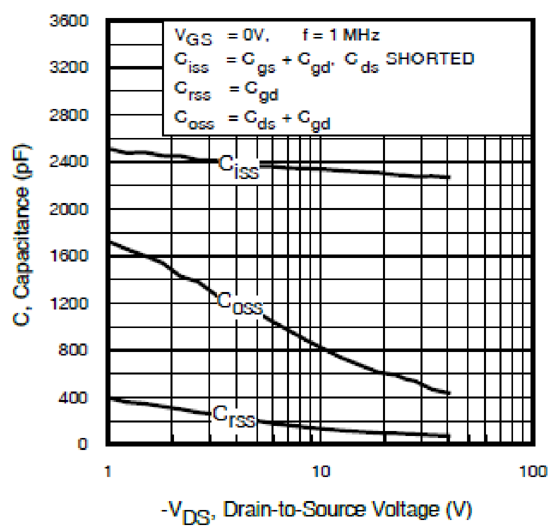


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

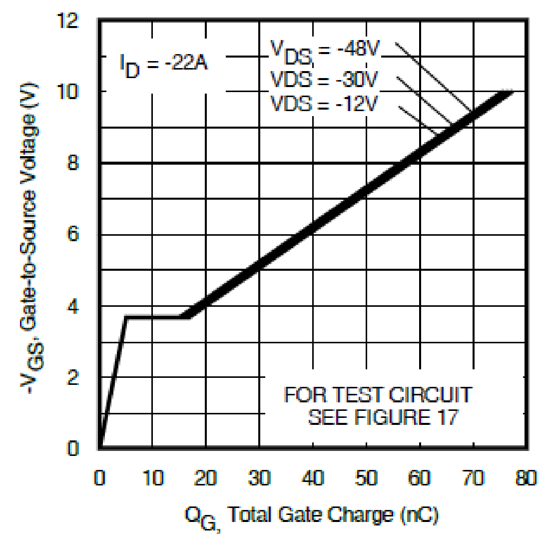


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

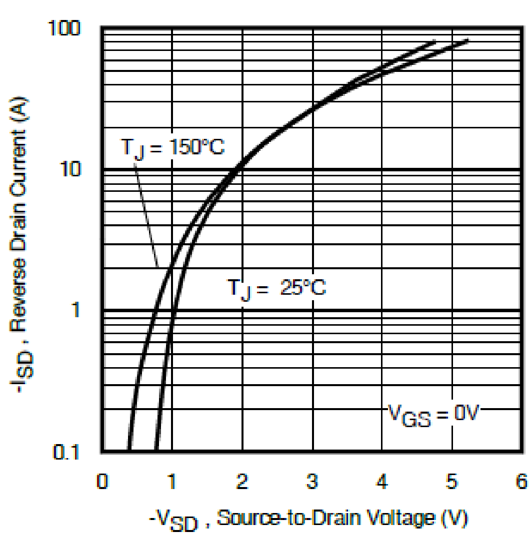


Fig 11. Typical Source-to-Drain Diode Forward Voltage

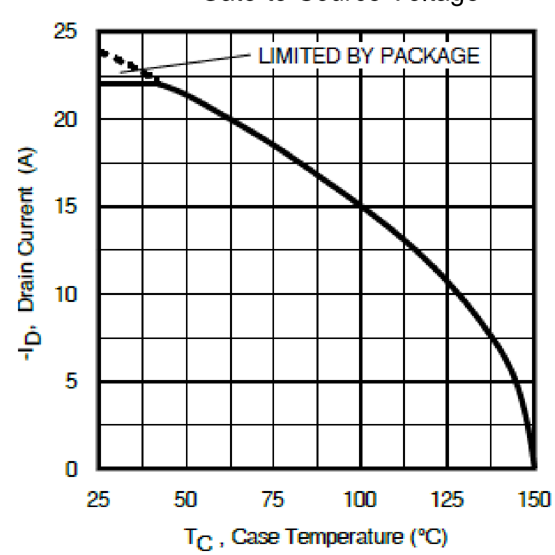


Fig 12. Maximum Drain Current Vs. Case Temperature

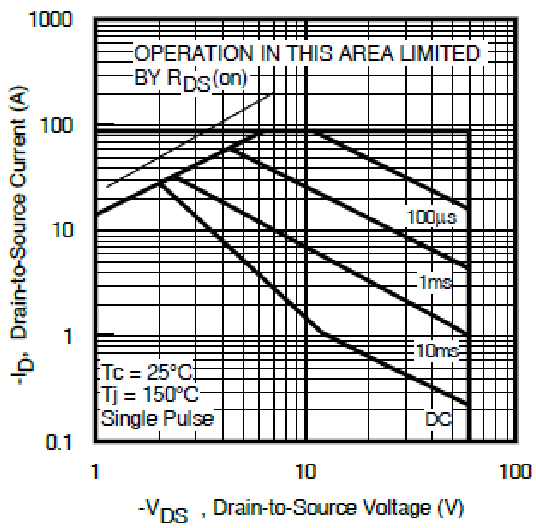


Fig 13. Maximum Safe Operating Area

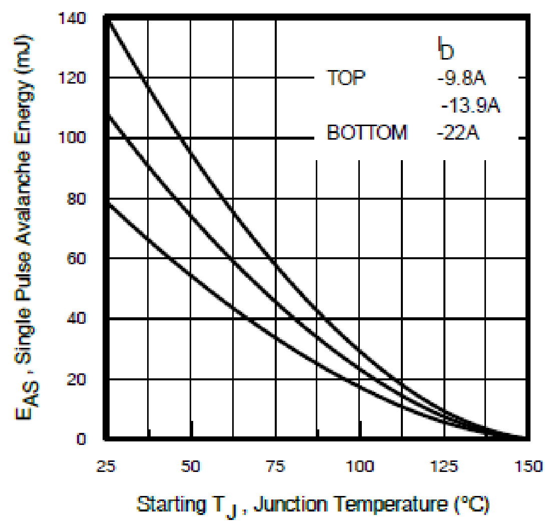


Fig 14. Maximum Avalanche Energy Vs. Drain Current

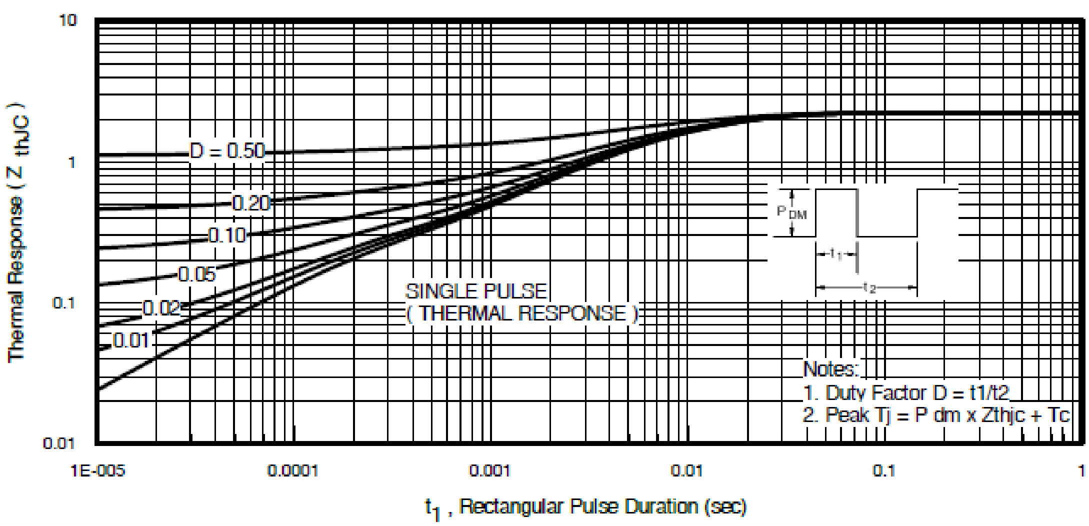


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

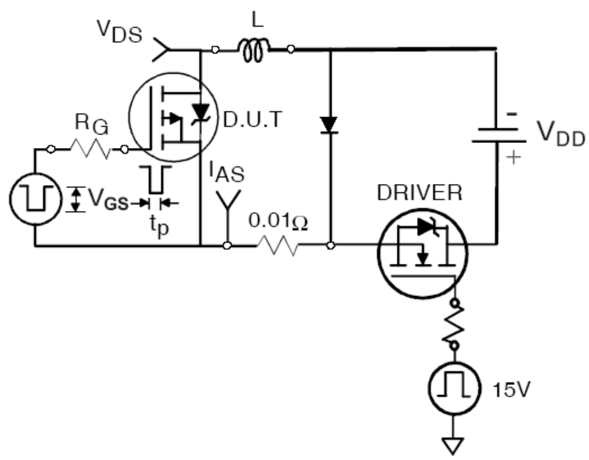


Fig 16a. Unclamped Inductive Test Circuit

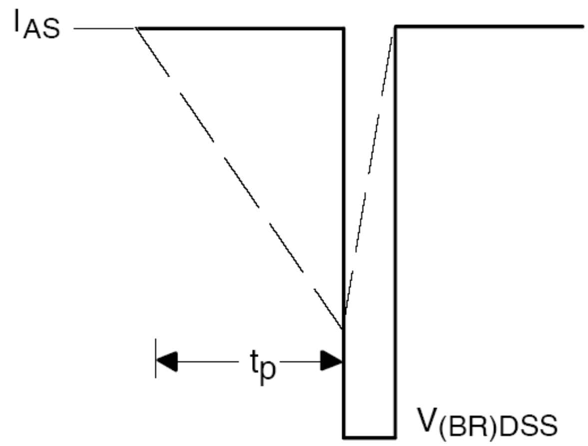


Fig 16b. Unclamped Inductive Wave-

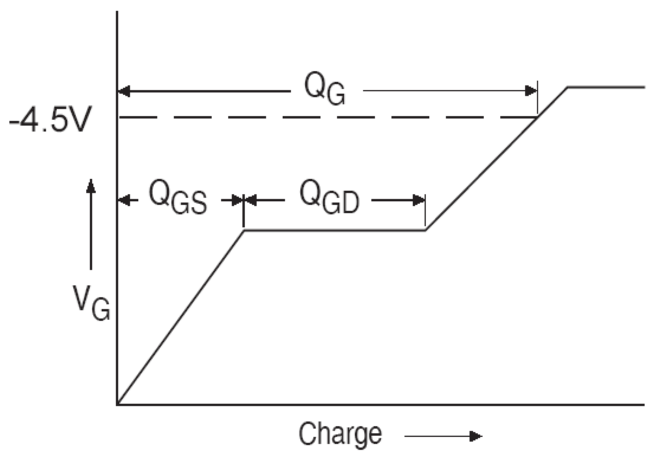


Fig 17a. Basic Gate Charge Waveform

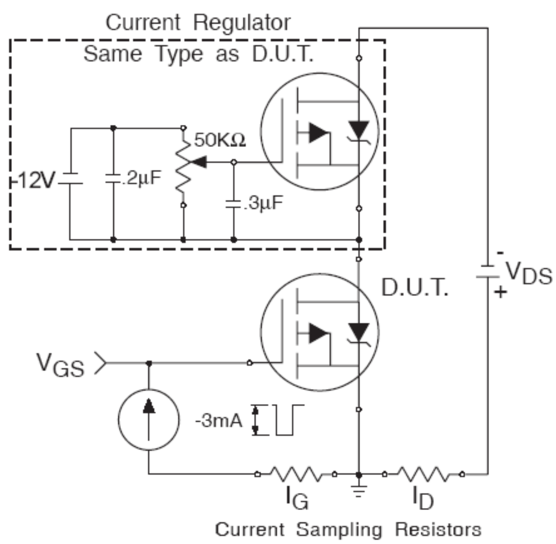


Fig 17b. Gate Charge Test Circuit

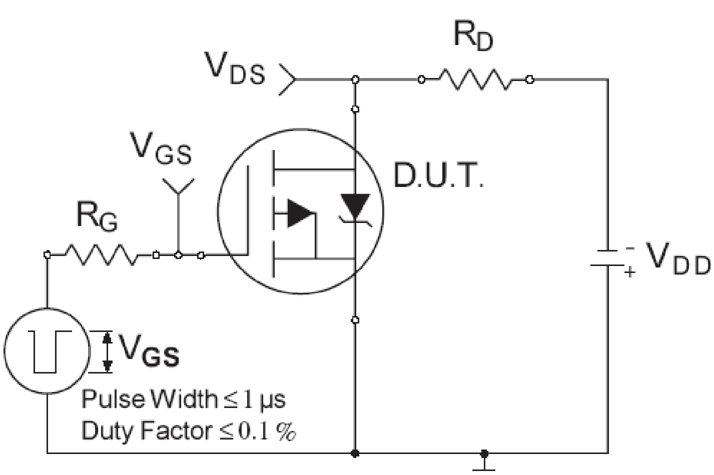


Fig 18a. Switching Time Test Circuit

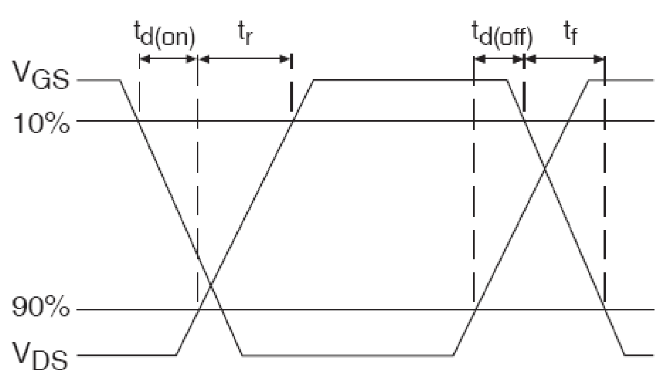
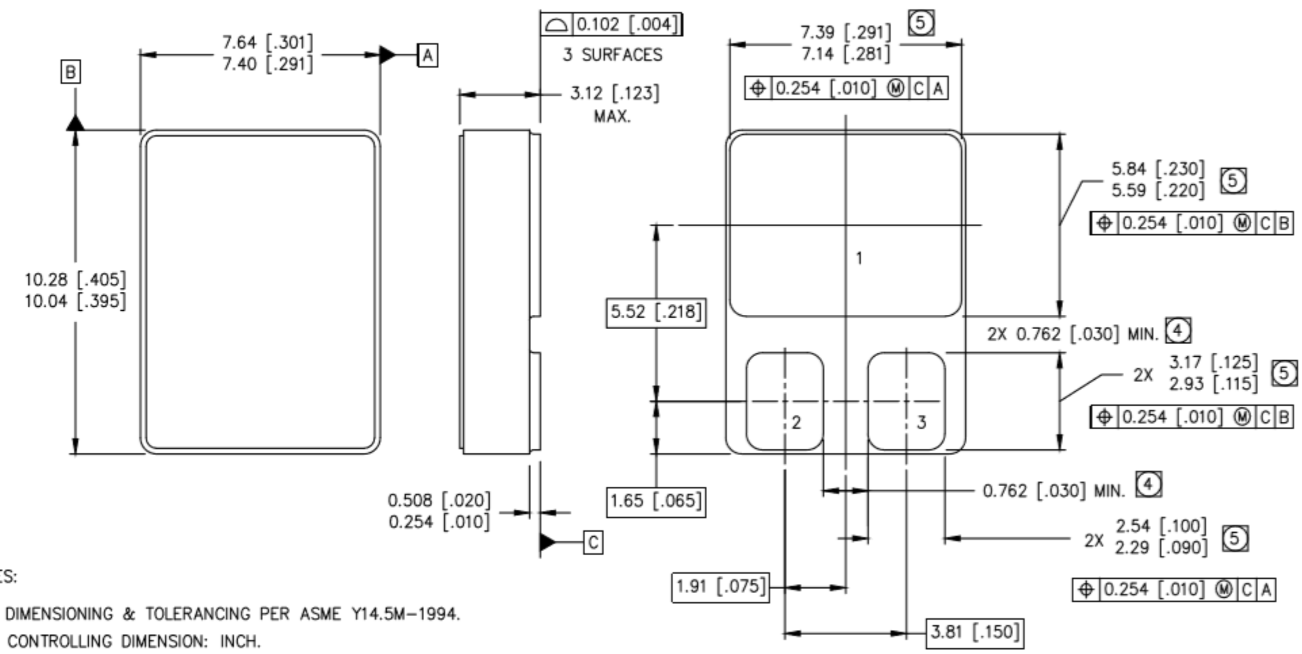


Fig 18b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: [SMD – 0.5]

Case Outline and Dimensions - SMD-0.5

REV.	DESCRIPTION	ECN	DATE
B	INITIAL RELEASE	1120_ER6904	4-3-20



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. DIMENSION INCLUDES METALLIZATION FLASH.
5. DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.
6. STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb.

PAD ASSIGNMENTS

MOSFET

1 = DRAIN
2 = GATE
3 = SOURCE

IOR HiRel
An Infineon Technologies Company

TITLE: SMD–0.5 OUTLINE	
DRAWING NO. D100724G–WEB	REV B

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