

# MOSFET

Metal Oxide Semiconductor Field Effect Transistor

## OptiMOS™

OptiMOS™ 5 Power-Transistor, 80 V  
IPB049N08N5

## Data Sheet

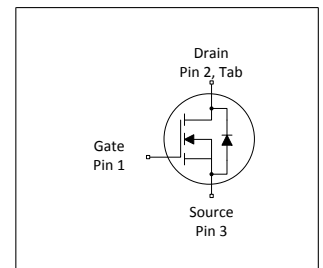
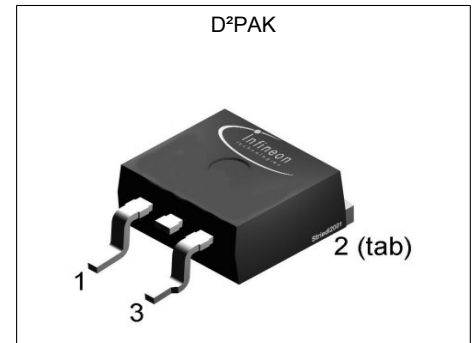
Rev. 2.0  
Final

Power Management & Multimarket

## 1 Description

### Features

- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	80	V
$R_{DS(on),max}$	4.9	m $\Omega$
$I_D$	80	A
$Q_{oss}$	51	nC
$Q_G(0V..10V)$	42	nC



Type / Ordering Code	Package	Marking	Related Links
IPB049N08N5	PG-TO 263-3	049N08N5	-

<sup>1)</sup> J-STD20 and JESD22



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## 2 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	80	A	$T_C=25\text{ °C}$ $T_C=100\text{ °C}$
Pulsed drain current <sup>1)</sup>	$I_{D,pulse}$	-	-	320	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	-	-	84	mJ	$I_D=80\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	125	W	$T_C=25\text{ °C}$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

## 3 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	0.9	1.2	K/W	-
Thermal resistance, junction - ambient, minimal footprint	$R_{thJA}$	-	-	62	K/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>3)</sup>	$R_{thJA}$	-	-	40	K/W	-
Soldering temperature, wave and reflow soldering are allowed	$T_{sold}$	-	-	260	°C	reflow MSL1

<sup>1)</sup> See figure 3 for more detailed information

<sup>2)</sup> See figure 13 for more detailed information

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

## 4 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}$ , $I_D=66\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=80\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=80\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	1	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	4.3 5.7	4.9 6.6	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=80\text{ A}$ $V_{GS}=6\text{ V}$ , $I_D=40\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	1.1	1.7	$\Omega$	-
Transconductance	$g_{fs}$	52	104	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=80\text{ A}$

**Table 5 Dynamic characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	2900	3770	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=40\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	490	637	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=40\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{riss}$	-	23	40	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=40\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	17	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=80\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	7	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=80\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	27	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=80\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	7	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=80\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	15	-	nC	$V_{DD}=40\text{ V}$ , $I_D=80\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	-	9.4	14	nC	$V_{DD}=40\text{ V}$ , $I_D=80\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	16	-	nC	$V_{DD}=40\text{ V}$ , $I_D=80\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	42	53	nC	$V_{DD}=40\text{ V}$ , $I_D=80\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.2	-	V	$V_{DD}=40\text{ V}$ , $I_D=80\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	36	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	51	68	nC	$V_{DD}=40\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test.

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	80	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	320	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.98	1.2	V	$V_{GS}=0\text{ V}, I_F=80\text{ A}, T_J=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	56	112	ns	$V_R=40\text{ V}, I_F=80\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	92	184	nC	$V_R=40\text{ V}, I_F=80\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test.

## 5 Electrical characteristics diagrams

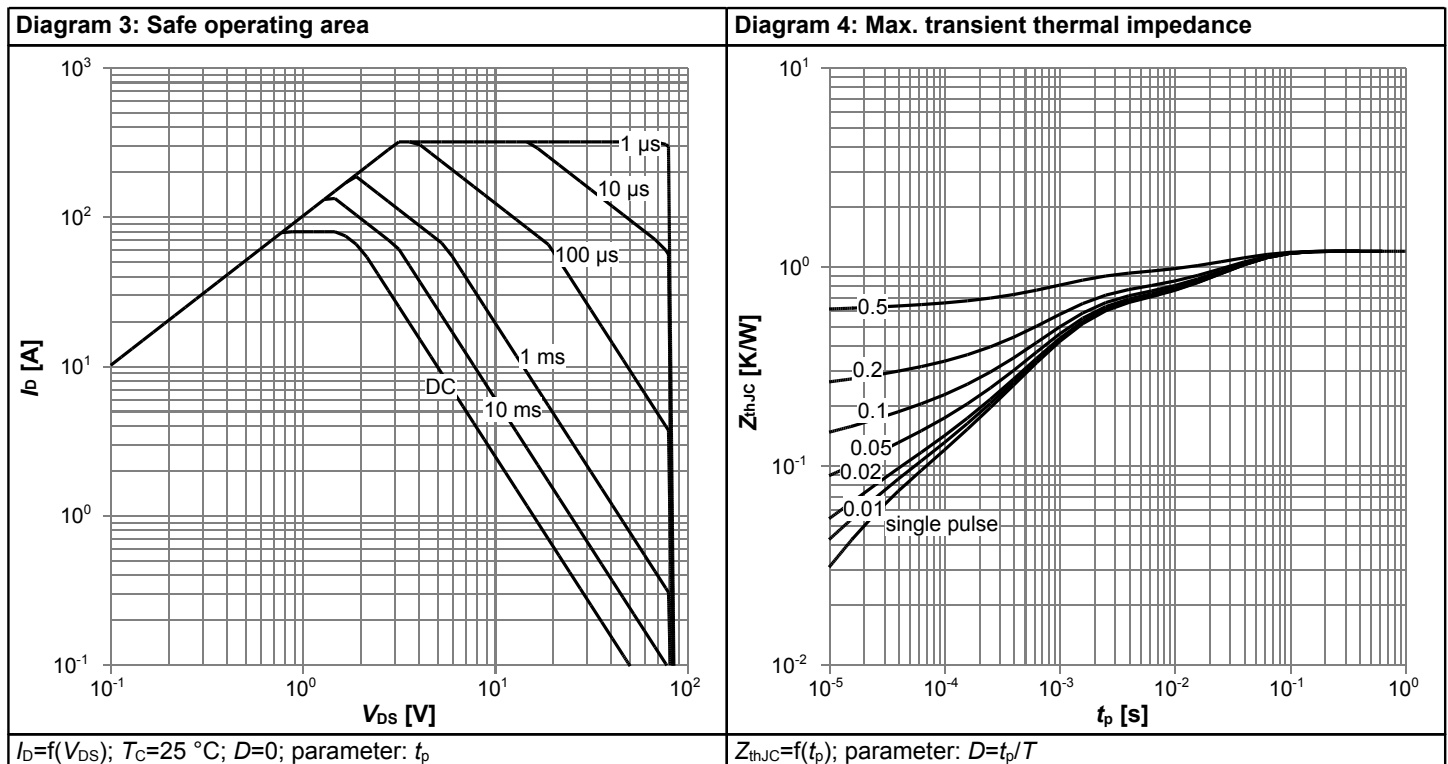
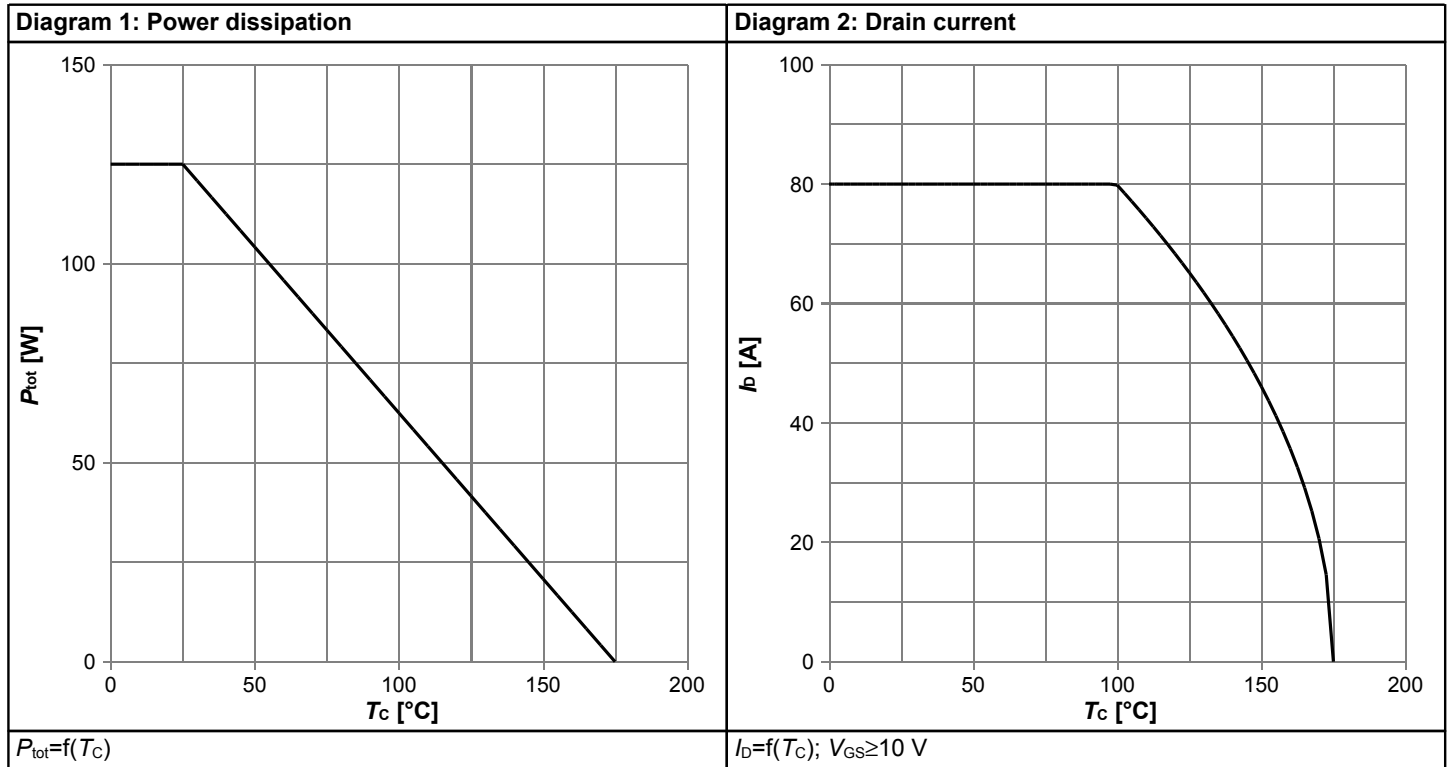
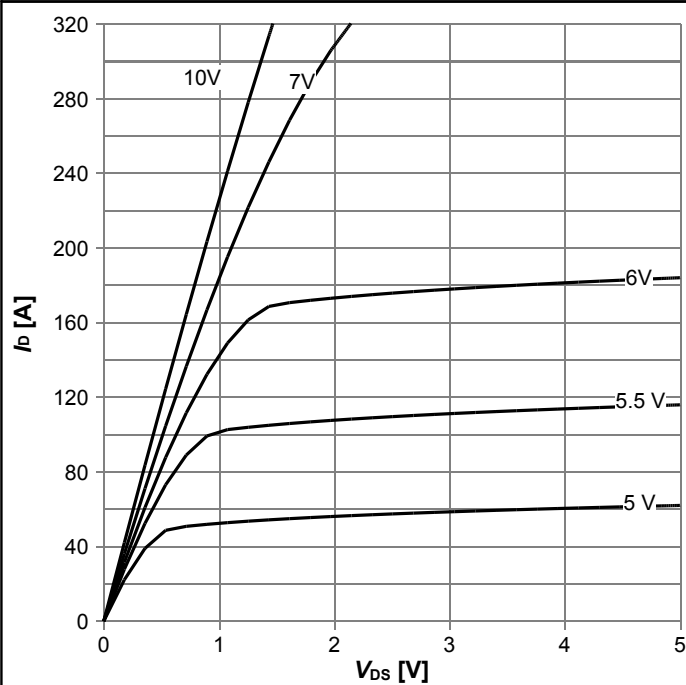
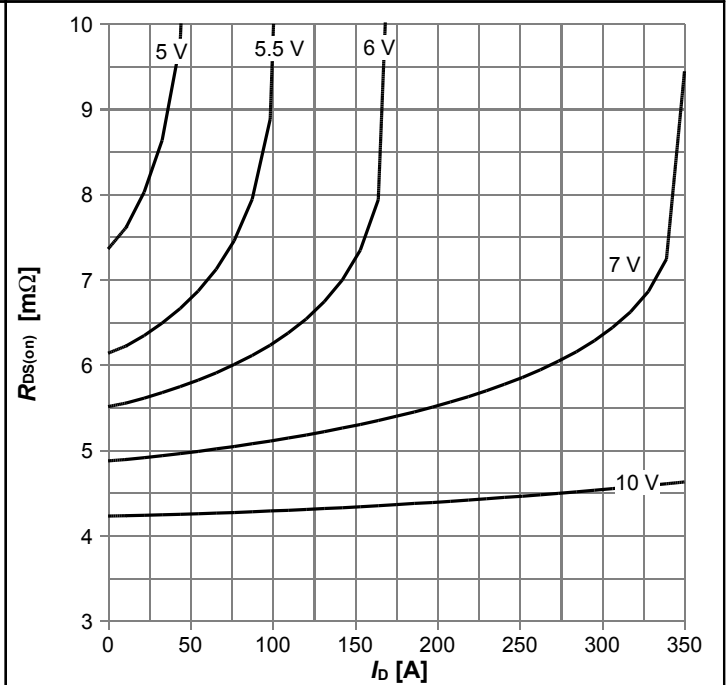


Diagram 5: Typ. output characteristics



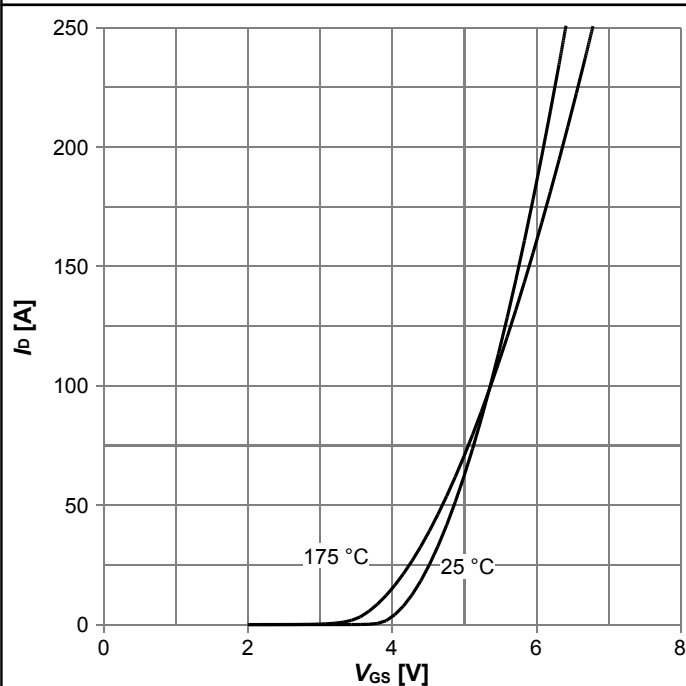
$I_D = f(V_{DS}); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



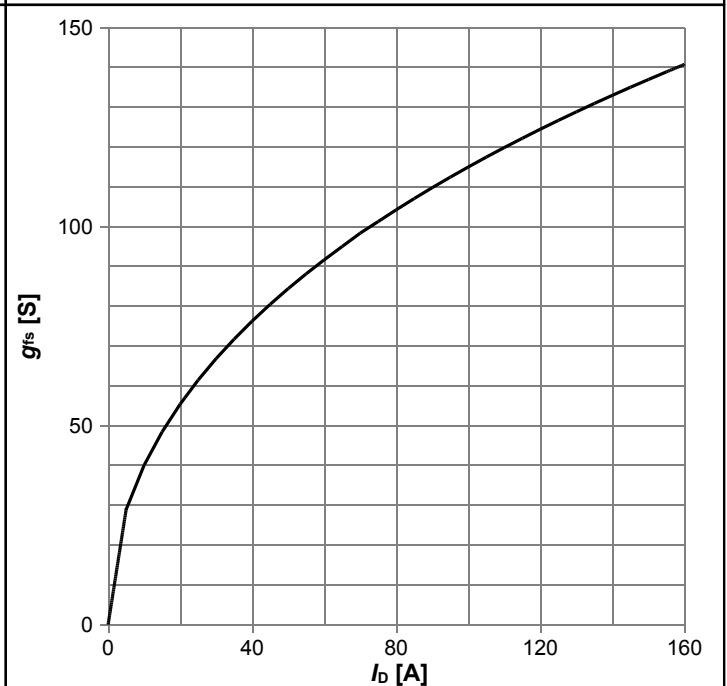
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

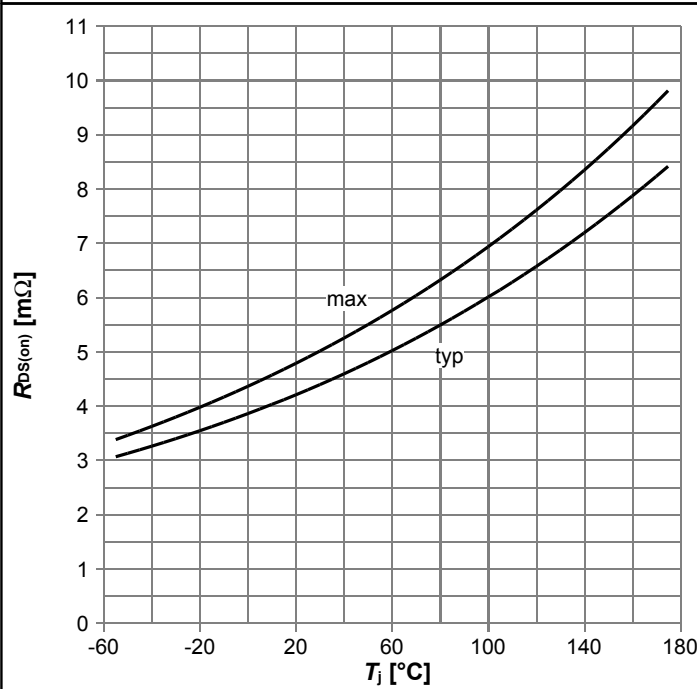
Diagram 8: Typ. forward transconductance



$g_{fs} = f(I_D); T_j = 25\text{ °C}$

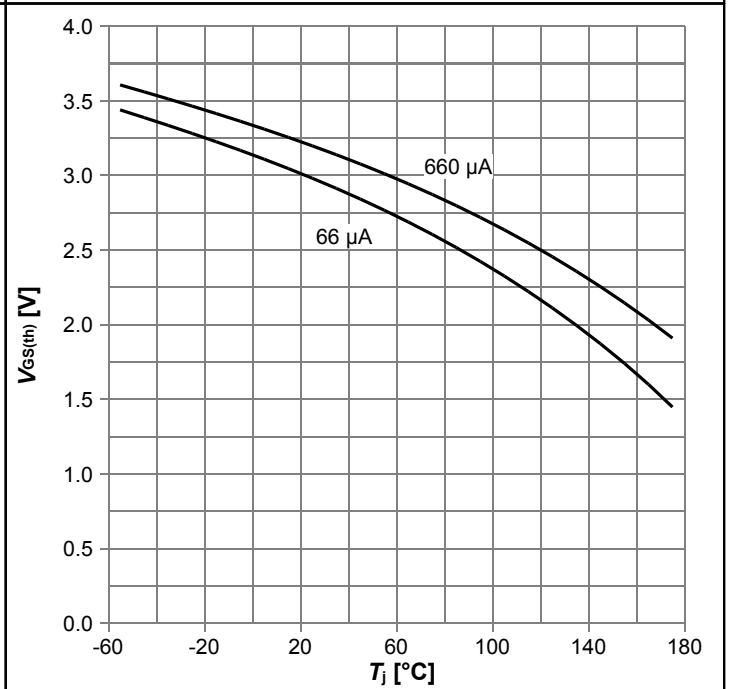


Diagram 9: Drain-source on-state resistance



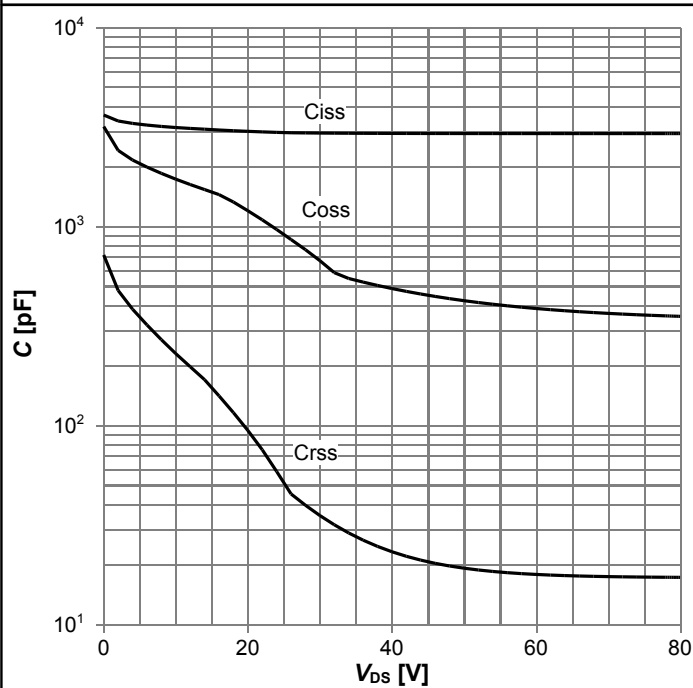
$R_{DS(on)}=f(T_j)$ ;  $I_D=80$  A;  $V_{GS}=10$  V

Diagram 10: Typ. gate threshold voltage



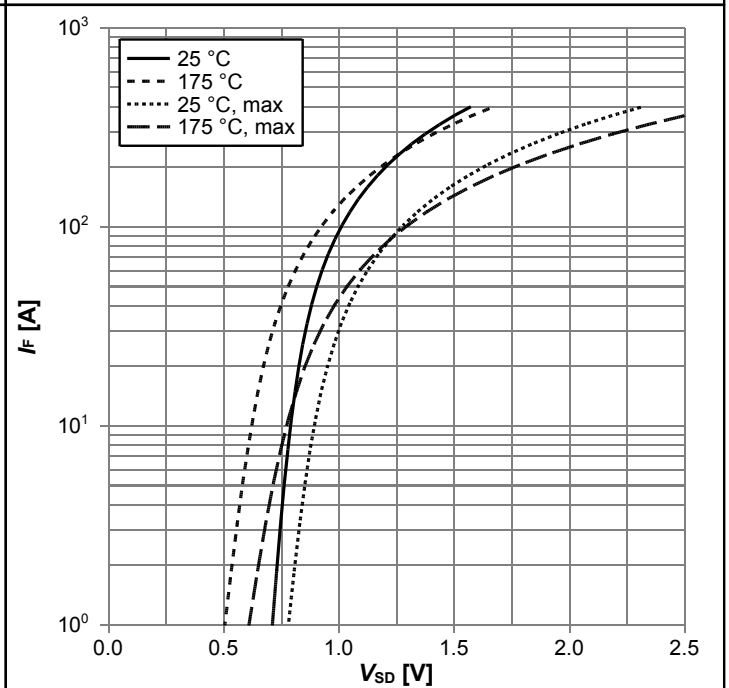
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



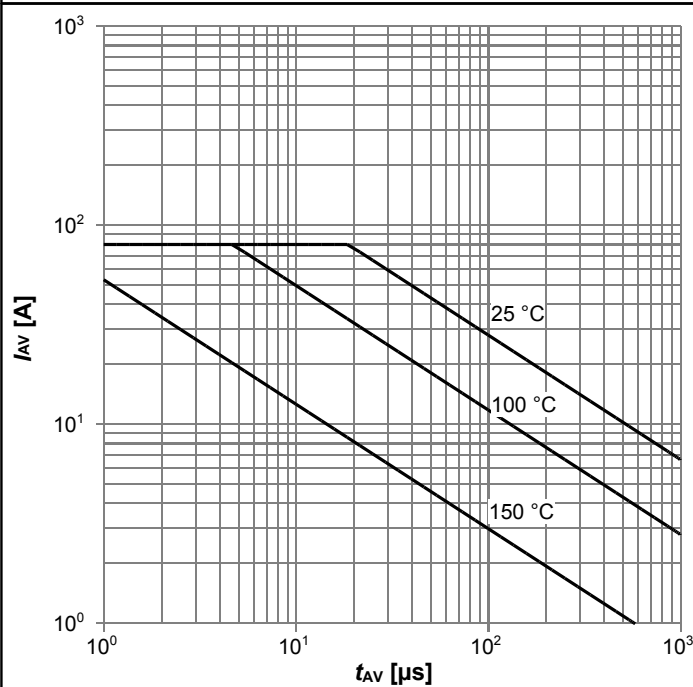
$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

Diagram 12: Forward characteristics of reverse diode



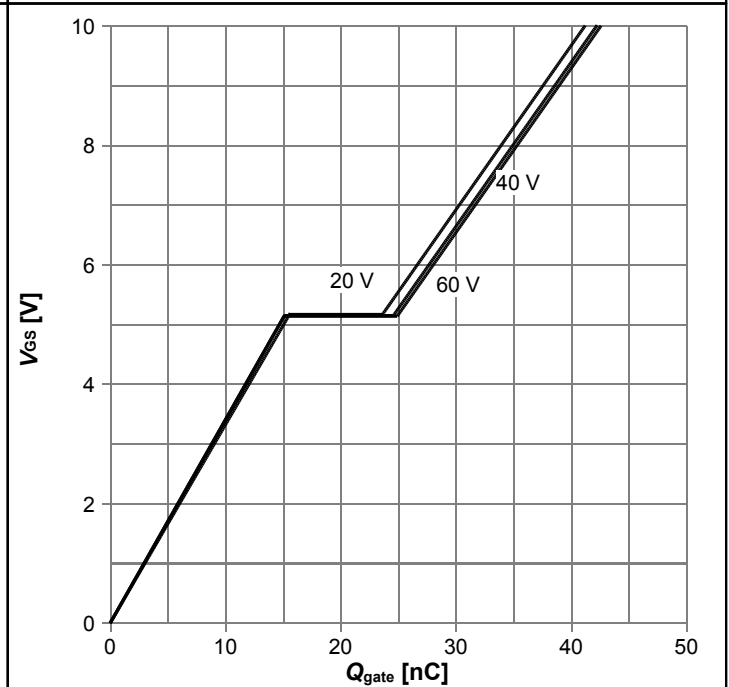
$I_F=f(V_{SD})$ ; parameter:  $T_j$

Diagram 13: Avalanche characteristics



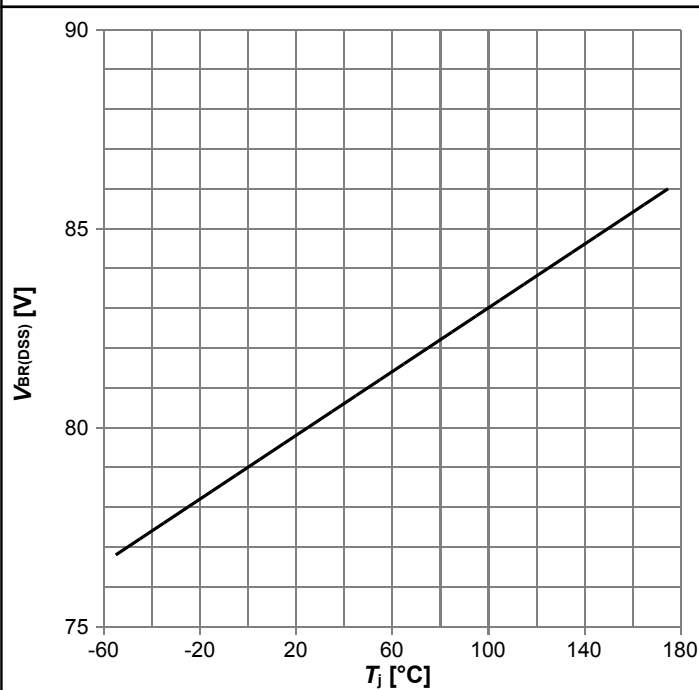
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

Diagram 14: Typ. gate charge



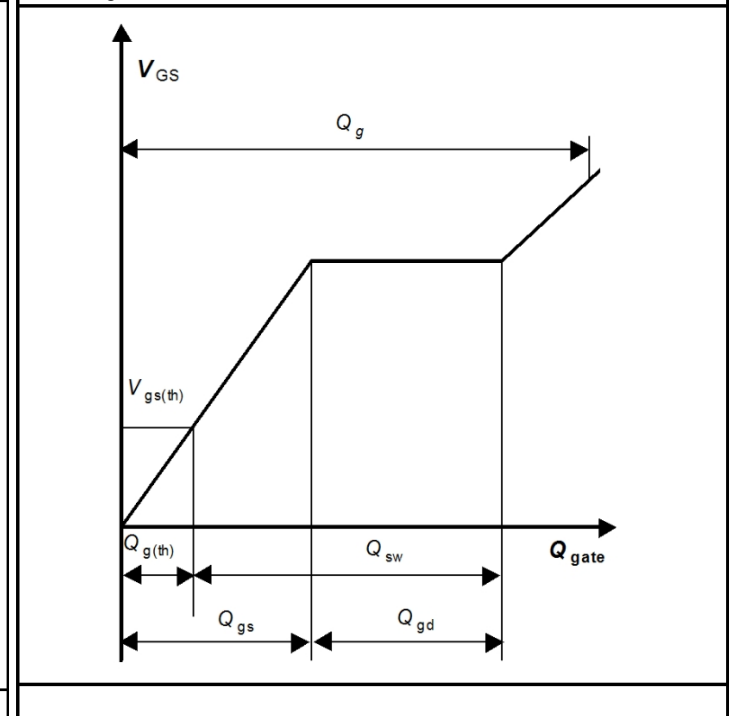
$V_{GS}=f(Q_{gate}); I_D=80$  A pulsed; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage

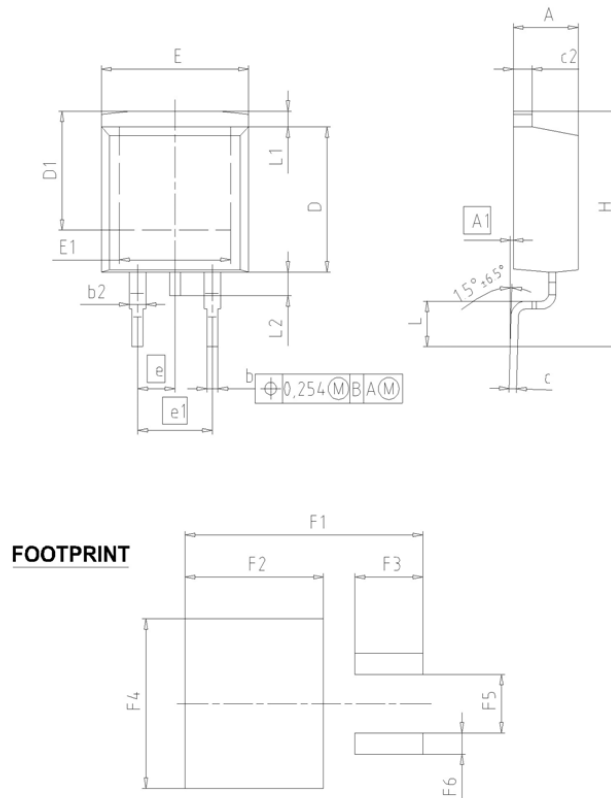


$V_{BR(DSS)}=f(T_j); I_D=1$  mA

Gate charge waveforms



## 6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	2		2	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	3.65	3.85	0.144	0.152
F6	1.25	1.45	0.049	0.057

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Z8B00003324

SCALE  
0 5 5  
7.5mm

EUROPEAN PROJECTION



ISSUE DATE  
30-08-2007

REVISION  
01

Figure 1 Outline PG-TO 263-3, dimensions in mm/inches

## Revision History

IPB049N08N5

**Revision: 2014-12-17, Rev. 2.0**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-12-17	Release of final version

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