50mA Linear Voltage Regulator with Ultra Low Quiescent Current and Adjustable Output Voltage

IFX30081LDV

Industrial Linear Voltage Regulator

Data Sheet

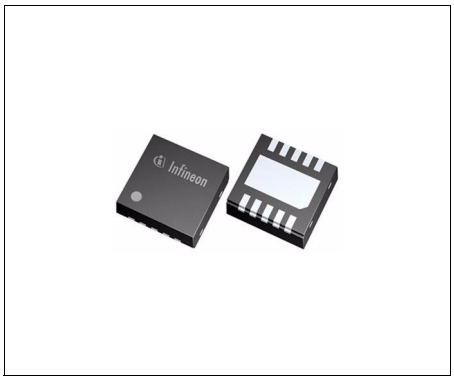
Rev.1.0, 2016-03-11

Standard Power

IFX30081LDV

RoHS

1 Overview



PG-TSON-10

Features

- Ultra Low Quiescent Current of typ. 5 µA
- Wide Input Voltage Range of 2.75 V to 42 V
- Output Current Capability up to 50 mA
- Shutdown Current less than 1 µA
- Low Drop Out Voltage of typ. 100mV @ 50mA
- Output Current Limit Protection
- Over temperature Shutdown
- Enable Feature
- PG-TSON-10 package supports Automated Optical Inspection
- Wide temperature range -40°C ≤ T_j ≤ 125°C
- Green Product (RoHS compliant)

Applications

- Battery Operated Systems
- Sensor Supplies
- Smoke and Fire Detectors

Description

The IFX30081LDV is a wide input voltage, low drop out voltage and ultra low quiescent current linear voltage regulator. The IFX30081LDV is available in a tiny PG-TSON-10 package which also enables Automated Optical Inspection (AOI).

With a wide input voltage range of 2.75 V to 42 V and ultra low quiescent current of only 5 µA this regulator is perfectly suitable for battery operated systems as well as supplies for sensors.

The IFX30081LDV is available with an adjustable output voltage with an accuracy of 2 % and maximum output current up to 50 mA.

The regulation concept implemented in the IFX30081LDV combines fast regulation and very good stability while requiring only a small ceramic capacitor of 1 µF at the output.

Internal protection features like output current limitation and over temperature shutdown are implemented to protect the device against failures like output short circuit to GND, over-current and over-temperature. The device can be switched on and off by the enable feature. When the device is switched off, the current consumption is less than 1 µA.

Type	Package	Marking
IFX30081LDV	PG-TSON-10	381LDV

Overview

Choosing External Components

An input capacitor C_{IN} is recommended to compensate line influences. The output capacitor C_{OUT} is necessary for the stability of the regulating circuit. Stability is guaranteed at values $C_{OUT} \geq 1\mu F$ and an ESR $\leq 100\ \Omega$ within the whole operating range.

The qualification of this product is based on JEDEC JESD47 and may reference existing qualification results of similar products. Such referring is justified by structural similarity of the products. The product is not qualified and manufactured according to the requirements of Infineon Technologies with regard to automotive and/or transportation applications. Infineon Technologies administrates a comprehensive quality management system according to the latest version of the ISO9001 and ISO/TS 16949. The most updated certificates of the aforesaid ISO9001 and ISO/TS 16949 are available on the Infineon Technologies webpage http://www.infineon.com/cms/en/product/technology/quality/

2 Block Diagram

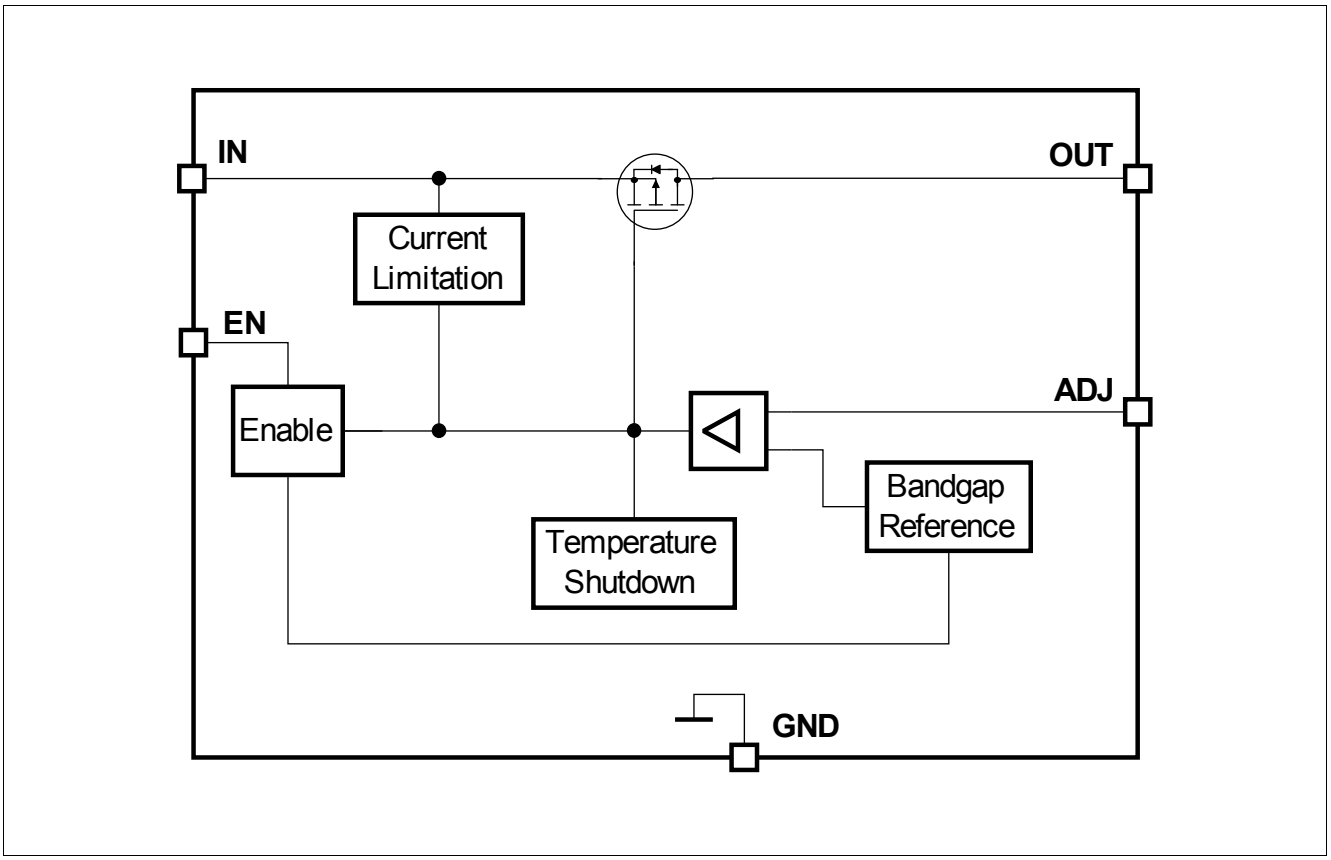


Figure 1 Block Diagram IFX30081LDV

3 Pin Configuration

3.1 Pin Assignment in PG-TSON-10 Package

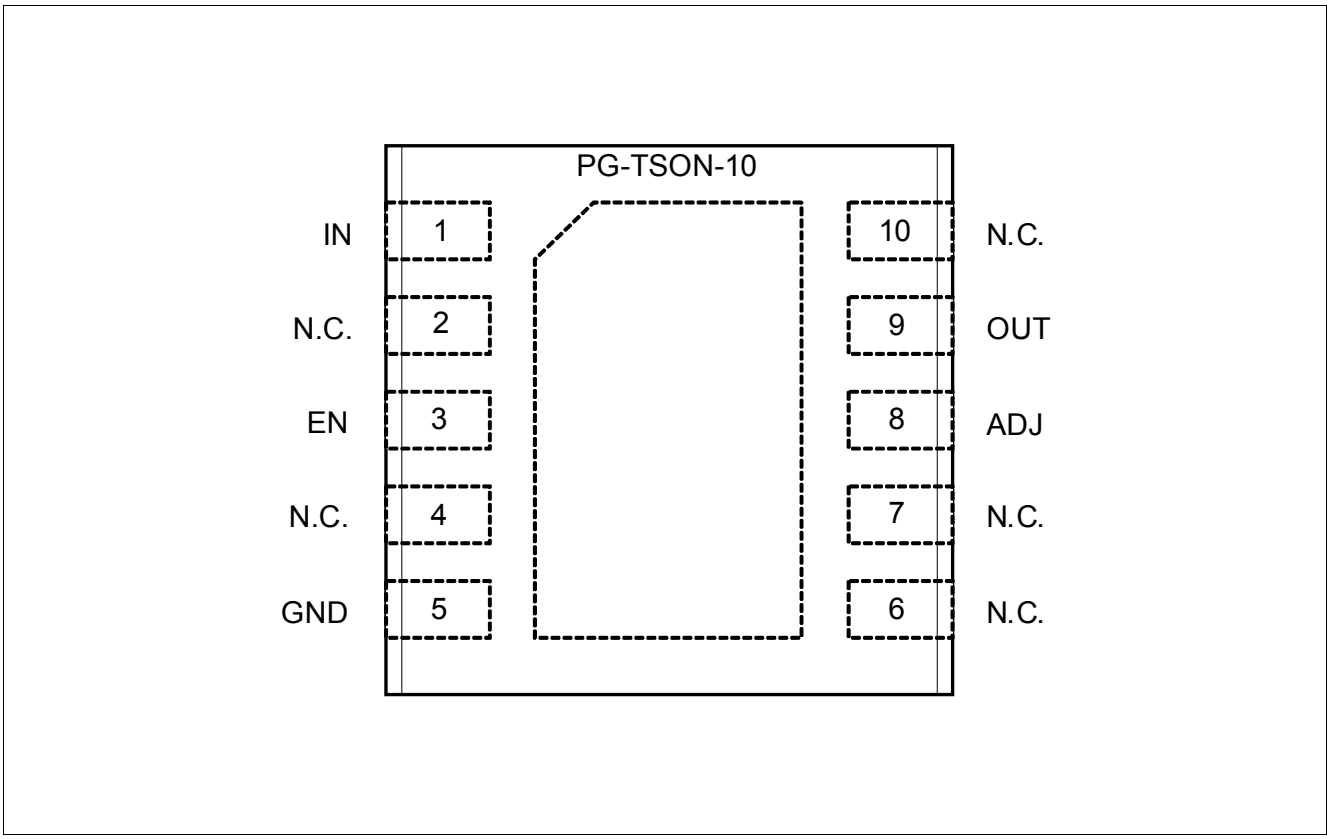


Figure 2 Pin Configuration IFX30081LDV in PG-TSON-10 package

3.2 Pin Definitions and Functions in PG-TSON-10 Package

Pin	Symbol	Function
1	IN	**Input** Compensating line influences by placing a small ceramic capacitor (e.g. 100 nF), to GND, close to the IC terminals is recommended.
2	N.C.	**Not Connected**
3	EN	**Enable** (Integrated pull-down resistor) Enable the IC with high level input signal. Disable the IC with low level input signal.
4	N.C.	**Not Connected**
5	GND	**Ground**

Pin Configuration

Pin	Symbol	Function
6	N.C.	**Not Connected**
7	N.C.	**Not Connected**
8	ADJ	**Voltage Adjustment** Connect an external voltage divider to set the desired output voltage.
9	OUT	**Output** Connect an output capacitor C_{OUT} to GND close to the IC's terminals, respecting the values specified for its capacitance and ESR in Table 2 "Functional Range" on Page 8.
10	N.C.	**Not Connected**
Exposed Pad	–	Connect to heatsink area. Connect to GND.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40 °C to +125 °C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input IN, Enable EN							
Voltage	V_{IN}; V_{EN}	-0.3	–	45	V	–	P_4.1.1
Output OUT, Voltage Adjustment ADJ							
Voltage	V_{OUT}	-0.3	–	45	V	–	P_4.1.2
Voltage	V_{ADJ}	-0.3	–	7	V	–	P_4.1.3
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.4
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.5
ESD Absorption							
ESD Absorption	$V_{ESD,HBM}$	-2	–	2	kV	HBM[2)]	P_4.1.6
ESD Absorption	$V_{ESD,CDM}$	-750	–	750	V	CDM[3)] at all pins	P_4.1.7

1) Not subject to production testing, specified by design.
2) ESD susceptibility, HBM Test according to ANSI/ESDA/JEDEC JS-001 (1.5kOhm, 100pF).
3) ESD susceptibility, Charged Device Model “CDM” according to JEDEC JESD22-C101

Note:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage Range	V_{IN}	$V_{OUT,nom}$ + V_{dr}	–	42	V	–[1]	P_4.2.1
Extended Input Voltage Range	$V_{IN,ext}$	2.75	–	42	V	–[2]	P_4.2.2
Output Voltage Adjustable Range	V_{OUT}	1.2	–	V_{IN} - V_{dr}	V	V_{IN} < 42 V	P_4.2.7
Enable Voltage Range	V_{EN}	0	–	42	V	–	P_4.2.3
Output Capacitor	C_{OUT}	1	–	–	µF	–[3]	P_4.2.4
Output Capacitor's ESR	ESR(C_{OUT})	–	–	100	Ω	–[4]	P_4.2.5
Junction temperature	T_j	-40	–	125	°C	–	P_4.2.6

1) Output current is limited internally and depends on the input voltage, see Electrical Characteristics for more details.
2) Between min. value and $V_{OUT,nom}$ + V_{dr}: V_{OUT} = V_{IN}- V_{dr}. Below min. value: V_{OUT} can drop down to 0 V.
3) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.
4) Relevant ESR value at f = 10 kHz.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 3 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	13	–	K/W	–	P_4.3.1
Junction to Ambient	R_{thJA}	–	60	–	K/W	2s2p board[2)]	P_4.3.2
Junction to Ambient	R_{thJA}	–	188	–	K/W	footprint only[3)]	P_4.3.3
Junction to Ambient	R_{thJA}	–	76	–	K/W	300 mm^2 heatsink area on PCB[3)]	P_4.3.4
Junction to Ambient	R_{thJA}	–	64	–	K/W	600 mm^2 heatsink area on PCB[3)]	P_4.3.5

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with two inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Wherever applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with one inner copper layers (1 x 70µm Cu)

5 Block Description and Electrical Characteristics

5.1 Voltage Regulation

The output voltage V_{OUT} is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and drives the pass transistor accordingly.

The control loop stability depends on the output capacitor C_{OUT}, the load current, the chip temperature and the internal circuit design. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in "Functional Range" on Page 8 have to be maintained. For further details please refer to the typical performance graph "Output Capacitor Series Resistor ESR(C_{OUT}) versus Output Current I_{OUT}" on Page 13. Since the output capacitor is used to buffer load steps, it should be sized according to the application's needs.

An input capacitor C_{IN} is not required for stability, but is recommended to compensate line fluctuations. An additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the regulator terminals.

In order to prevent overshoots during start-up, a smooth ramping up function is implemented. This ensures almost no overshoots during start-up, mostly independent from load and output capacitance.

Whenever the load current exceeds the specified limit, e.g. in case of a short circuit, the output current is limited and the output voltage decreases.

The over temperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuit) by switching off the power stage. After the chip has cooled down, the regulator restarts. This oscillatory thermal behavior causes the junction temperature to exceed the 150° C maximum and significantly reducing the IC's life.

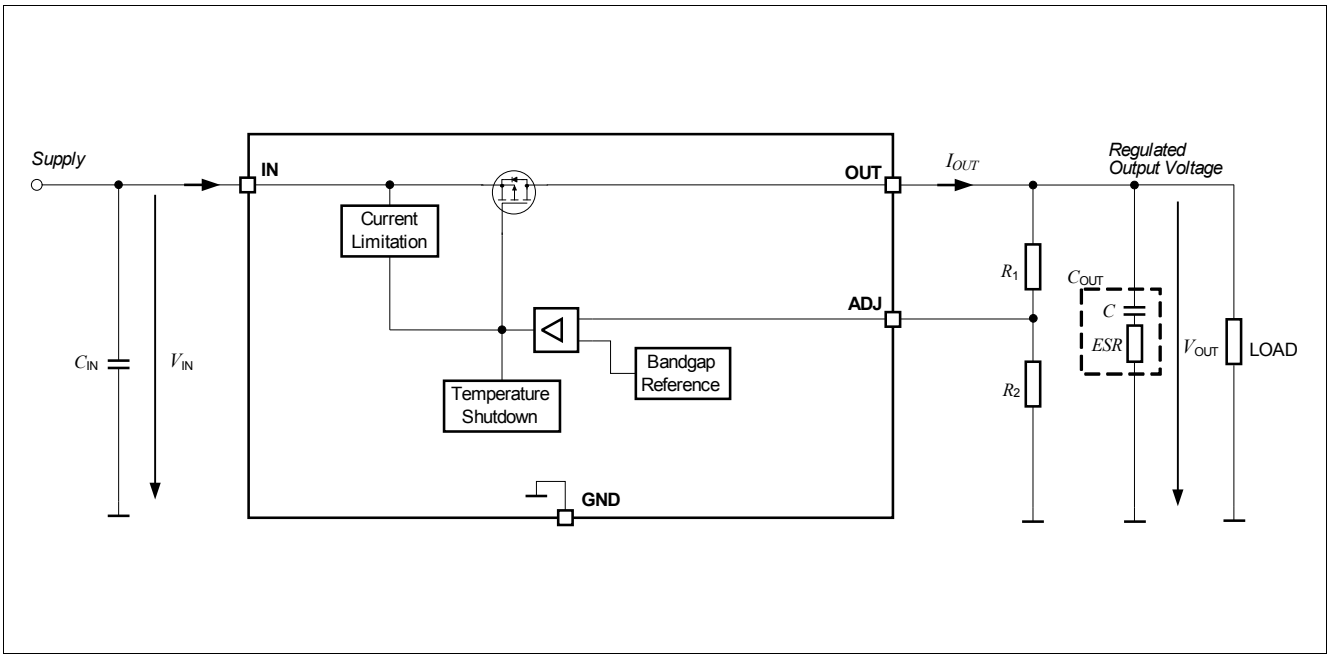


Figure 3 Block Diagram Voltage Regulation

Table 4 Electrical Characteristics

T_j = -40 °C to +125 °C, V_{IN} = 13.5 V all voltages with respect to ground (unless otherwise specified). Typical values are given at Tj = 25°C, V_{IN} = 13.5 V

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage Precision[1]	ΔV_{OUT}	-2	–	2	%	50 µA ≤ I_{OUT} ≤ 50 mA, V_{OUT} + V_{dr} ≤ V_{IN} ≤ 28 V V_{IN} ≥ 3 V, R_2 ≤ 250 kΩ	P_5.1.2
Output Voltage Precision	ΔV_{OUT}	-2	–	2	%	50 µA ≤ I_{OUT} ≤ 25 mA, V_{OUT} + V_{dr} ≤ V_{IN} ≤ 42 V V_{IN} ≥ 3 V, R_2 ≤ 250 kΩ	P_5.1.3
Output Current Limitation	$I_{OUT,lim}$	51	85	120	mA	0 V ≤ V_{OUT} ≤ $V_{OUT,nom}$ - 0.1 V	P_5.1.4
Line Regulation steady-state	$\Delta V_{OUT,line}$	–	1	20	mV	I_{OUT} = 1 mA, 6 V ≤ V_{IN} ≤ 32 V	P_5.1.6
Load Regulation steady-state	$\Delta V_{OUT,load}$	-20	-1	–	mV	V_{IN} = 6 V, 50 µA ≤ I_{OUT} ≤ 50 mA	P_5.1.7
Dropout Voltage[2] V_{dr} = V_{IN} - V_{OUT}	V_{dr}	–	100	300	mV	I_{OUT} = 50 mA, V_{IN} = 5.4 V	P_5.1.11
Reference Voltage	V_{ref}	1.17	1.2	1.23	V	–	P_5.1.12
Ripple Rejection[3]	*PSRR*	–	60	–	dB	I_{OUT} = 50 mA, V_{OUT} = 1.2 V f_{ripple} = 100 Hz, V_{ripple} = 0.5 V_{p-p}	P_5.1.13
Over temperature Shutdown Threshold	$T_{j,sd}$	151	175	–	°C	T_j increasing	P_5.1.14
Over temperature Shutdown Threshold Hysteresis	$T_{j,sdh}$	–	10	–	K	T_j decreasing	P_5.1.15

1) Referring to the device tolerance only, the tolerance of the resistor divider can cause additional deviation. Parameter is tested with the ADJ pin directly connected to the output pin OUT.

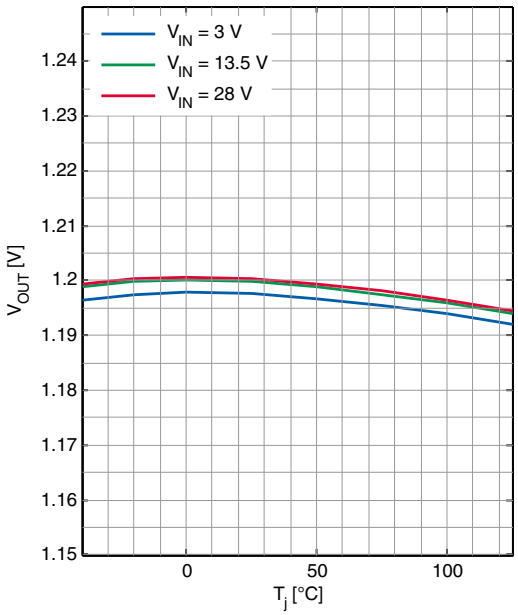
2) Measured when the output voltage V_{OUT} has dropped 100mV from the nominal value obtained at V_{IN} = 13.5 V

3) Not subject to production test, guaranteed by design

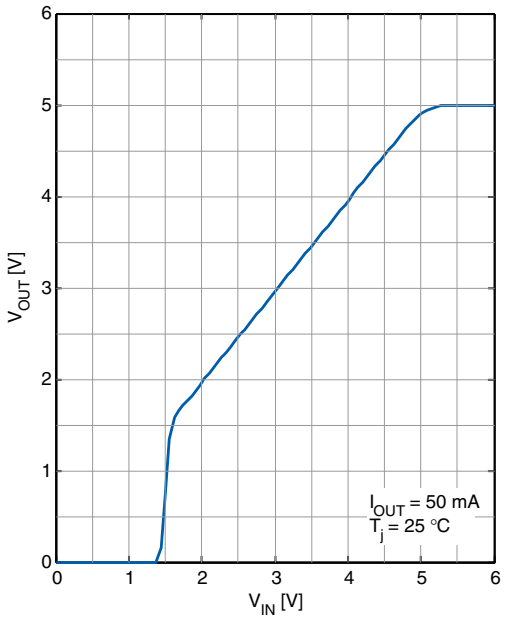
5.2 Typical Performance Characteristics Voltage Regulation

Typical Performance Characteristics

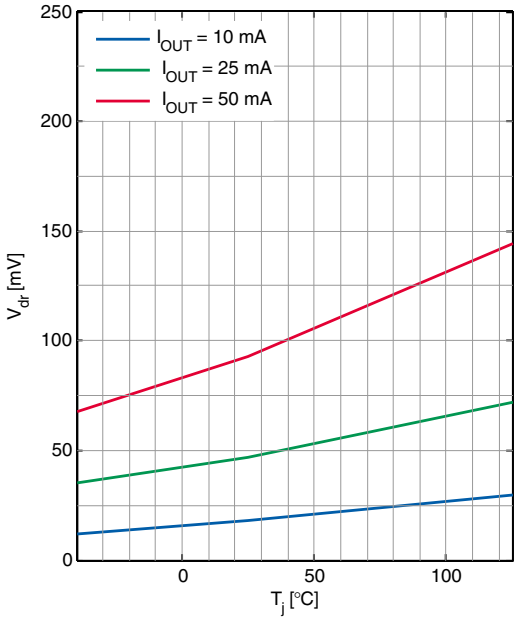
Output Voltage V_{OUT} versus Junction Temperature T_j



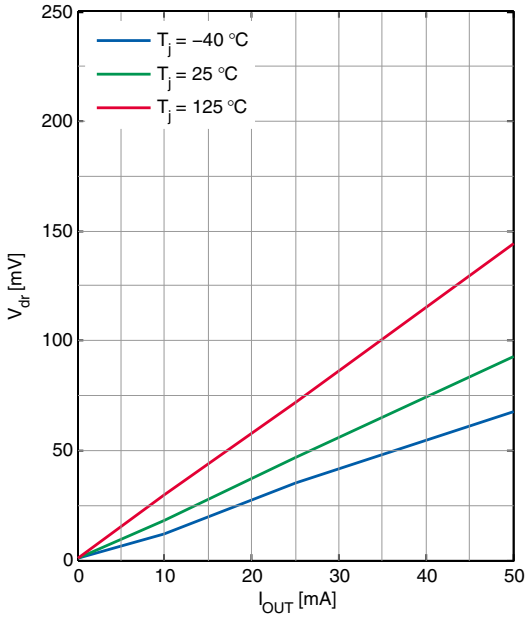
Output Voltage V_{OUT} versus Input Voltage V_{IN}



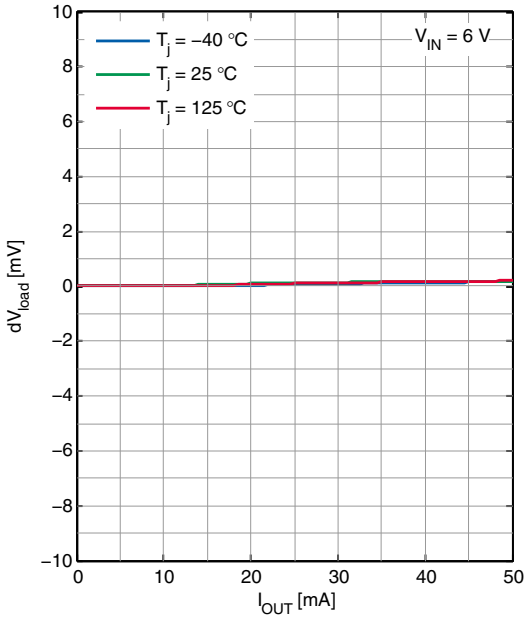
Dropout Voltage V_{dr} versus Junction Temperature T_j



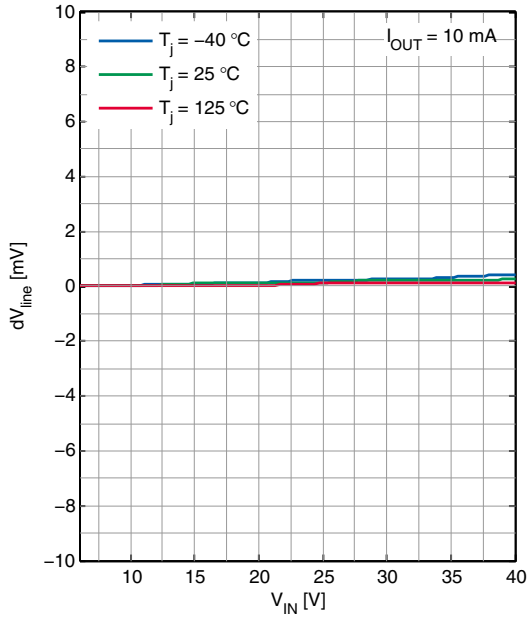
Dropout Voltage V_{dr} versus Output Current I_{OUT}



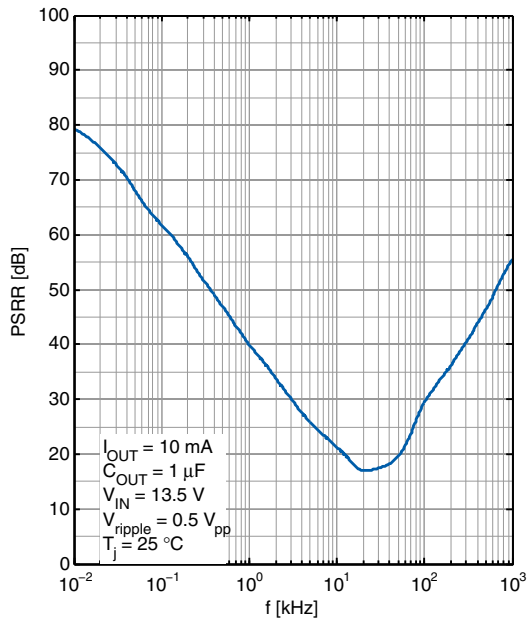
Load Regulation $\Delta V_{OUT,load}$ versus Output Current Change ΔI_{OUT}



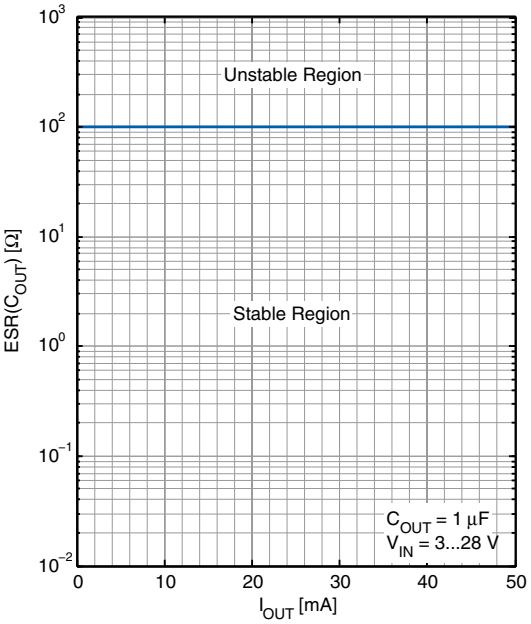
Line Regulation $\Delta V_{OUT,line}$ versus Input Voltage V_{IN}



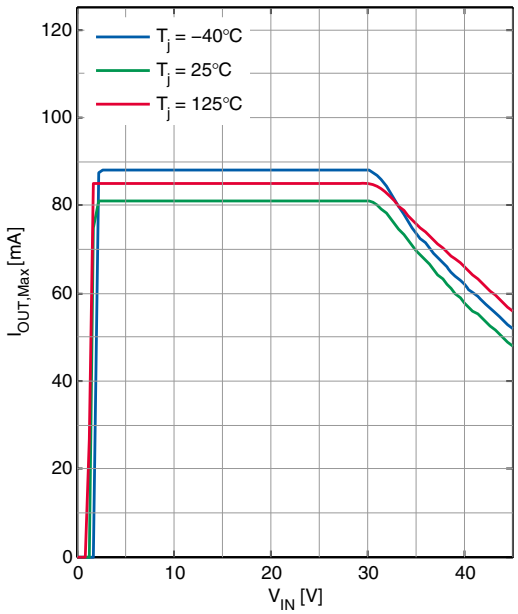
Power Supply Ripple Rejection *PSRR* versus ripple frequency f_r



Output Capacitor Series Resistor *ESR*(C_{OUT}) versus Output Current I_{OUT}



Maximum Output Current $I_{OUT,Max}$ versus Input Voltage V_{IN}



5.3 Current Consumption

Table 5 Electrical Characteristics Current Consumption IFX30081LDV

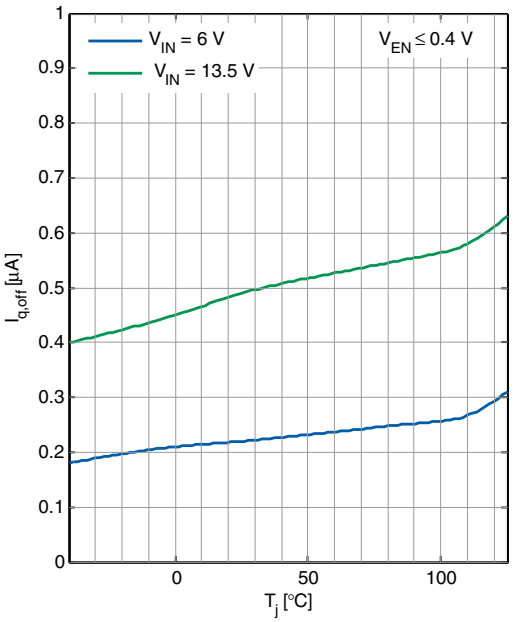
T_j = -40 °C to +125 °C, V_{IN} = 13.5 V, all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption $I_q = I_{IN}$	$I_{q,OFF}$	–	–	1	µA	$V_{EN} \leq 0.4$ V, $T_j < 105$ °C	P_5.3.1
Current Consumption $I_q = I_{IN} - I_{OUT}$	I_q	–	5	7.5	µA	I_{OUT} = 50µA, T_j = 25 °C	P_5.3.2
Current Consumption $I_q = I_{IN} - I_{OUT}$	I_q	–	6	10	µA	I_{OUT} = 50 µA, $T_j < 105$ °C	P_5.3.3
Current Consumption $I_q = I_{IN} - I_{OUT}$	I_q	–	6.5	11	µA	I_{OUT} = 50 µA, $T_j < 125$ °C	P_5.3.4
Current Consumption $I_q = I_{IN} - I_{OUT}$	I_q	–	6.5	11	µA	I_{OUT} = 50 mA, $T_j < 125$ °C	P_5.3.5

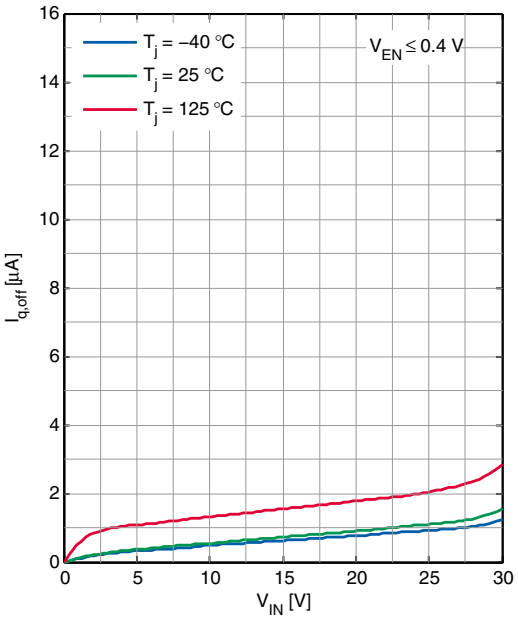
5.4 Typical Performance Characteristics Current Consumption

Typical Performance Characteristics

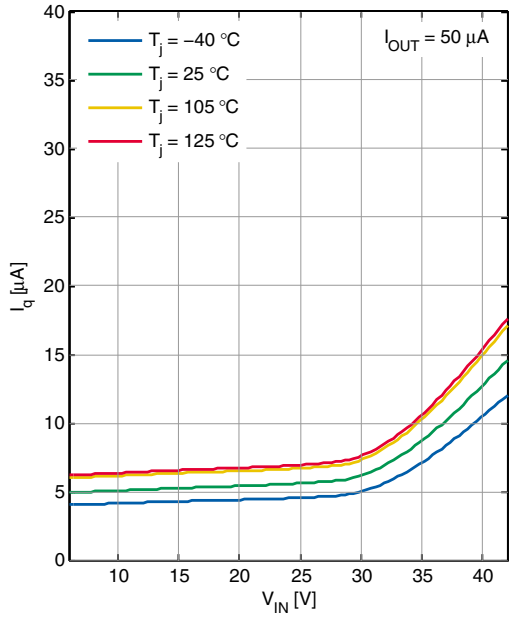
Current Consumption in OFF mode $I_{q,OFF}$ versus Junction Temperature T_j



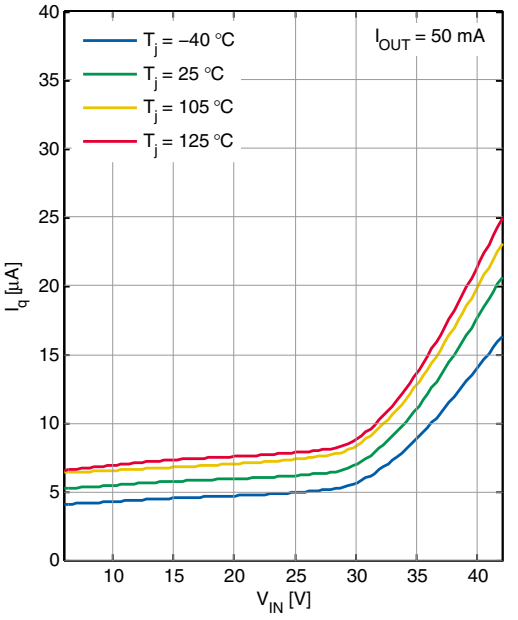
Current Consumption in OFF mode $I_{q,OFF}$ versus Input Voltage V_{IN}



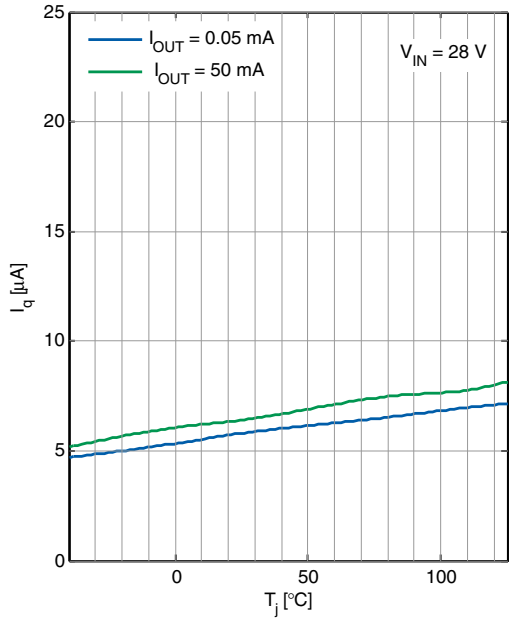
Current Consumption I_q versus Input Voltage V_{IN}



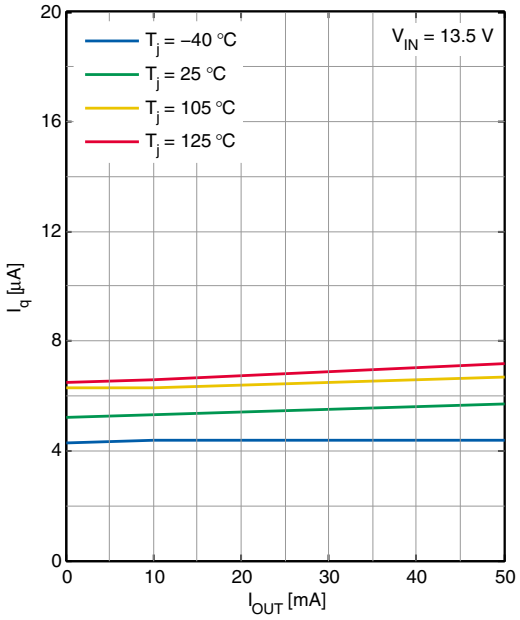
Current Consumption I_q versus Input Voltage V_{IN}



Current Consumption I_q versus Junction Temperature T_j



Current Consumption $I_q$versus Output Current I_{OUT}



5.5 Enable

The device IFX30081LDV can be switched on and off by the Enable feature: Connect a HIGH level as specified below (e.g. the battery voltage) to pin EN to enable the device; connect a LOW level as specified below (e.g. GND) to shut it down. The enable has a build in hysteresis to avoid toggling between ON/OFF state, if signals with slow slopes are applied to the enable input.

Table 6 Electrical Characteristics Enable

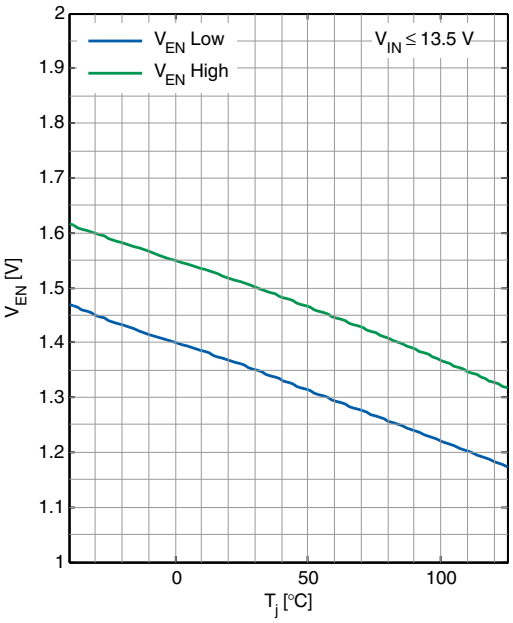
T_j = -40 °C to +125 °C, V_{IN} = 13.5 V all voltages with respect to ground (unless otherwise specified). Typical values are given at Tj = 25°C, V_{IN} = 13.5 V

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
High Level Enable Input Voltage	$V_{EN,H}$	2	–	–	V	V_{OUT} settled	P_5.5.1
Low Level Enable Input Voltage	$V_{EN,L}$	–	–	0.8	V	$V_{OUT} \leq 0.1$ V	P_5.5.2
High Level Input Current	$I_{EN,H}$	–	–	4	µA	V_{EN} = 5 V	P_5.5.4
Enable Internal Pull-down Resistor	R_{EN}	1.25	2	3.5	MΩ		P_5.5.6

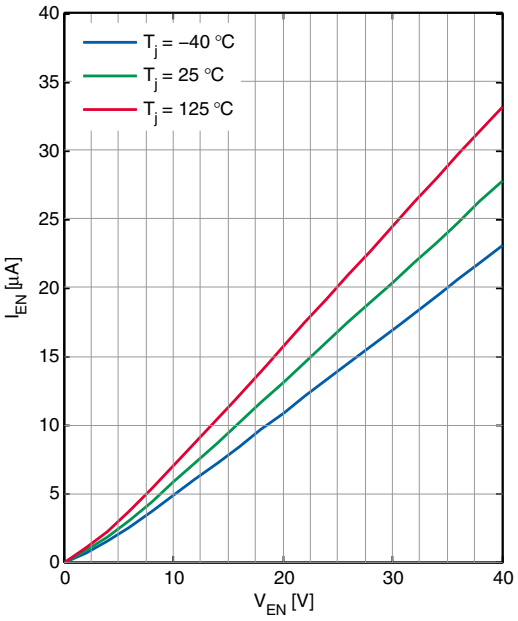
5.6 Typical Performance Characteristics Enable

Typical Performance Characteristics

Enable Input Voltage V_{EN} versus Junction Temperature T_j



Enable Input Current I_{EN} versus Enable Input Voltage V_{EN}



6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

6.1 Application Diagram

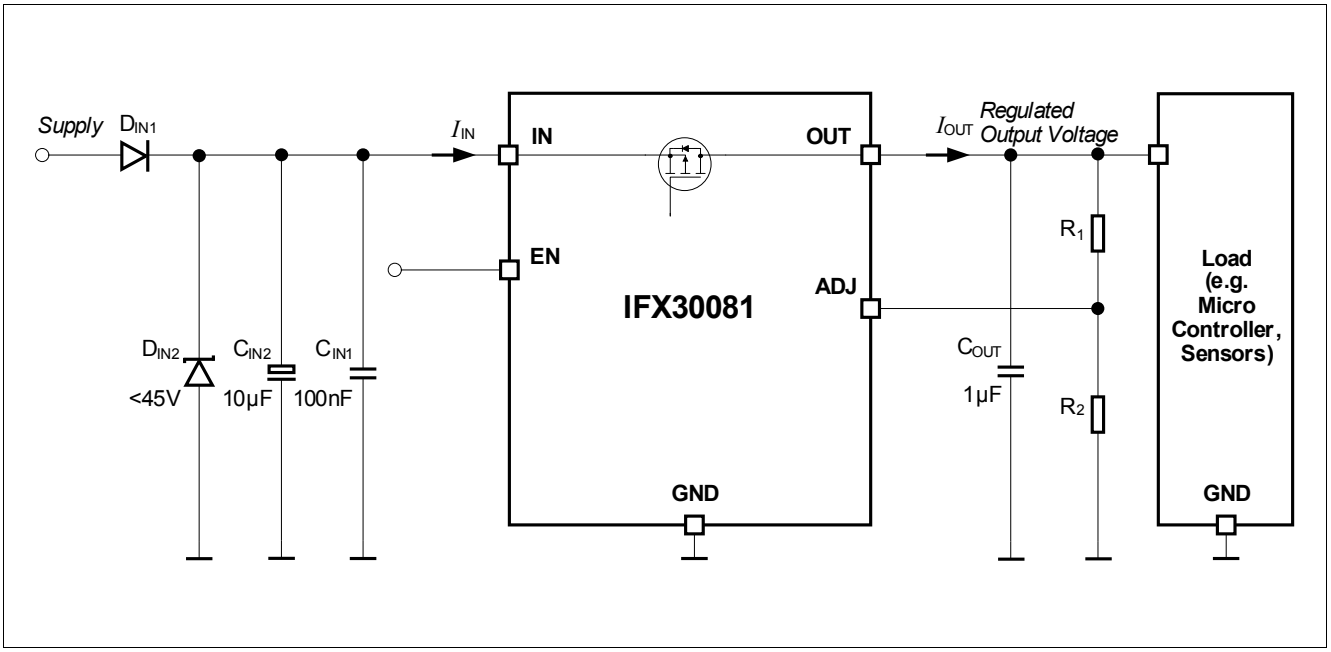


Figure 4 Application Diagram IFX30081LDV

6.2 Selection of External Components

6.2.1 Input Pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above i.e. Figure 4. A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line. The capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminium electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses. The capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage. The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

6.2.2 Output Pin

An output capacitor is mandatory for the stability of linear voltage regulators. The requirement of the output capacitor is given in **"Functional Range" on Page 8**. The graph **"Output Capacitor Series Resistor ESR(C_{OUT}) versus Output Current I_{OUT}" on Page 13** shows the stable operation range of the device. IFX30081LDV is designed to be stable with extremely low ESR capacitors. The output capacitor should be placed as close as possible to the regulator's output and GND pins, on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application to make sure that the stability requirements are fulfilled.

6.3 Output Voltage Adjust

The output voltage of the IFX30081LDV can be adjusted between 1.2 V and V_{IN} - V_{dr} by an external resistor divider, connected to the adjust pin ADJ, as shown in **Figure 4**.

The ADJ pin is connected internally to an error amplifier comparing the voltage at this pin with the internal reference voltage of typically 1.2 V. The output voltage can be easily calculated, neglecting the current flowing into the ADJ pin:

(6.1)

$$V_{OUT} = \frac{R_1 + R_2}{R_2} \times V_{ref}$$

where,
V_{ref}: internal reference voltage, typically 1.2V
R_1: resistor between regulator output OUT and adjust pin ADJ
R_2: resistor between adjust pin ADJ and GND

The bigger the resistors R_1 and R_2, the less the current flowing through the resistor divider. However, using very big resistors makes the current flowing into the ADJ pin non-negligible. In order to neglect the current flowing into the ADJ pin, the values of R_1 and R_2 should be selected fulfilling the criteria $R_2 \leq 250$ kΩ.

To set the output voltage to 1.2 V, the adjust pin ADJ should be directly connected to the output pin OUT.

Take into consideration that an additional error to the output voltage tolerance may be introduced by the accuracy of the resistors R_1 and R_2.

6.4 Thermal Considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

(6.2)

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_q$$

where,

Application Information

P_D: Continuous power dissipation
V_{IN}: Input Voltage
V_{OUT}: Output Voltage
I_{OUT}: Output Current
I_q: Quiescent Current

The maximum acceptable thermal resistance R_{thJA} can then be calculated as:

(6.3)

$$R_{thJA,\,max} = \frac{T_{j,\,max} - T_a}{P_D}$$

where,
$T_{j,max}$: Maximum allowed junction temperature
T_a: Ambient temperature of the application

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in “Thermal Resistance” on Page 9.

Example

Application conditions:
V_{IN} = 18 V
V_{OUT} = 5 V
I_{OUT} = 40 mA
T_a = 85 °C

Based on the equation (6.1), we can calculate the power dissipation for the above application example.
P_D = (18 V - 5 V) x 40 mA + 18 V x 0.011 mA = 0.52 W

According to equation (6.2), $R_{thJA,max}$ can be calculated as (125 °C - 85 °C)/0.52 W = 40/0.52 K/W = 76.9 K/W
As a result, for the above application example the PCB design must ensure a thermal resistance lower than 76.9 K/W. According to “Thermal Resistance” on Page 9, at least 300mm^2 heatsink area is needed on a FR4 1s0p PCB for this application.

6.5 Reverse Polarity Protection

IFX30081LDV is not self protected against reverse polarity faults. To protect the device against negative supply voltage, an external reverse polarity diode is needed, as shown in Figure 4. The absolute maximum ratings of the device as specified in “Absolute Maximum Ratings” on Page 7 must be kept.

6.6 Further Application Information

For further information please refer to http://www.infineon.com

7 Package Outlines

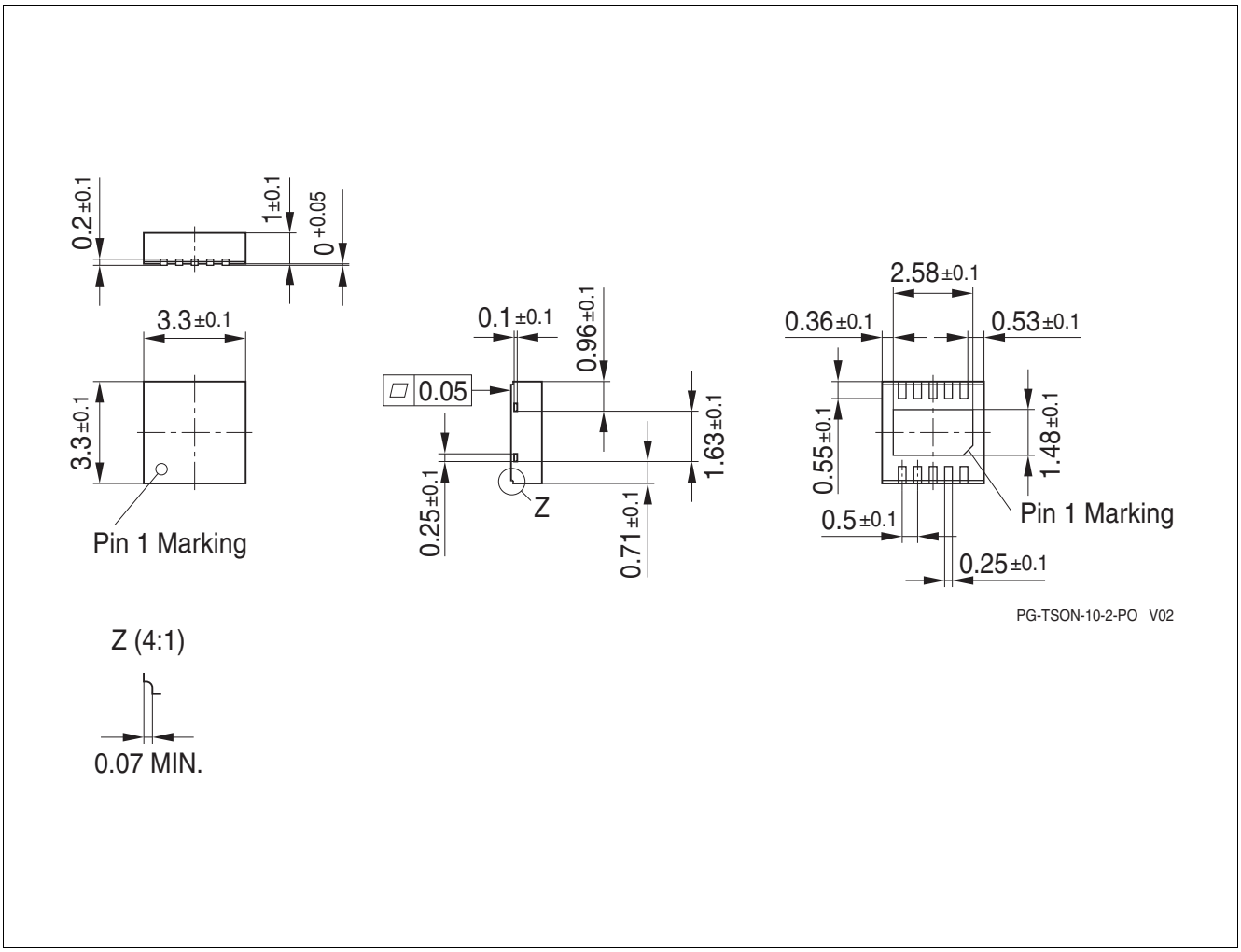


Figure 5 **PG-TSON-10** (**IFX30081LDV**) Package Outline

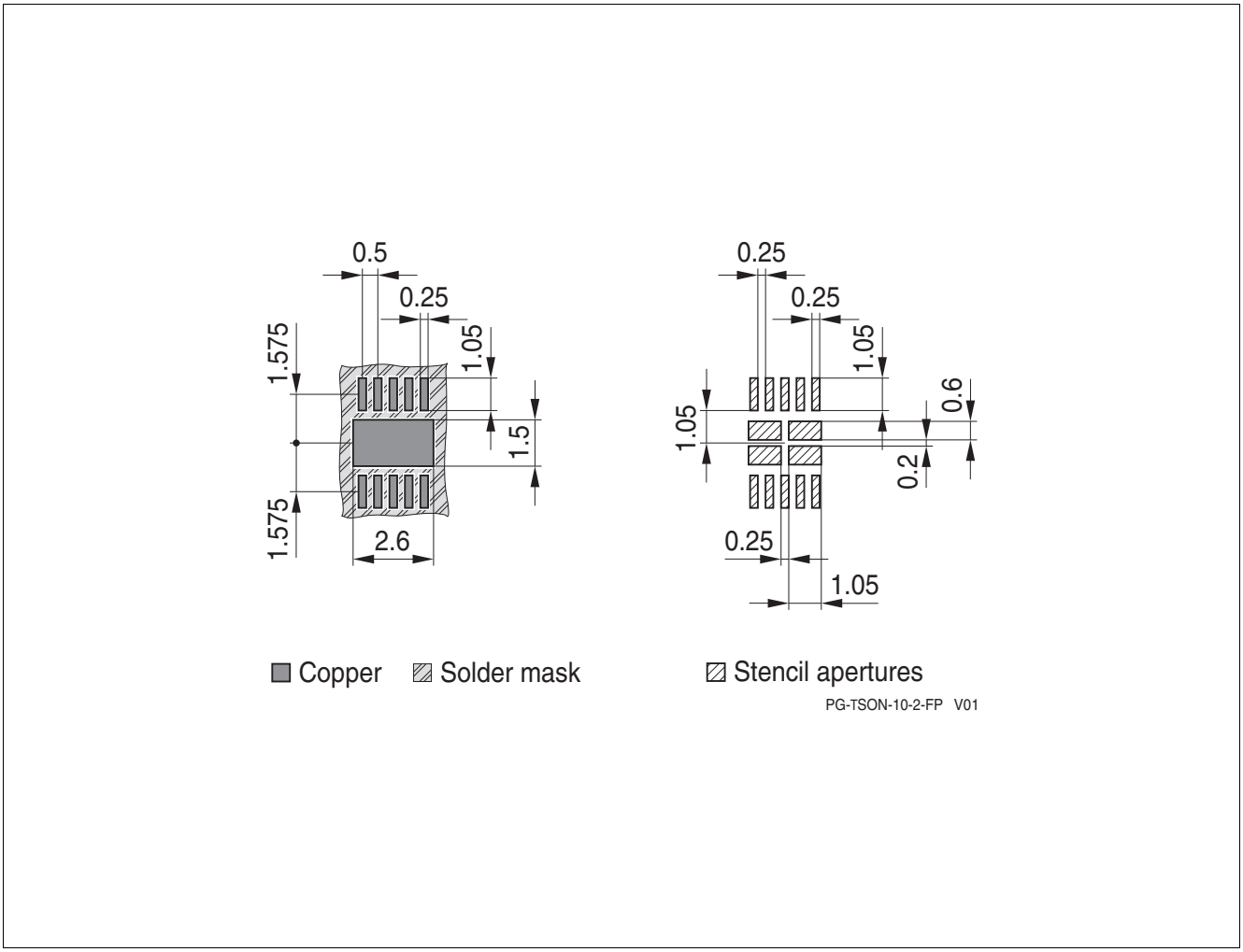


Figure 6 **PG-TSON-10** (**IFX30081LDV**) Package Footprint

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

8 Revision History

Revision	Date	Changes
1.0	2016-03-11	Data Sheet - Initial Version

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