PD-97834B

IRHLQ7S7214
2N7615U6

RADIATION HARDENED LOGIC LEVEL POWER MOSFET SURFACE MOUNT (LCC-28)

250V, Quad N-CHANNEL
R7 TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I_D
IRHLQ7S7214	100 kRads(Si)	1.0Ω	2.6A
IRHLQ7S3214	300 kRads(Si)	1.0Ω	2.6A

LCC-28

Description

IR HiRel R7 S-Line Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments.The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation.This is achieved while maintaining single event gate rupture and single event burnout immunity.
The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Features

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Package
- Surface Mount
- Light Weight
- ESD Rating: Class 1B per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = 4.5V, T_C = 25°C	Continuous Drain Current	2.6	A
I_{D2} @ V_{GS} = 4.5V, T_C = 100°C	Continuous Drain Current	1.6	
I_{DM} @ T_C = 25°C	Pulsed Drain Current ①	10.4	
P_D @T_C = 25°C	Maximum Power Dissipation	12	W
	Linear Derating Factor	0.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy ②	38.5	mJ
I_{AR}	Avalanche Current ①	2.6	A
E_{AR}	Repetitive Avalanche Energy ①	1.2	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.56	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (for 5s)	
	Weight	0.89 (Typical)	g

For Footnotes, refer to the page 2

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.25	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.0	Ω	V_{GS} = 4.5V, I_{D2} = 1.6A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-5.3	—	mV/°C	
Gfs	Forward Transconductance	2.5	—	—	S	V_{DS} = 15V, I_{D2} = 1.6A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	V_{DS} = 200V, V_{GS} = 0V
		—	—	15		V_{DS} = 200V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 10V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -10V
Q_G	Total Gate Charge	—	—	18	nC	I_{D1} = 2.6A
Q_{GS}	Gate-to-Source Charge	—	—	5.0		V_{DS} = 125V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	12		V_{GS} = 4.5V
$t_{d(on)}$	Turn-On Delay Time	—	—	27	ns	V_{DD} = 125V
tr	Rise Time	—	—	57		I_{D1} = 2.6A
$t_{d(off)}$	Turn-Off Delay Time	—	—	45		R_G = 7.5Ω
t_f	Fall Time	—	—	55		V_{GS} = 5.0V
Ls +L_D	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	605	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	62	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	0.7	—		f = 1.0MHz
R_G	Gate Resistance	—	8.0	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.6	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	10.4		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 2.6A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	371	ns	T_J = 25°C, I_F = 2.6A, V_{DD} ≤ 25V
Q_{rr}	Reverse Recovery Charge	—	—	858	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta J\text{-}PCB}$	Junction-to-PCB	—	—	10.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	90	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.
② V_{DD} = 50V, starting T_J = 25°C, L = 11.4mH, Peak I_L = 2.6A, V_{GS} = 10V
③ I_{SD} ≤ 2.6A, di/dt ≤ 399A/μs, V_{DD} ≤ 250V, T_J ≤ 150°C
④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
⑤ Total Dose Irradiation with V_{GS} Bias. 10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
⑥ Total Dose Irradiation with V_{DS} Bias. 200 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	Up to 300 kRads (Si) [1]		Units	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	V	V_{GS} = 0V, I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V_{GS} = 10V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100	nA	V_{GS} = -10V
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	μA	V_{DS} = 200V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.85	Ω	V_{GS} = 4.5V, I_{D2} = 1.6A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (LCC-28)	—	1.0	Ω	V_{GS} = 4.5V, I_{D2} = 1.6A
V_{SD}	Diode Forward Voltage	—	1.2	V	V_{GS} = 0V, I_S = 2.6A

1. Part number IRHLQ7S7214, IRHLQ7S3214

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

ION	LET (MeV/(mg/cm²))	Energy (MeV)	Range (μm)	VDS (V)					
				@ VGS = 0V	@ VGS = -1V	@ VGS = -2V	@ VGS = -5V	@ VGS = -6V	@ VGS = -7V
Kr	34.1	573	69.6	250	250	250	250	250	250
Xe	56.8	1010	79.7	250	250	250	—	—	—

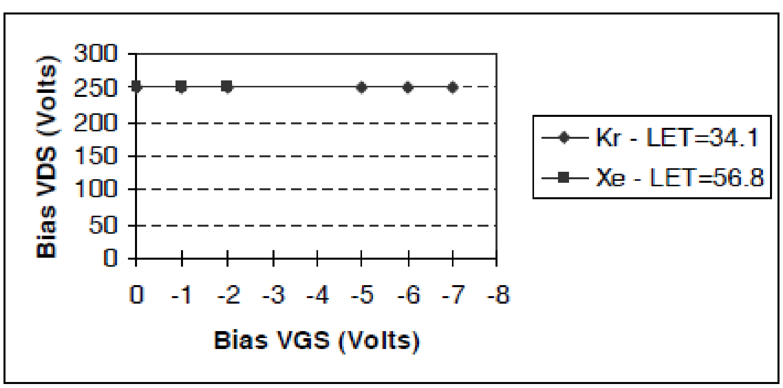


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

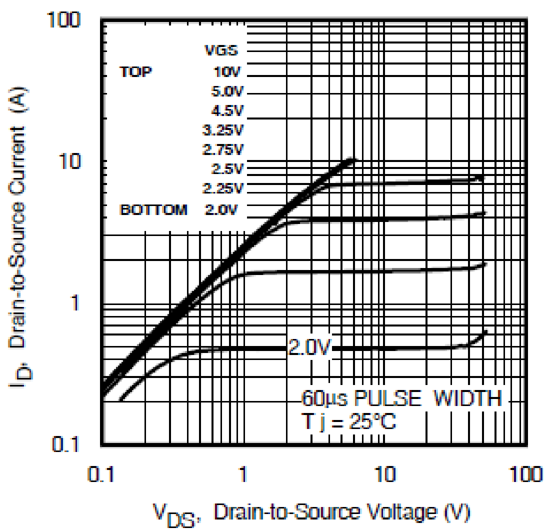


Fig 1. Typical Output Characteristics

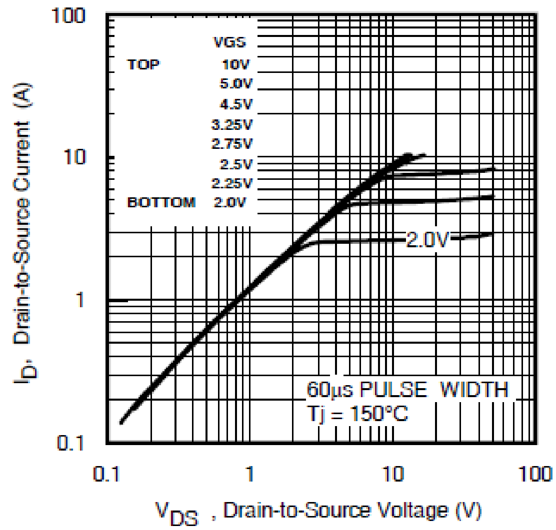


Fig 2. Typical Output Characteristics

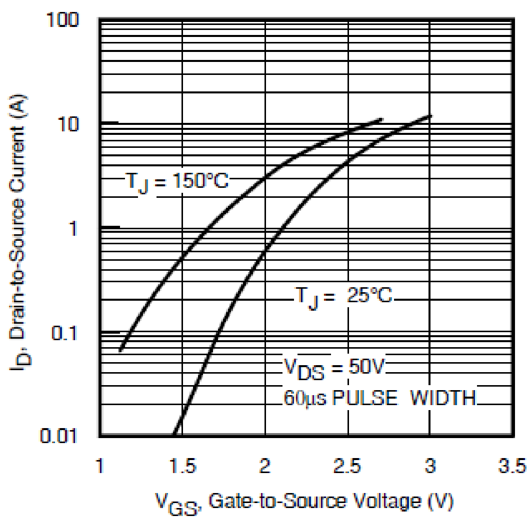


Fig 3. Typical Transfer Characteristics

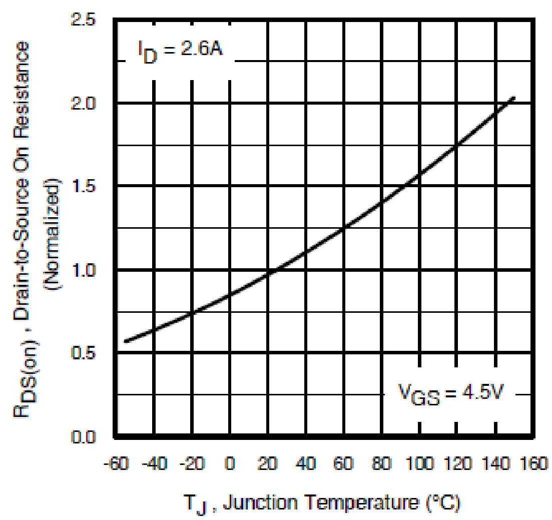


Fig 4. Normalized On-Resistance Vs. Temperature

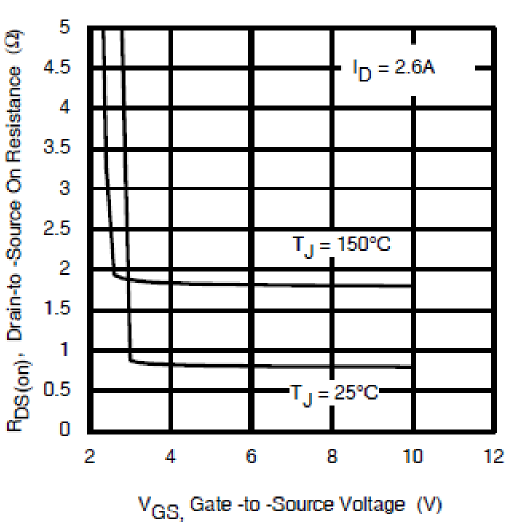


Fig 5. Typical On-Resistance Vs Gate Voltage

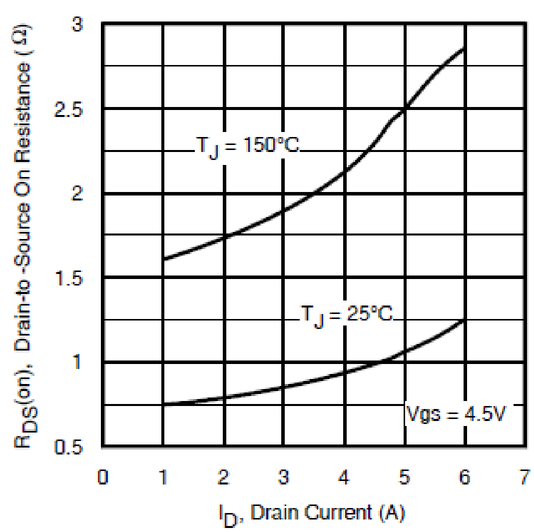


Fig 6. Typical On-Resistance Vs Drain Current

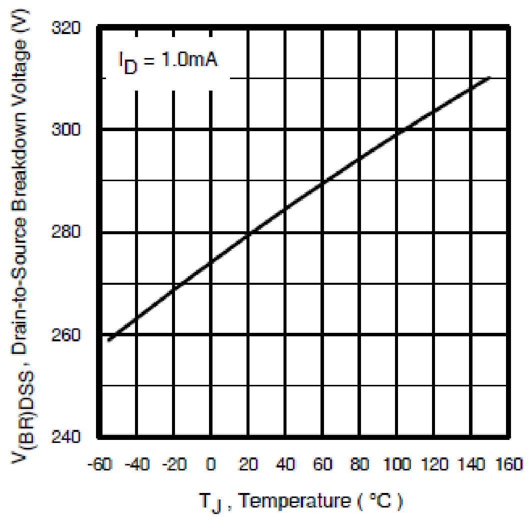


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

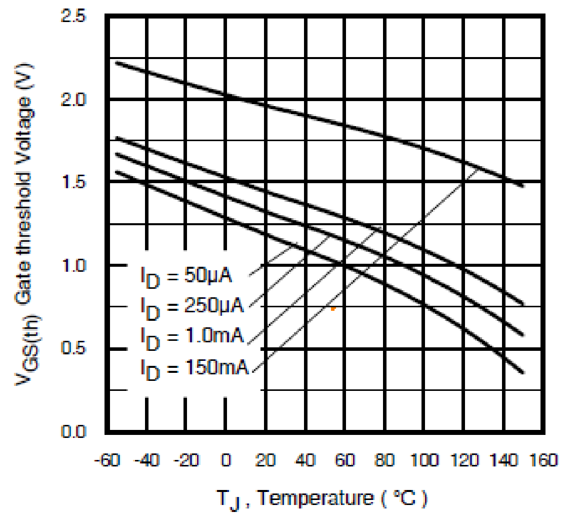


Fig 8. Typical Threshold Voltage Vs Temperature

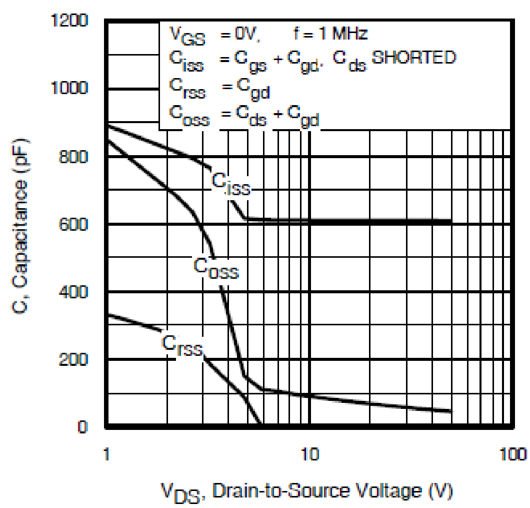


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

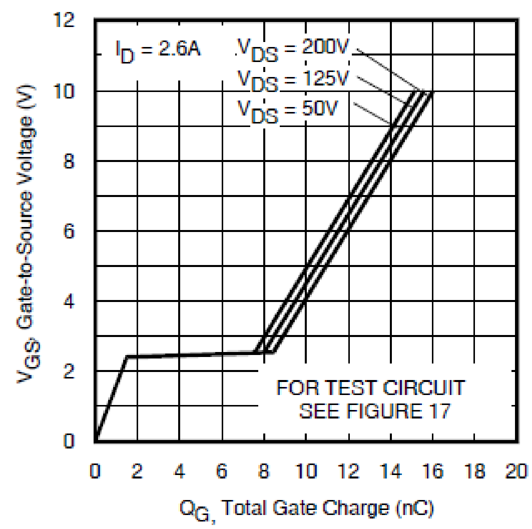


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

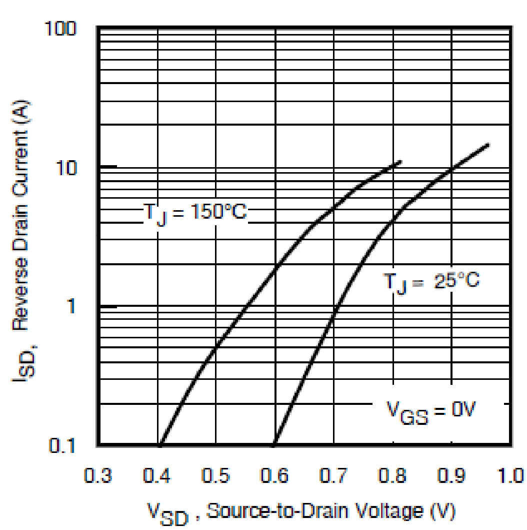


Fig 11. Typical Source-Drain Diode Forward Voltage

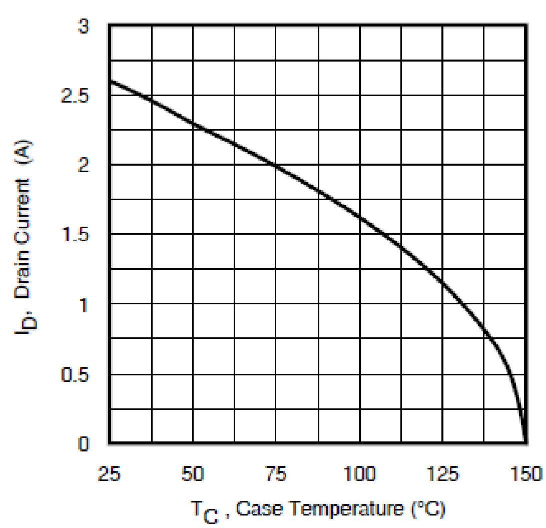


Fig 12. Maximum Drain Current Vs.Case Temperature

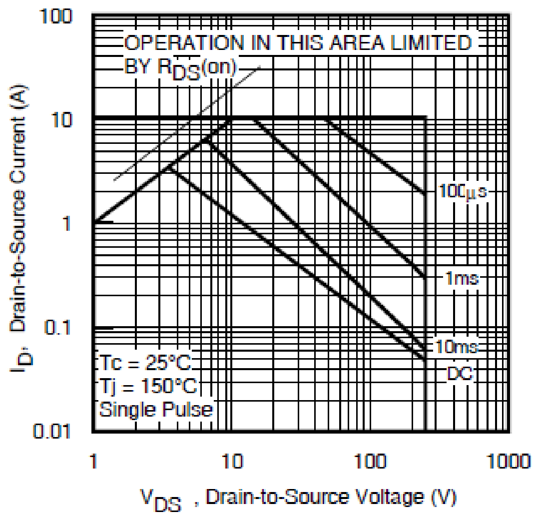


Fig 13. Maximum Safe Operating Area

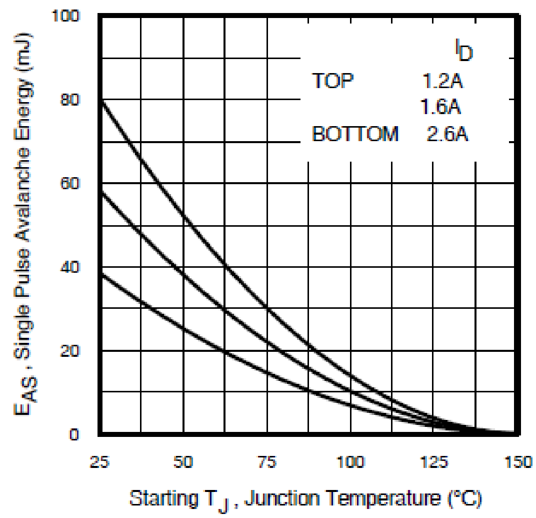


Fig 14. Maximum Avalanche Energy Vs. Drain Current

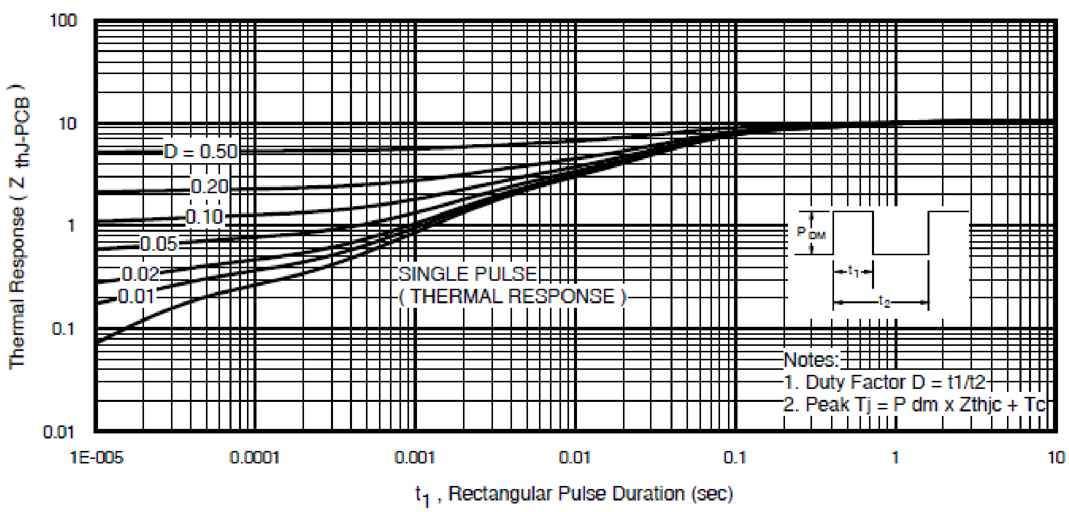


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-PCB

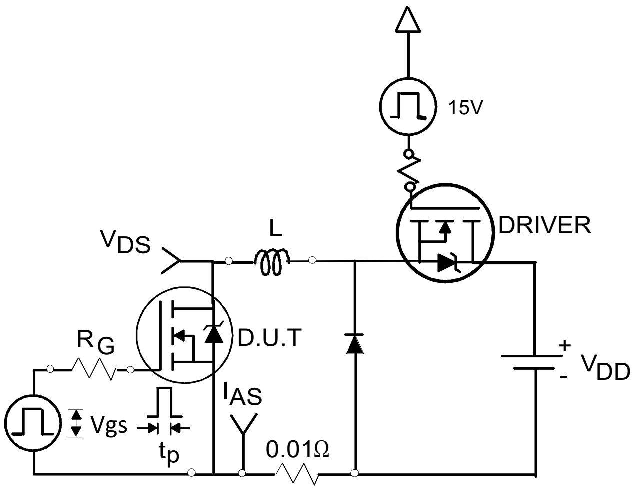


Fig 16a. Unclamped Inductive Test Circuit

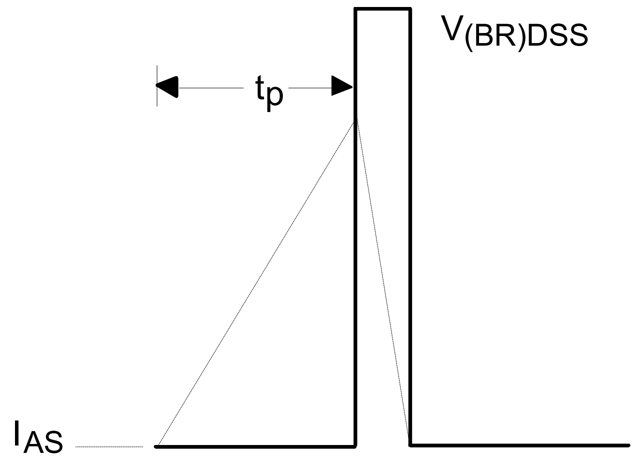


Fig 16b. Unclamped Inductive Waveforms

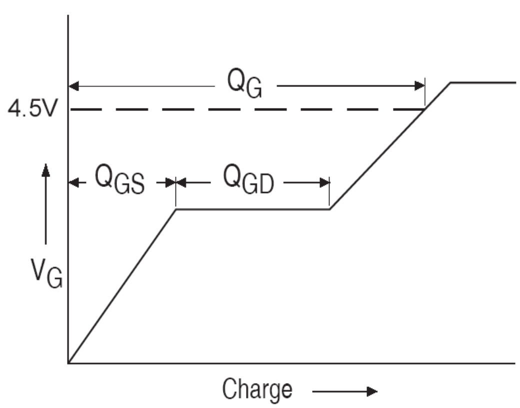


Fig 17a. Gate Charge Waveform

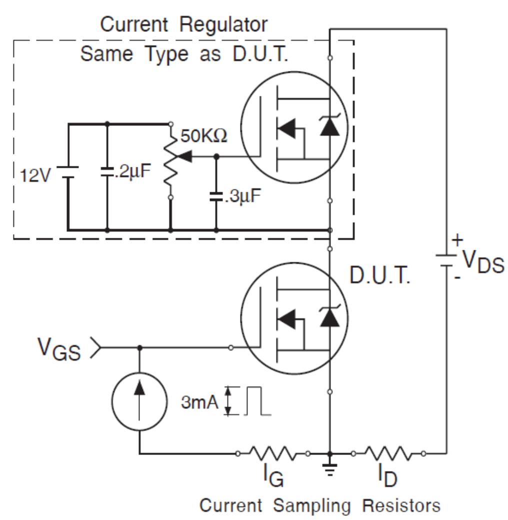


Fig 17b. Gate Charge Test Circuit

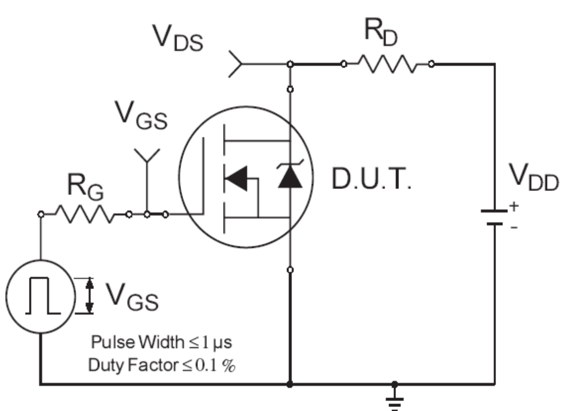


Fig 18a. Switching Time Test Circuit

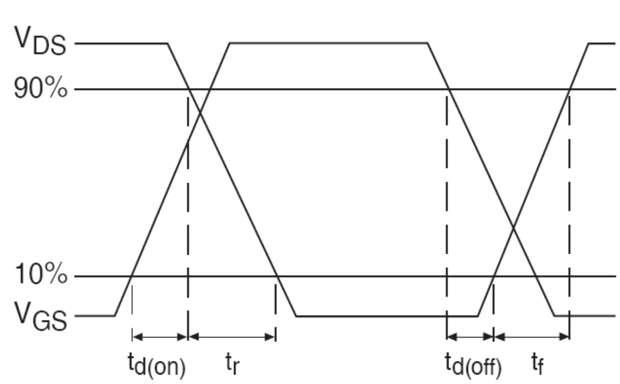
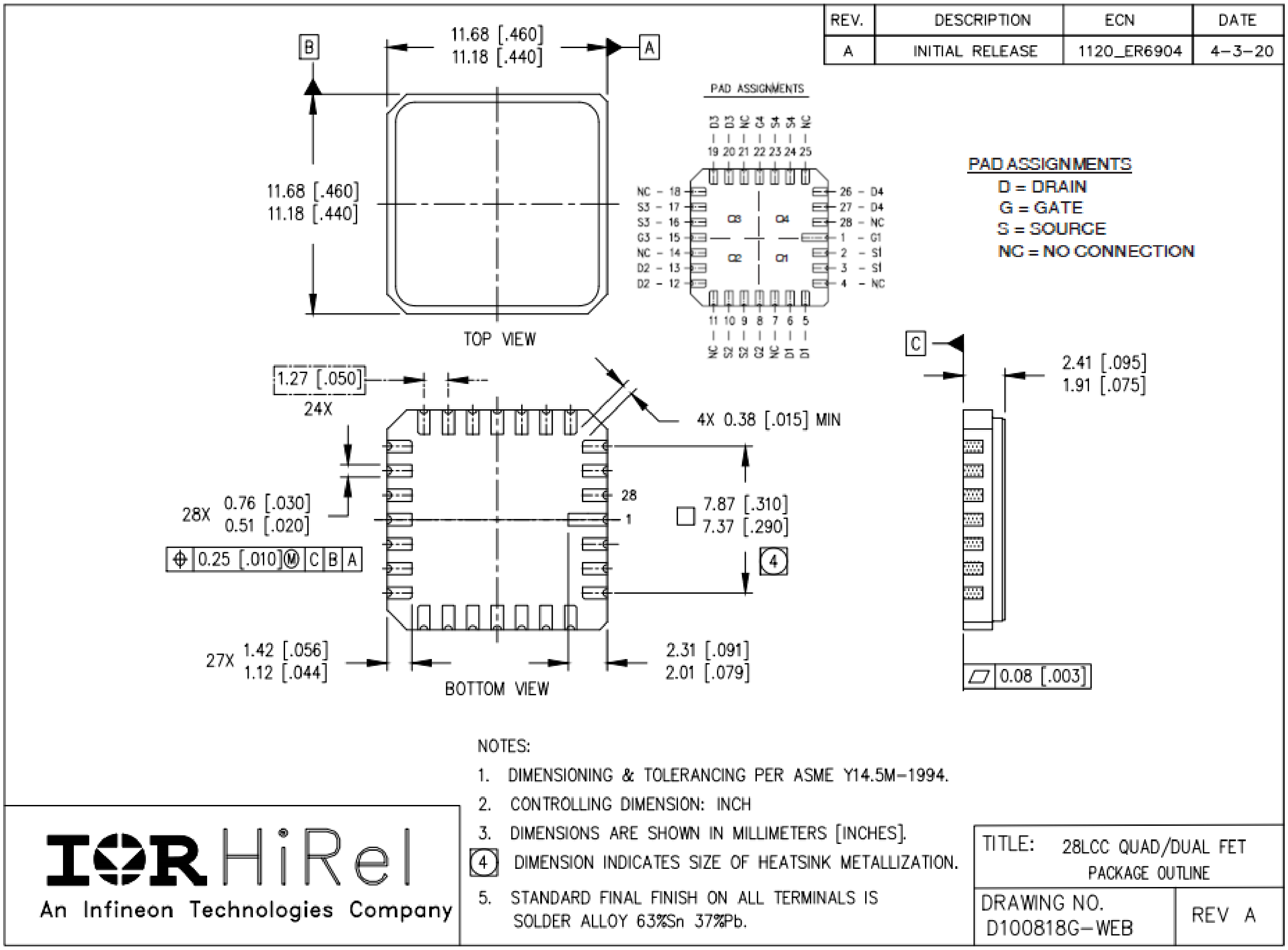


Fig 18b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: [LCC-28]

Case Outline and Dimensions — LCC-28



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