International
IOR Rectifier

DS No.PD60266 Rev A

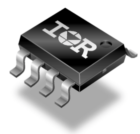
IRS2308(S)PbF

HALF-BRIDGE DRIVER

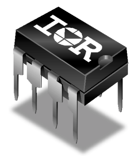
Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Logic and power ground +/- 5 V offset.
- Internal 540 ns deadtime
- Lower di/dt gate driver for better noise immunity

Packages



8-Lead SOIC
IRS2308S



8-Lead PDIP
IRS2308

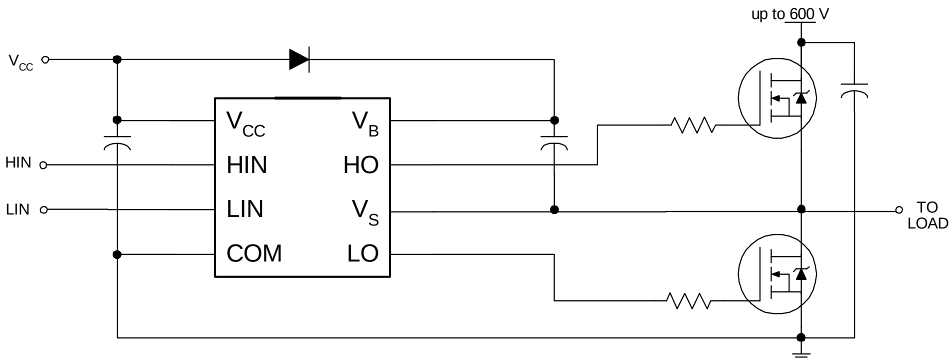
Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Deadtime (ns)	Ground Pins	Ton/Toff (ns)
2106	HIN/LIN	no	none	COM	220/200
21064				V_{SS}/COM	
2108	HIN/$\overline{LIN}$	yes	Internal 540	COM	220/200
21084			Programmable 540 - 5000	V_{SS}/COM	
2109	IN/$\overline{SD}$	yes	Internal 540	COM	750/200
21094			Programmable 540 - 5000	V_{SS}/COM	
2304	HIN/LIN	yes	Internal 100	COM	160/140
2308	HIN/LIN	yes	Internal 540	COM	220/200

Description

The IRS2308 is a high voltage, high speed power MOSFET and IGBT driver with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 V.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage param eters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measure under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Un
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)		V_{SS} - 0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/n
P_D	Package power dissipation @ $T_A \leq$ +25 °C	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within th recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min.	Max.	Un
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	COM	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$. (Please refer to the Desig DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, C_L = 1000 pF, T_A = 25 °C, DT = V_{SS} unless otherwise specified.

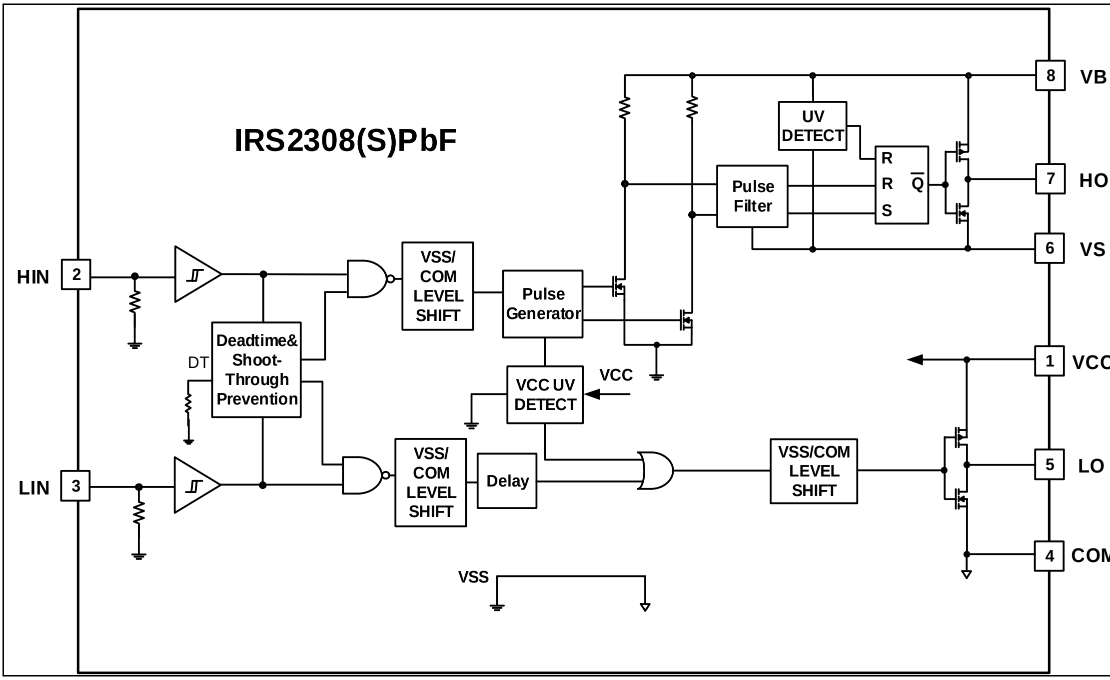
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditi
t_{on}	Turn-on propagation delay	—	220	300	ns	V_S = 0 V
t_{off}	Turn-off propagation delay	—	200	280		V_S = 0 V or 60
MT	Delay matching | t_{on} - t_{off} |	—	0	46		
t_r	Turn-on rise time	—	100	220		V_S = 0 V
t_f	Turn-off fall time	—	35	80		
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	400	540	680		
MDT	Deadtime matching = | DT_{LO-HO} - DT_{HO-LO} |	—	0	60		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, DT= V_{SS} and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH}, and I_{IN} par eters are referenced to V_{SS}/COM and are applicable to the respective input leads: HIN and LIN. The V_O, I_O, and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditi
V_{IH}	Logic "1" input voltage for HIN & LIN	2.5	—	—	V	V_{CC} = 10 V to 2
V_{IL}	Logic "0" input voltage for HIN & LIN	—	—	0.8		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.05	0.2		I_O = 2 mA
V_{OL}	Low level output voltage, V_O	—	0.02	0.1		
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 60
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0 V or 5
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	
I_{IN+}	Logic "1" input bias current	—	5	20	µA	HIN = 5 V, LIN =
I_{IN-}	Logic "0" input bias current	—	1	2		HIN = 0 V, LIN =
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed curren	200	290	—	mA	V_O = 0 V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	420	600	—		V_O = 15 V, PW ≤ 10 µs

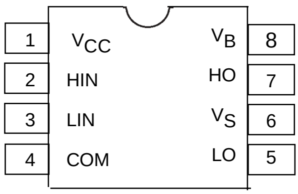
Functional Block Diagram



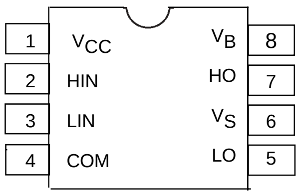
Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
V_B	High side floating supply
HO	High side gate driver output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate driver output
COM	Low side return

Lead Assignments



8 Lead PDIP



8 Lead SOIC

IRS2308PbF	IRS2308SPbF

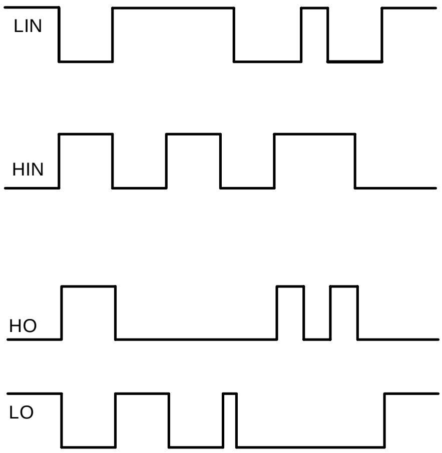


Figure 1. Input/Output Timing Diagram

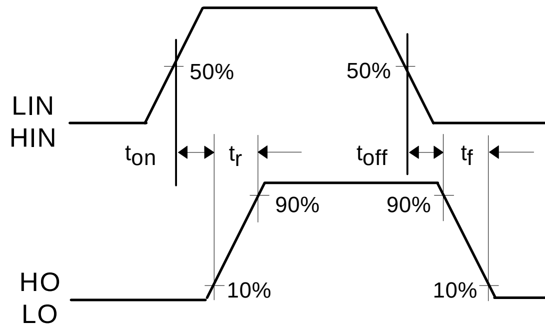


Figure 2. Switching Time Waveform Definitions

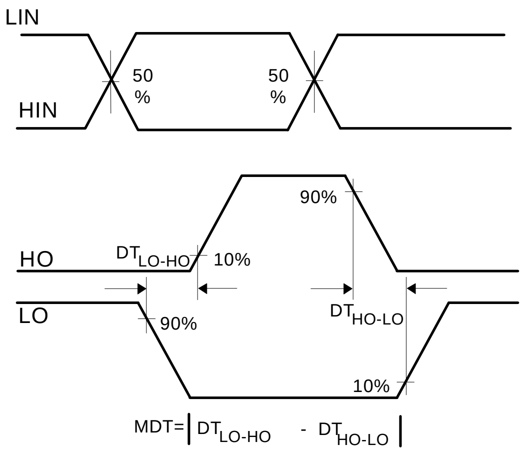


Figure 3. Deadtime Waveform Definitions

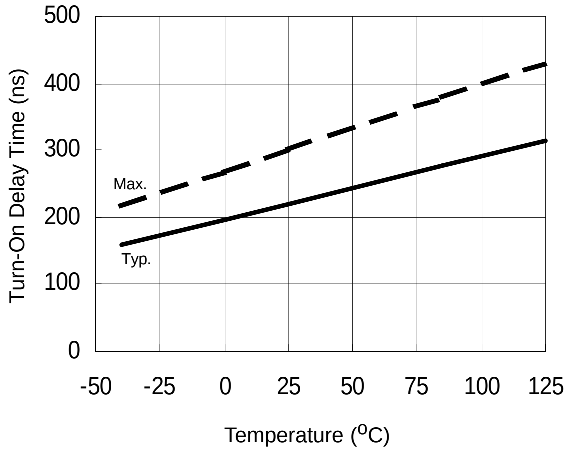


Figure 4A. Turn-On Time vs. Temperature

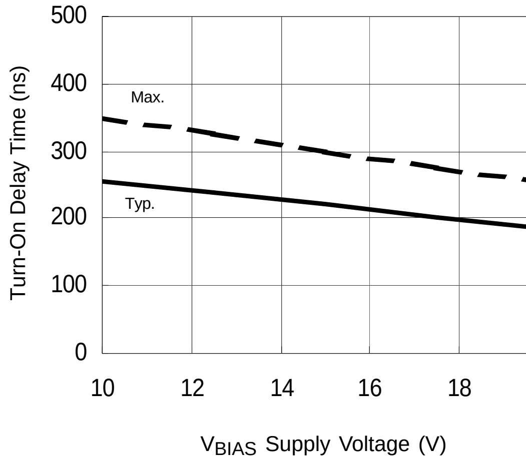


Figure 4B. Turn-On Time vs. Supply Voltage

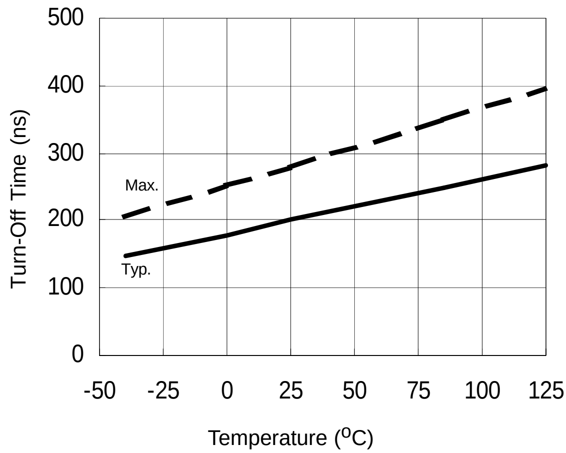


Figure 5A. Turn-Off Propagation Delay vs. Temperature

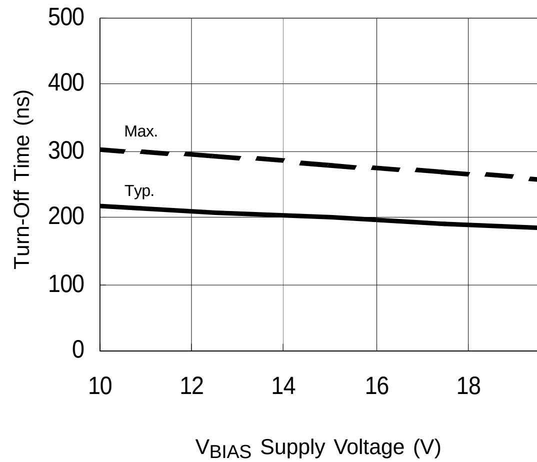


Figure 5B. Turn-Off Propagation Delay vs. Supply Voltage

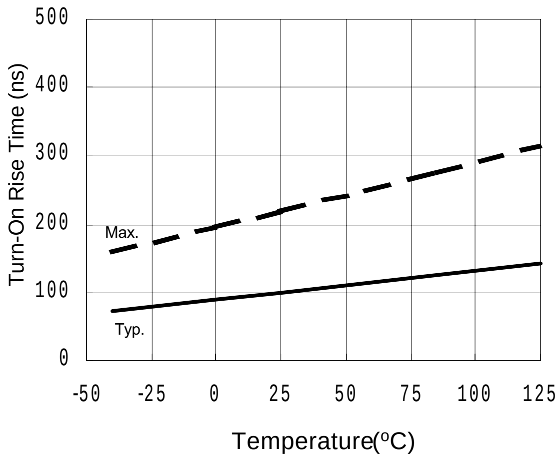


Figure 6A. Turn-On Rise Time vs. Temperature

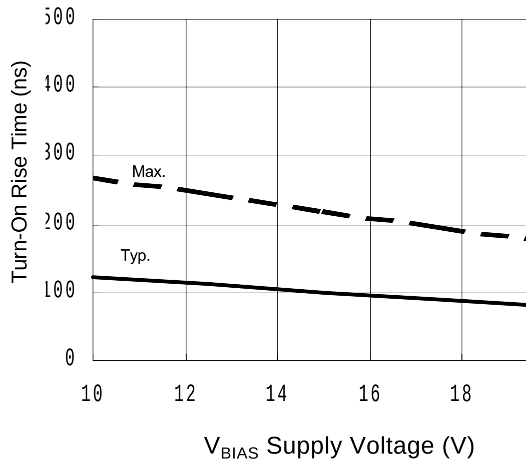


Figure 6B. Turn-On Rise Time vs. Supply Voltage

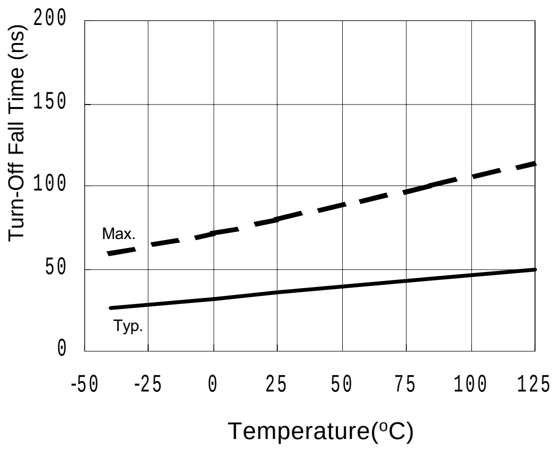


Figure 7A. Turn-Off Fall Time vs. Temperature

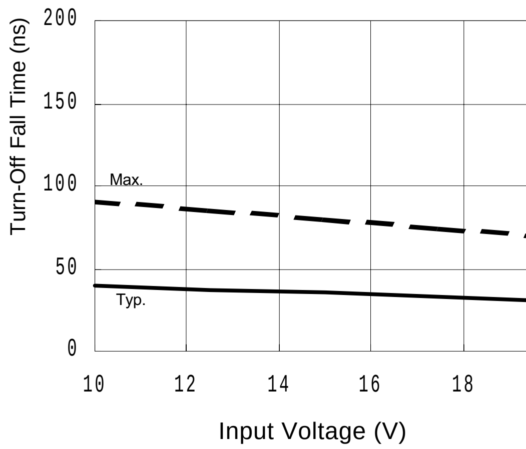


Figure 7B. Turn-Off Fall Time vs. Supply Voltage

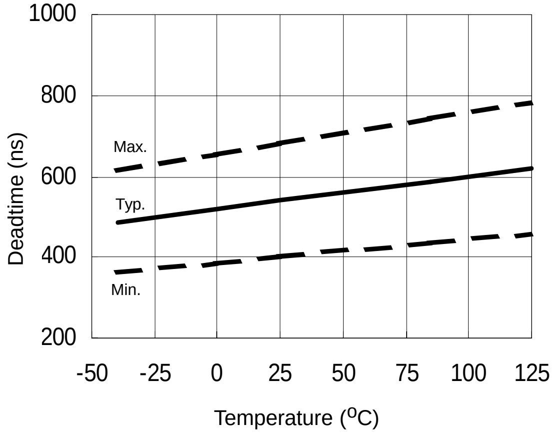


Figure 8A. Deadtime vs. Temperature

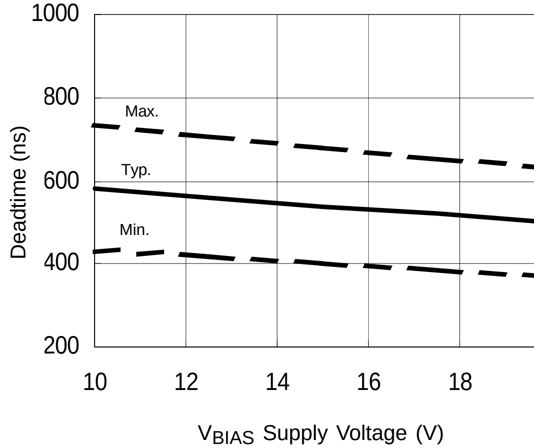


Figure 8A. Deadtime vs. Supply Voltage

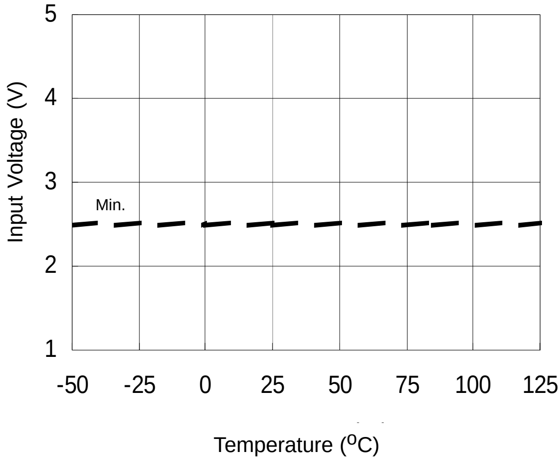


Figure 9A. Logic "1" Input Voltage vs. Temperature

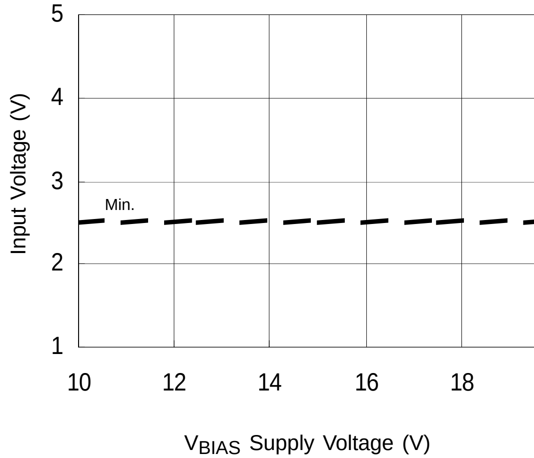


Figure 9B. Logic "1" Input Voltage vs. Supply Voltage

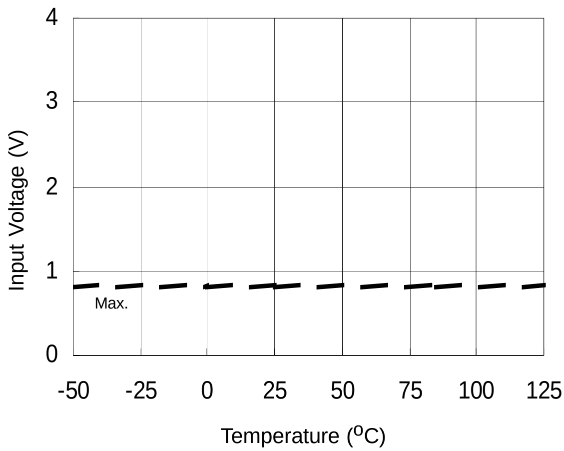


Figure 10A. Logic "0" Input Voltage vs. Temperature

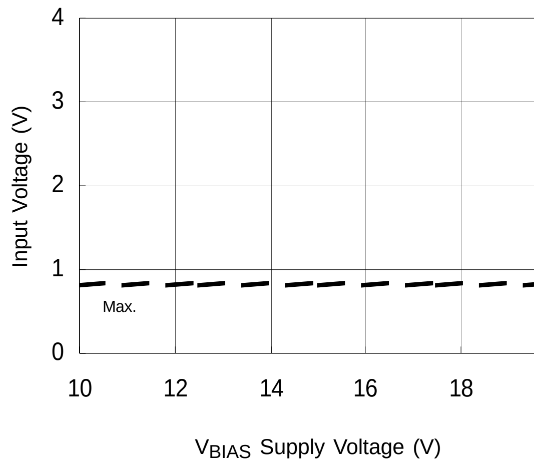


Figure 10A. Logic "0" Input Voltage vs. Supply Voltage

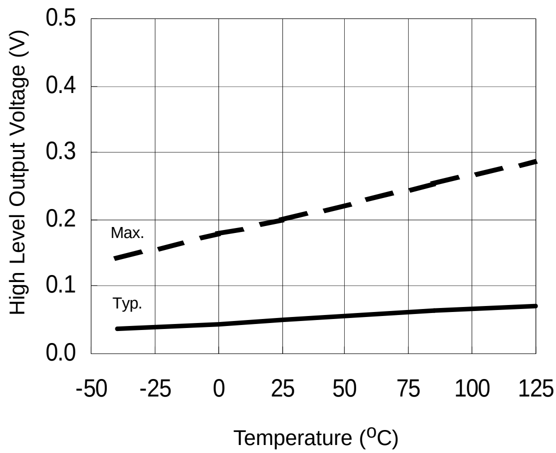


Figure 11A. High Level Output Voltage vs. Temperature

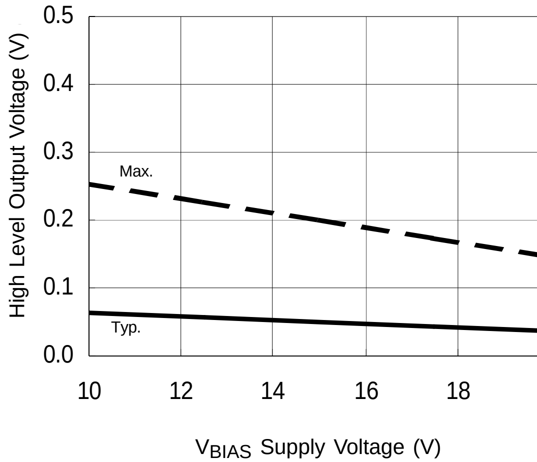


Figure 11A. High Level Output Voltage vs. Supply Voltage

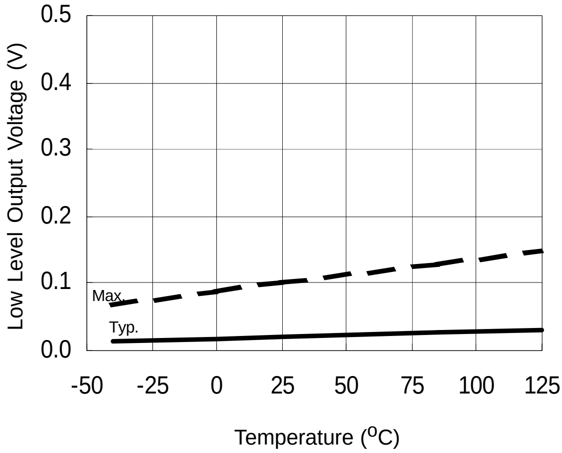


Figure 12A. Low Level Output Voltage vs. Temperature

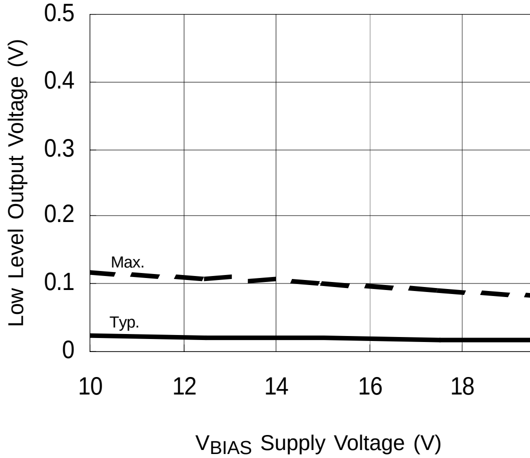


Figure 12B. Low Level Output Voltage vs. Supply Voltage

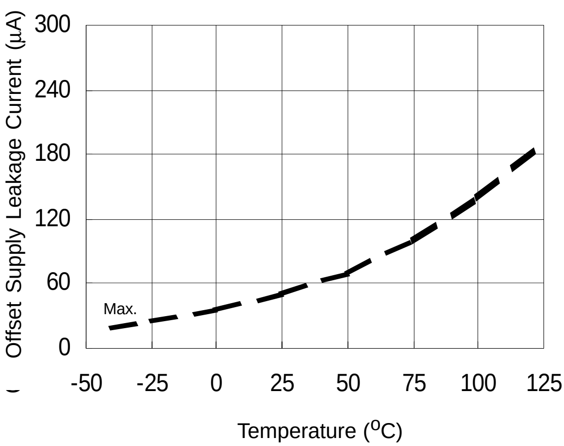


Figure 13A. Offset Supply Leakage Current vs. Temperature

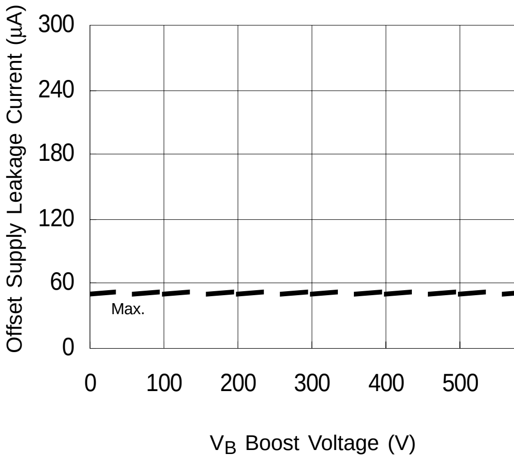


Figure 13A. Offset Supply Leakage Curr
vs. Supply Voltage

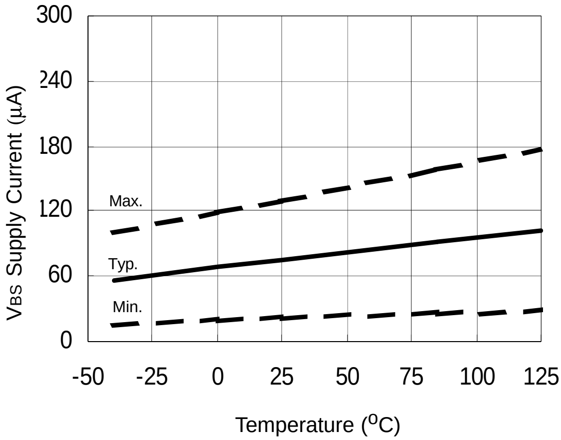


Figure 14A. V_{BS} Supply Current vs. Temperature

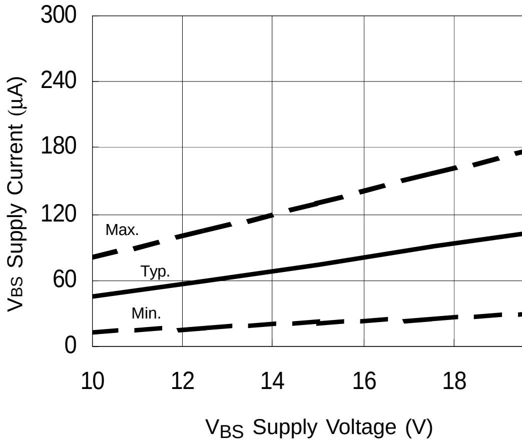


Figure 14B. V_{BS} Supply Current vs. Supply Voltage

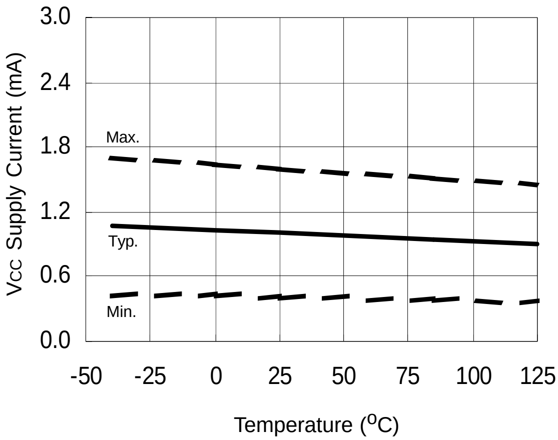


Figure 15A. V_{CC} Supply Current vs. Temperature

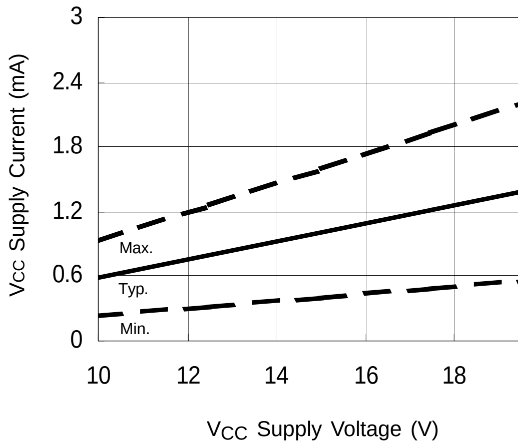


Figure 14B. V_{CC} Supply Current vs. Supply Voltage

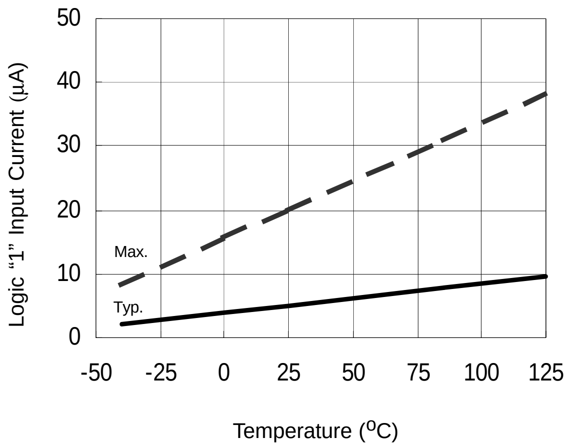


Figure 16A. Logic "1" Input Current vs. Temperature

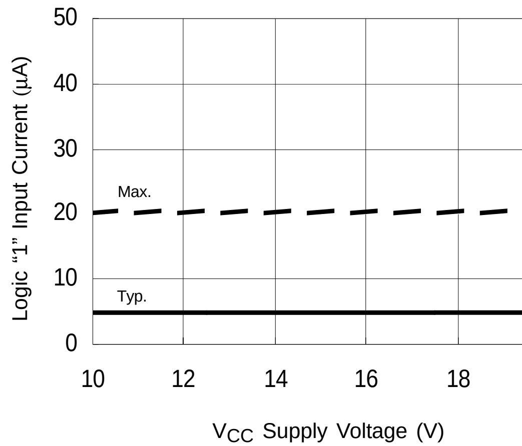


Figure 16B. Logic "1" Input Current vs. Supply Voltage

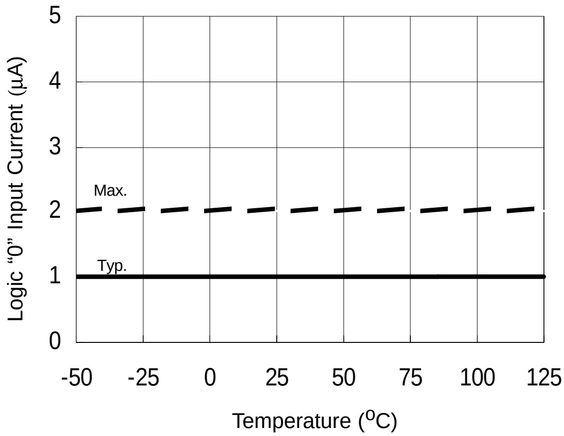


Figure 17A. Logic "0" Input Current vs. Temperature

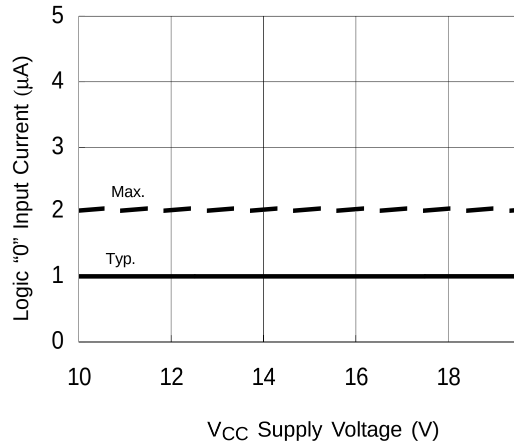


Figure 17B. Logic "0" Input Current vs. Supply Voltage

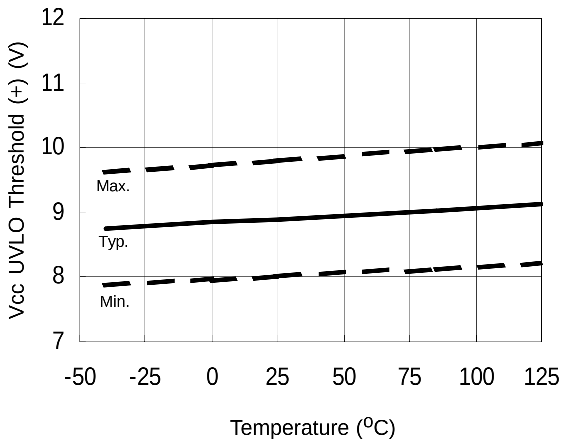


Figure 18. V_{CC} Undervoltage Threshold (+) vs. Temperature

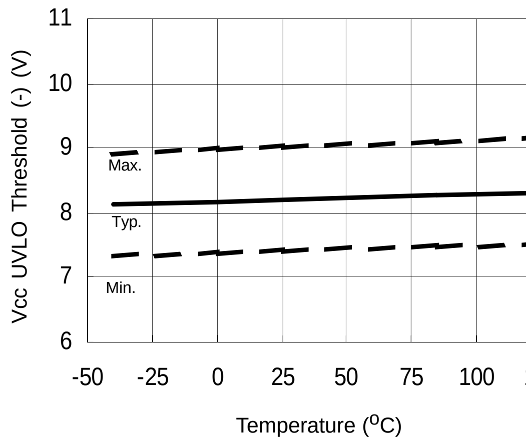


Figure 19. V_{CC} Undervoltage Threshold (- vs. Temperature

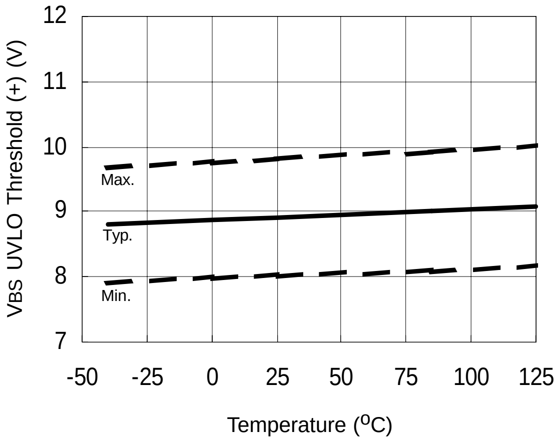


Figure 20. V_{BS} Undervoltage Threshold (+) vs. Temperature

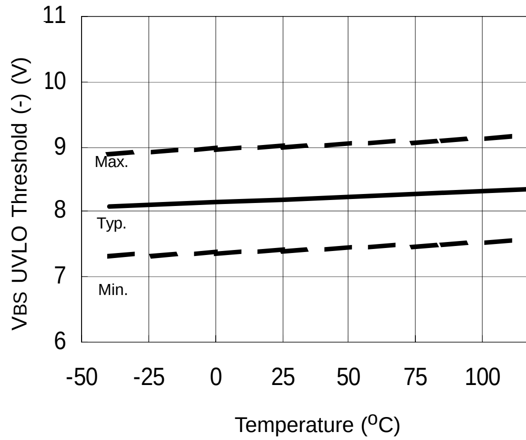


Figure 21. V_{BS} Undervoltage Threshold (- vs. Temperature

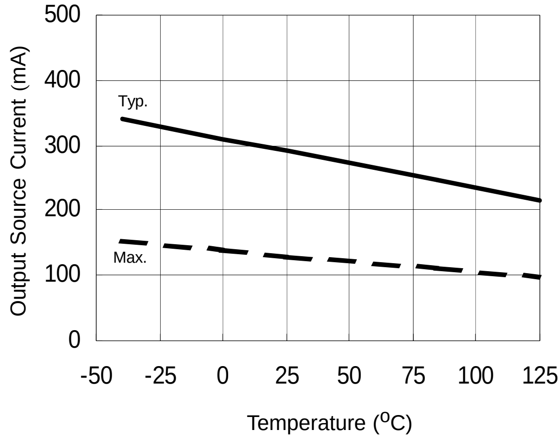


Figure 22A. Output Source Current vs. Temperature

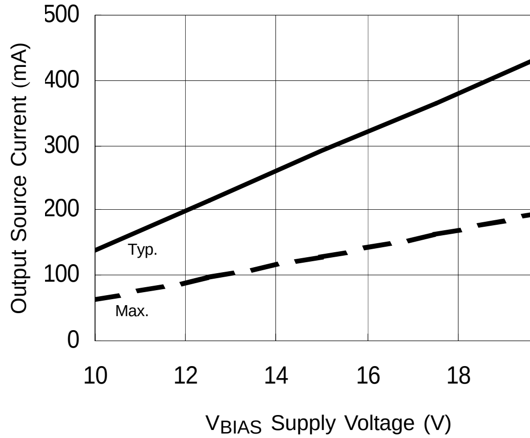


Figure 22B. Output Source Current vs. Supply Voltage

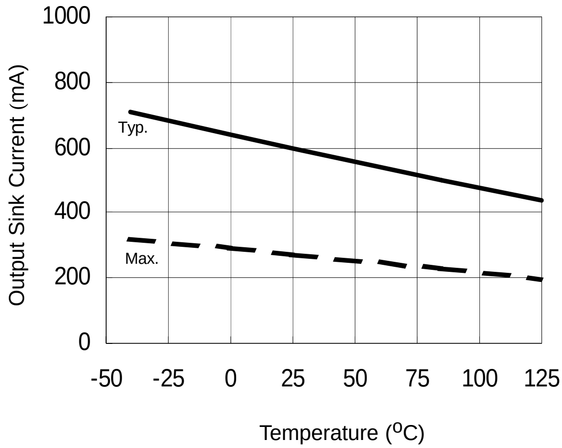


Figure 23A. Output Sink Current vs. Temperature

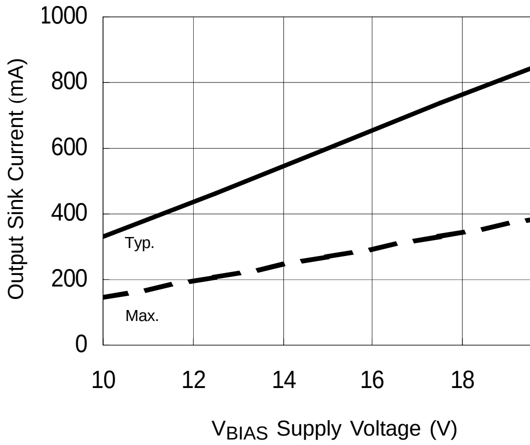


Figure 23B. Output Sink Current vs. Supply Voltage

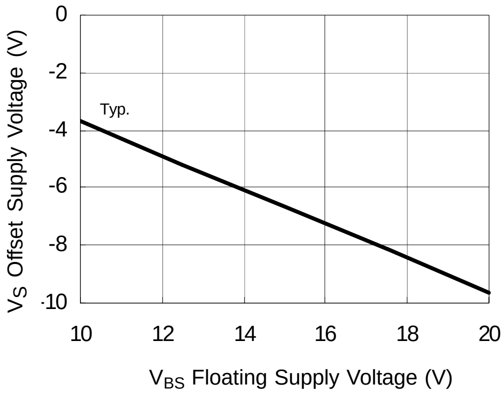


Figure 24. Maximum V_S Negative Offset vs. Supply Voltage

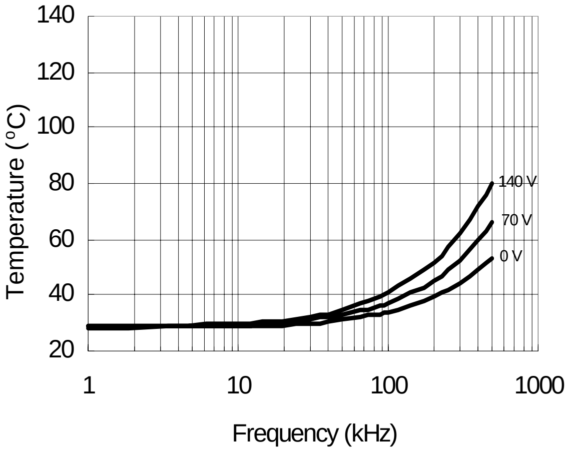


Figure 25. IRS2308 vs. Frequency (IRFBC20), R_{gate}=33Ω, V_{CC}=15 V

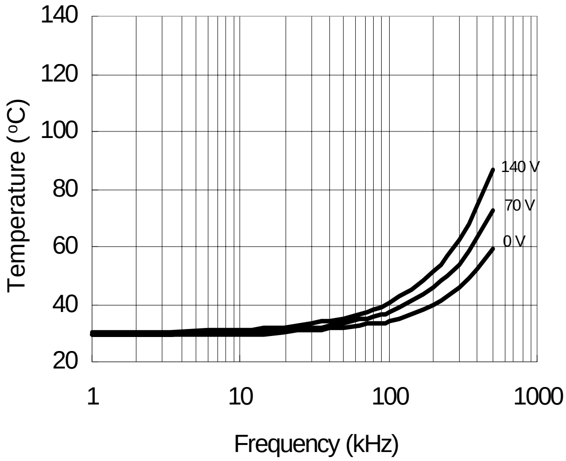


Figure 26. IRS2308 vs. Frequency (IRFBC30), R_{gate}=22Ω, V_{CC}=15 V

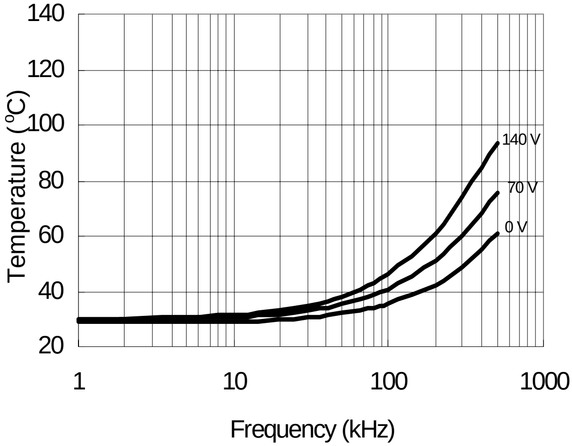


Figure 27. IRS2308 vs. Frequency (IRFBC40), R_{gate}=15Ω, V_{CC}=15 V

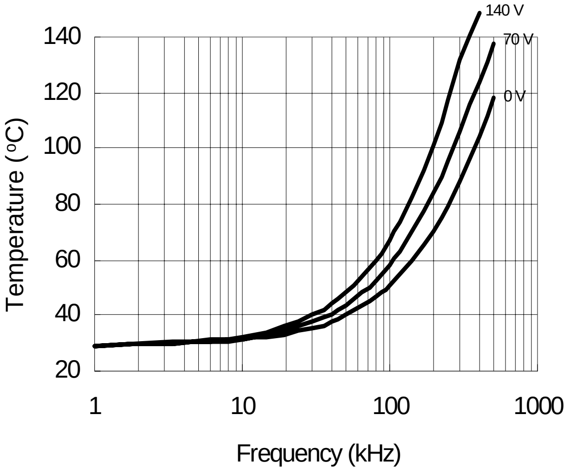


Figure 28. IRS2308 vs. Frequency (IRFPE50), R_{gate}=10Ω, V_{CC}=15 V

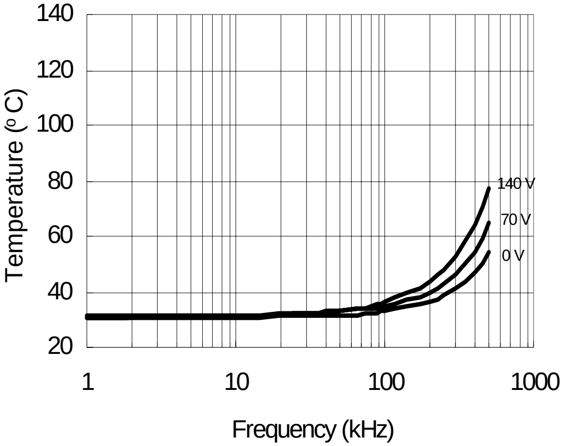


Figure 29. IRS2308S vs. Frequency (IRFBC20), R_{gate}=33 Ω, V_{CC}=15 V

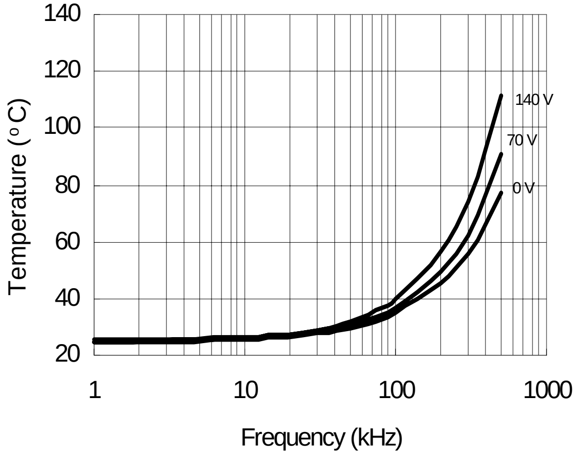


Figure 30. IRS2308S vs. Frequency (IRFBC30), R_{gate}=22 Ω, V_{CC}=15 V

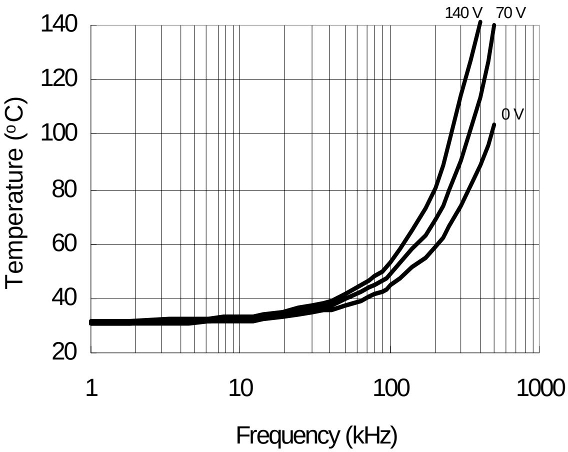


Figure 31. IRS2308S vs. Frequency (IRFBC40), R_{gate}=15 Ω, V_{CC}=15 V

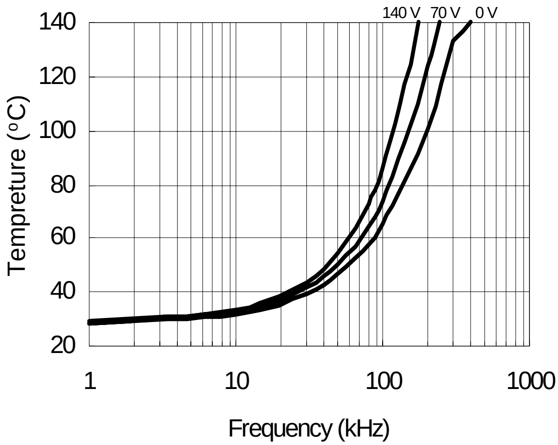
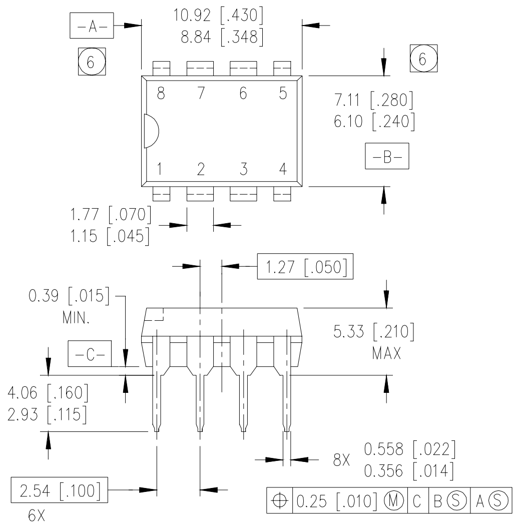
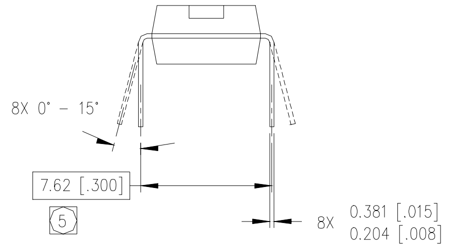


Figure 32. IRS2308S vs. Frequency (IRFPE50), R_{gate}=10 Ω, V_{CC}=15 V

Case outlines





NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

8-Lead PDIP

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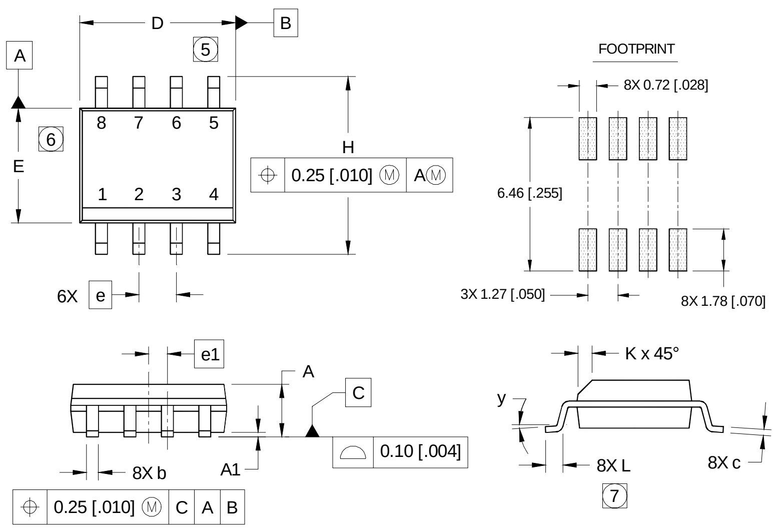

DIM	INCHES		MILLIMETE	
	MIN	MAX	MIN	M
A	.0532	.0688	1.35	1.7
A1	.0040	.0098	0.10	0.2
b	.013	.020	0.33	0.5
c	.0075	.0098	0.19	0.2
D	.189	.1968	4.80	5.0
E	.1497	.1574	3.80	4.0
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASI	
H	.2284	.2440	5.80	6.2
K	.0099	.0196	0.25	0.5
L	.016	.050	0.40	1.2
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

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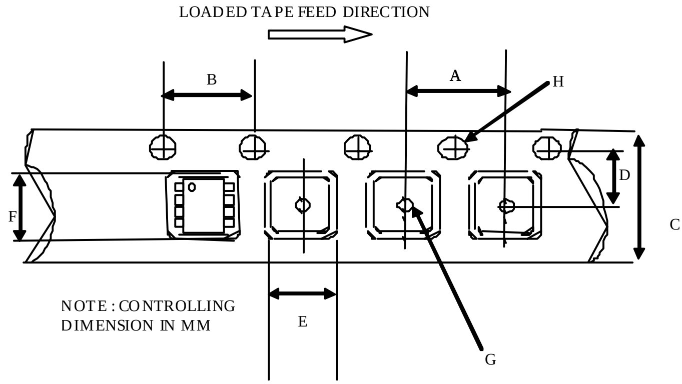
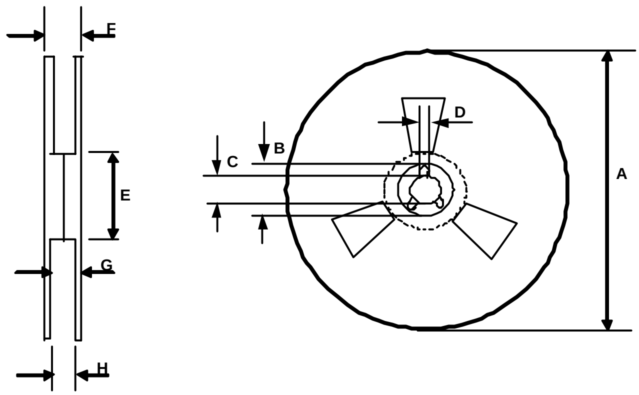
01-0021 11 (MS-01

Tape & Reel
8-Lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

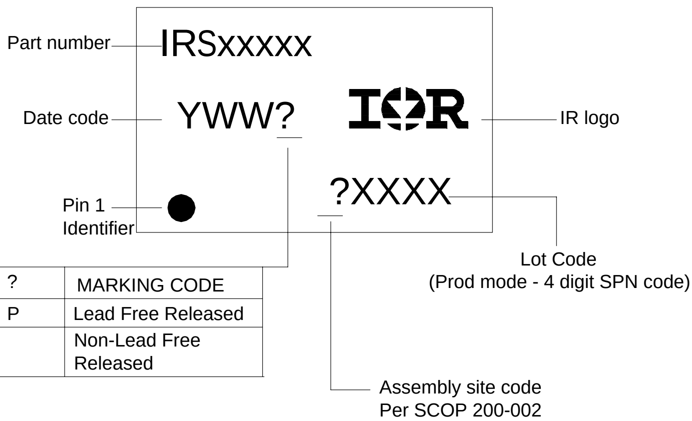
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

LEADFREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

ORDER INFORMATION

8-Lead PDIP IRS2308PbF
8-Lead SOIC IRS2308SPbF
8-Lead SOIC Tape & Reel IRS2308STRPbF

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The SOIC-8 is MSL2 qua
This product has been designed and qualified for the industrial
Qualification standards can be found at www.irf.com <http://www.irf.c

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Data and specifications subject to change without notice. 9/08/