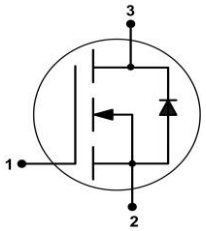
SIPMOS® Small-Signal-Transistor

Features

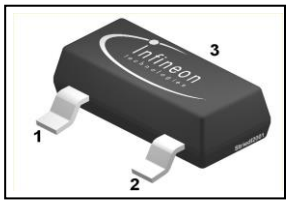
- n-channel
- enhancement mode
- Logic level (4.5V rated)
- d*v*/d*t* rated
- 100%lead-free; RoHS compliant
- Qualified according to AEC Q101
- Halogen-free according to IEC61249-2-21

Product Summary

V_{DS}	600	V
$R_{DS(on),max}$	500	Ω
I_D	0.021	A



PG-SOT-23



Type	Package	Pb-free	Halogen-free	Tape and Reel Information	Marking
BSS127	PG-SOT-23	Yes	Yes	H6327: 3000PCS/reel	SIs

Maximum ratings, at T_j=25 °C, unless otherwise specified

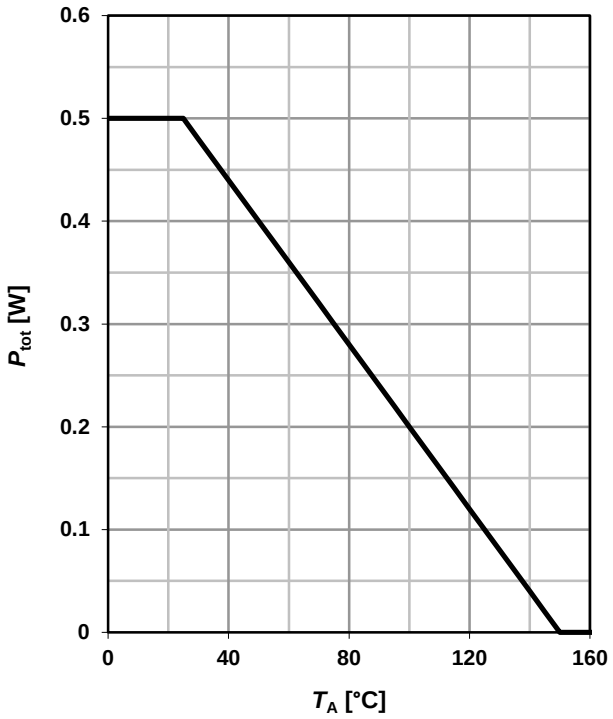
Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_A=25 °C	0.021	A
		T_A=70 °C	0.017	
Pulsed drain current	$I_{D,pulse}$	T_A=25 °C	0.09	
Reverse diode d*v*/d*t*	d*v*/d*t*	I_D=0.021 A, V_{DS}=480 V, d*i*/d*t*=200 A/µs, $T_{j,max}$=150 °C	6	kV/µs
Gate source voltage	V_{GS}		±20	V
ESD class (JESD22-A114-HBM)			0 (<250)	
Power dissipation	P_{tot}	T_A=25 °C	0.50	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - minimal footprint	R_{thJA}		-	-	250	K/W
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250 µA	600	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=8 µA	1.4	2.0	2.6	
Drain-source leakage current	$I_{D (off)}$	V_{DS}=600 V, V_{GS}=0 V, T_j=25 °C	-	-	0.1	µA
		V_{DS}=600 V, V_{GS}=0 V, T_j=150 °C	-	-	10	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=0.016 A	-	330	600	Ω
		V_{GS}=10 V, I_D=0.016 A	-	310	500	
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=0.01 A	0.007	0.015	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	21	28	pF
Output capacitance	C_{oss}		-	2.4	3	
Reverse transfer capacitance	C_{rss}		-	1.0	1.5	
Turn-on delay time	$t_{d(on)}$	V_{DD}=300 V, V_{GS}=10 V, I_D=0.01 A, $R_{G,ext}$=6 Ω	-	6.1	19.0	ns
Rise time	t_r		-	9.7	14.5	
Turn-off delay time	$t_{d(off)}$		-	14	21	
Fall time	t_f		-	115	170	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=300 V, I_D=0.01 A, V_{GS}=0 to 10 V	-	0.07	0.10	nC
Gate to drain charge	Q_{gd}		-	0.31	0.5	
Gate charge total	Q_g		-	0.65	1.0	
Gate plateau voltage	$V_{plateau}$		-	3.56	-	V
Reverse Diode						
Diode continous forward current	I_S	T_A=25 °C	-	-	0.016	A
Diode pulse current	$I_{S,pulse}$		-	-	0.09	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=0.016 A, T_j=25 °C	-	0.82	1.2	V
Reverse recovery time	t_{rr}	V_R=300 V, I_F=0.016 A, di_F/dt =100 A/µs	-	160	240	ns
Reverse recovery charge	Q_{rr}		-	13.2	19.8	nC

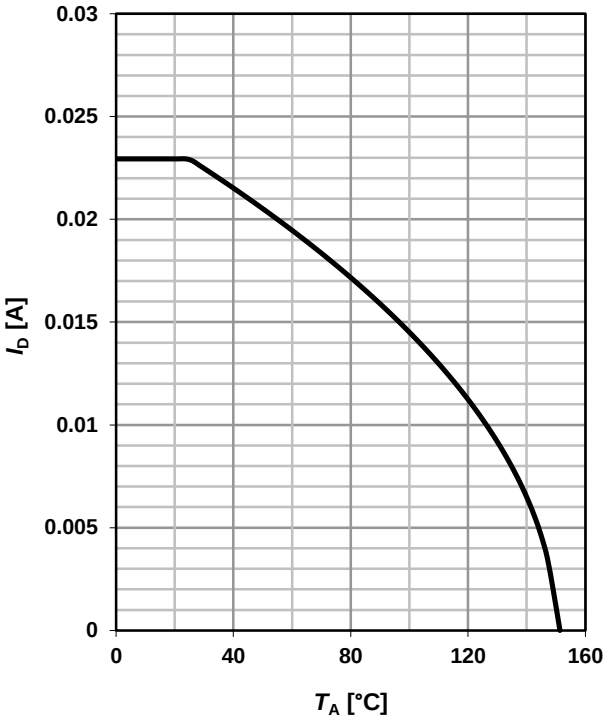
1 Power dissipation

$P_{tot}=f(T_A)$



2 Drain current

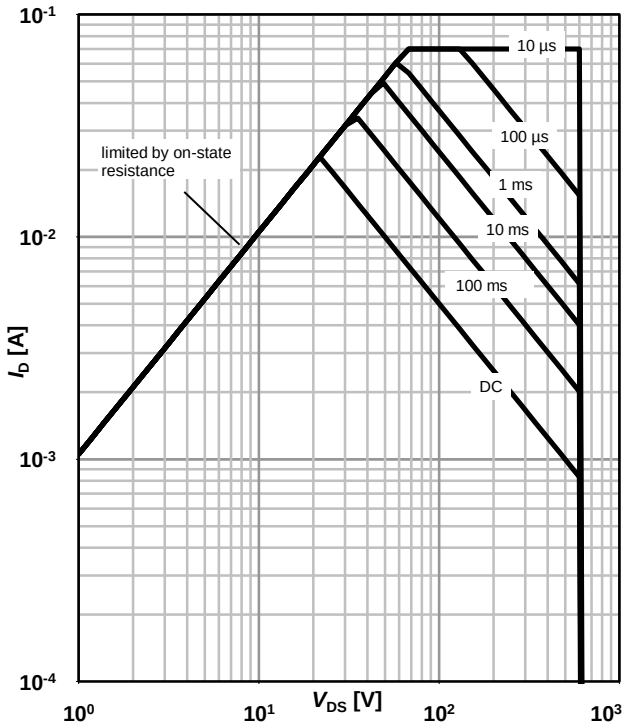
$I_D=f(T_A)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_A=25$ °C; $D=0$

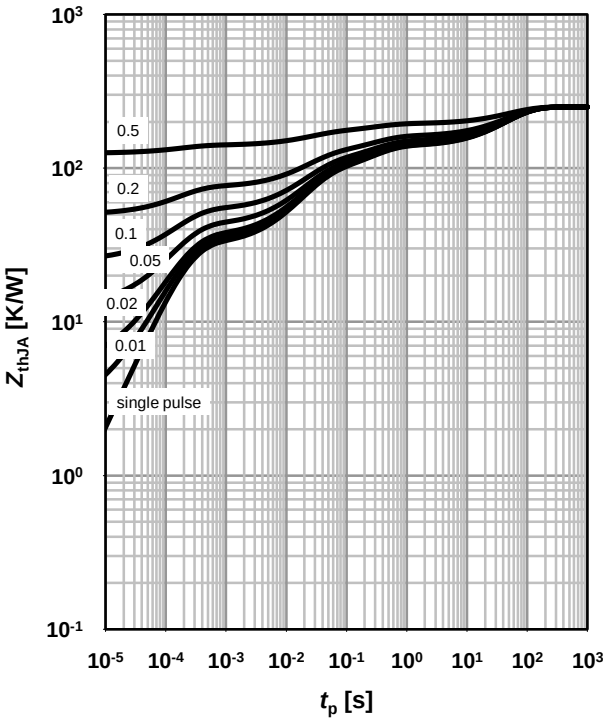
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJA}=f(t_p)$

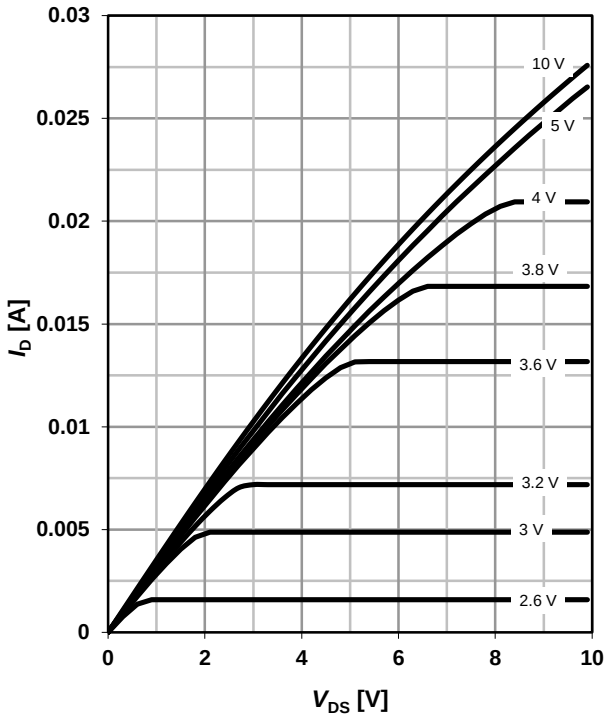
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

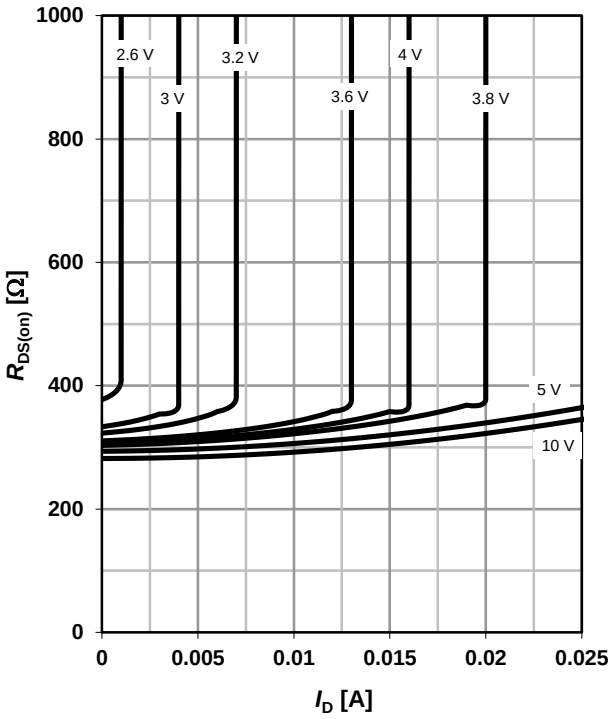
parameter: V_{GS}



6 Typ. drain-source on resistance

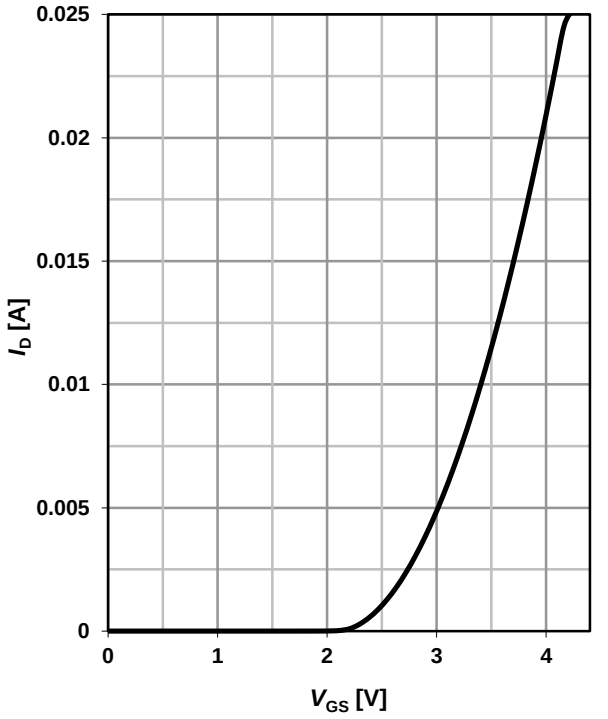
$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

parameter: V_{GS}



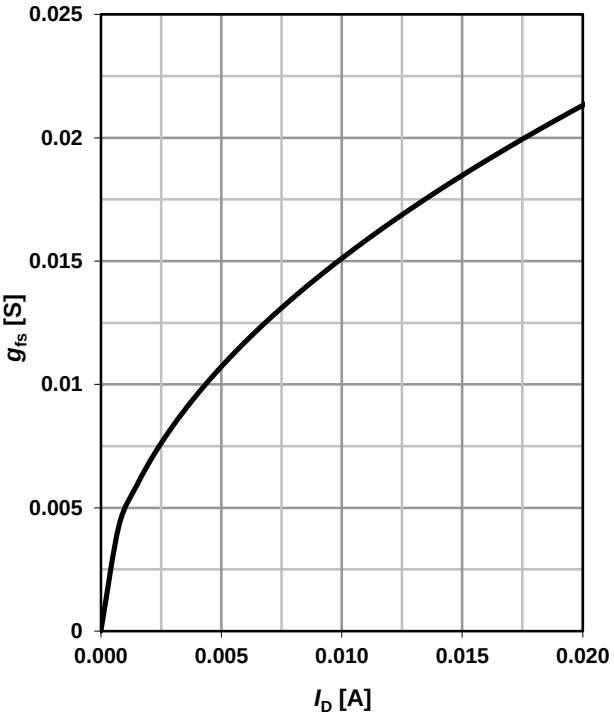
7 Typ. transfer characteristics

$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$



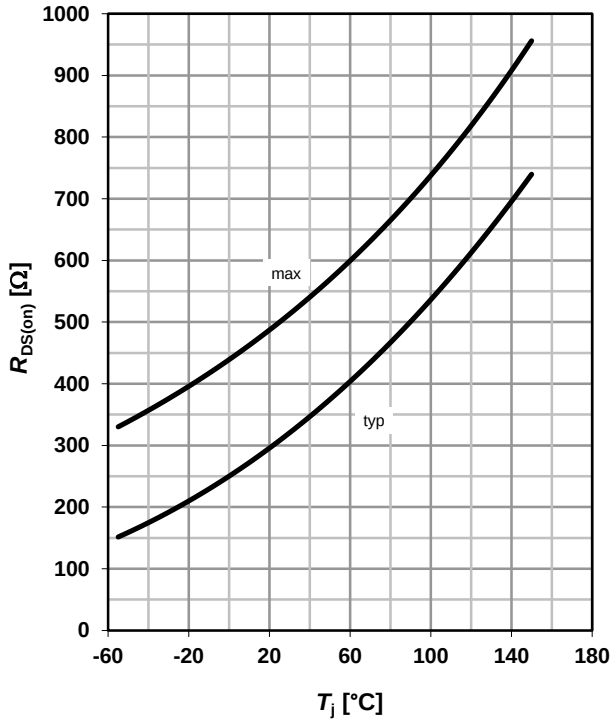
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



9 Drain-source on-state resistance

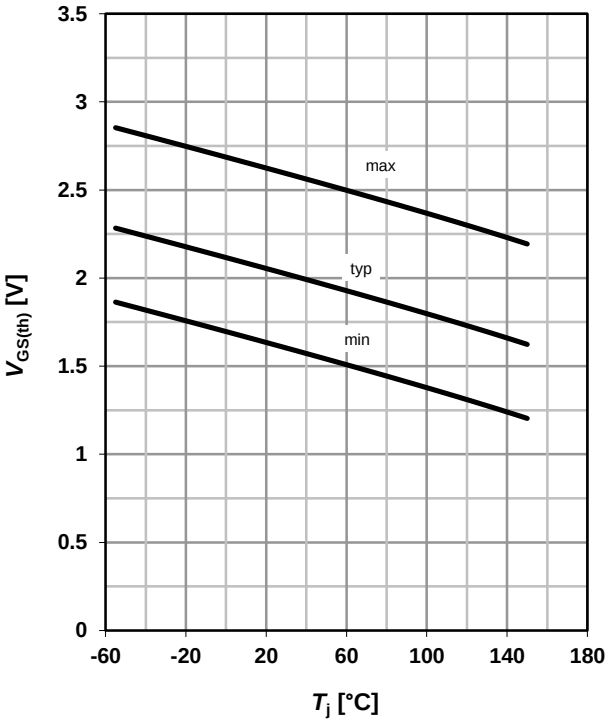
$R_{DS(on)}=f(T_j)$; $I_D=0.016$ A; $V_{GS}=10$ V



10 Typ. gate threshold voltage

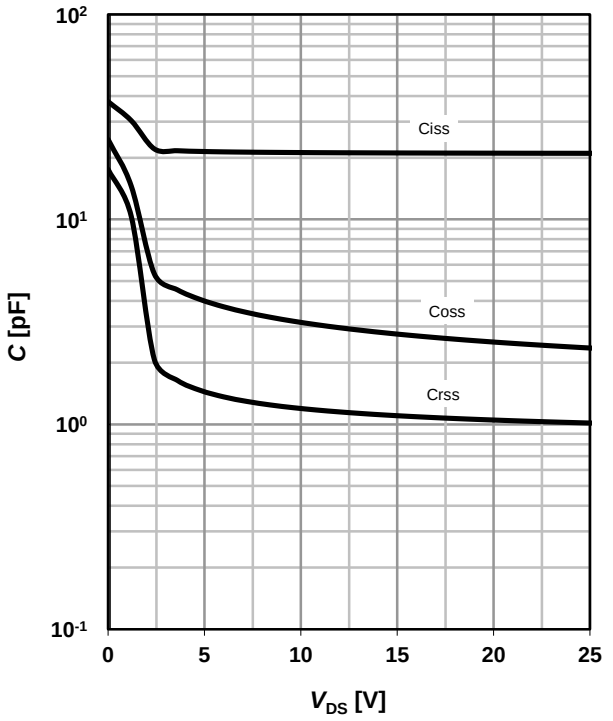
$V_{GS(th)}=f(T_j)$; $V_{DS}=V_{GS}$; $I_D=8$ µA

parameter: I_D



11 Typ. capacitances

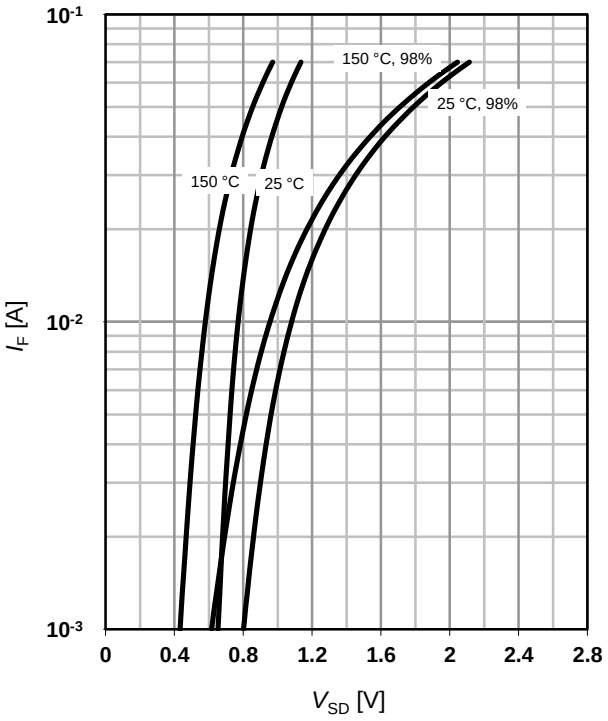
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz; $T_j=25$°C



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

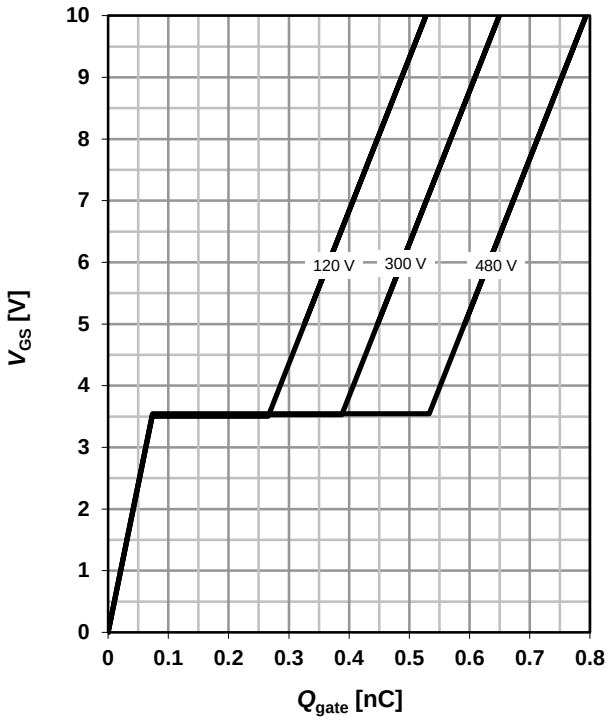
parameter: T_j



13 Typ. gate charge

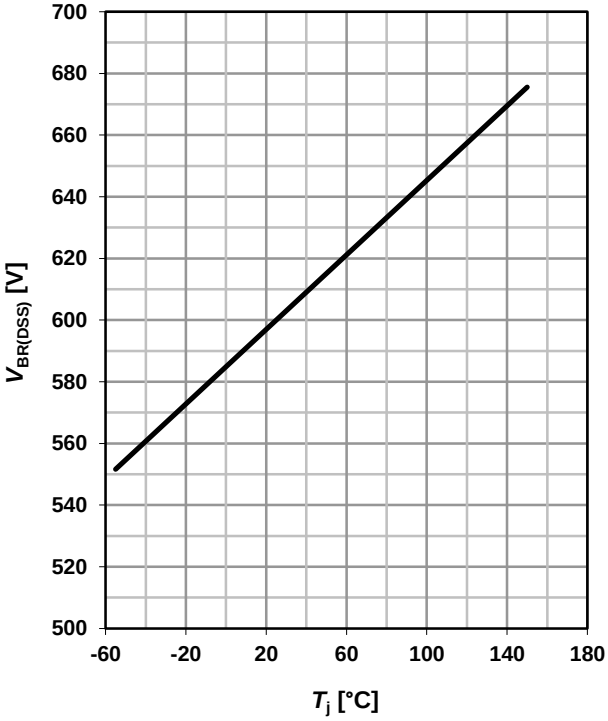
V_{GS}=f(Q_{gate}); I_D=0.01 A pulsed

parameter: V_{DD}

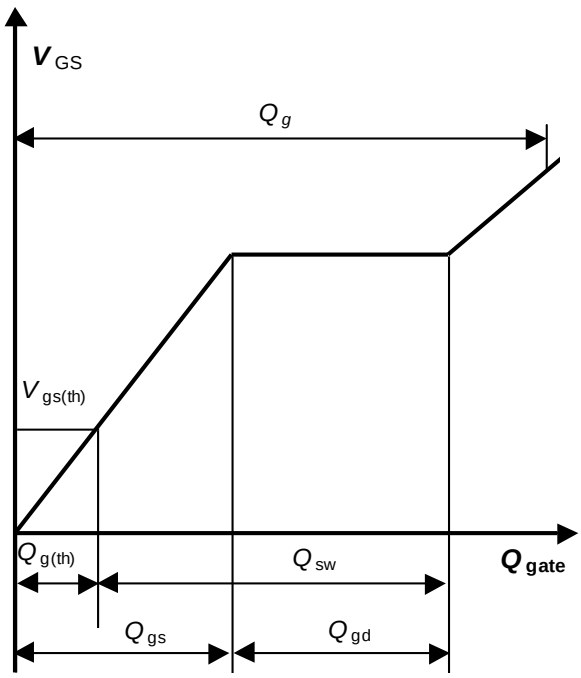


14 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=250 µA



15 Gate charge waveforms



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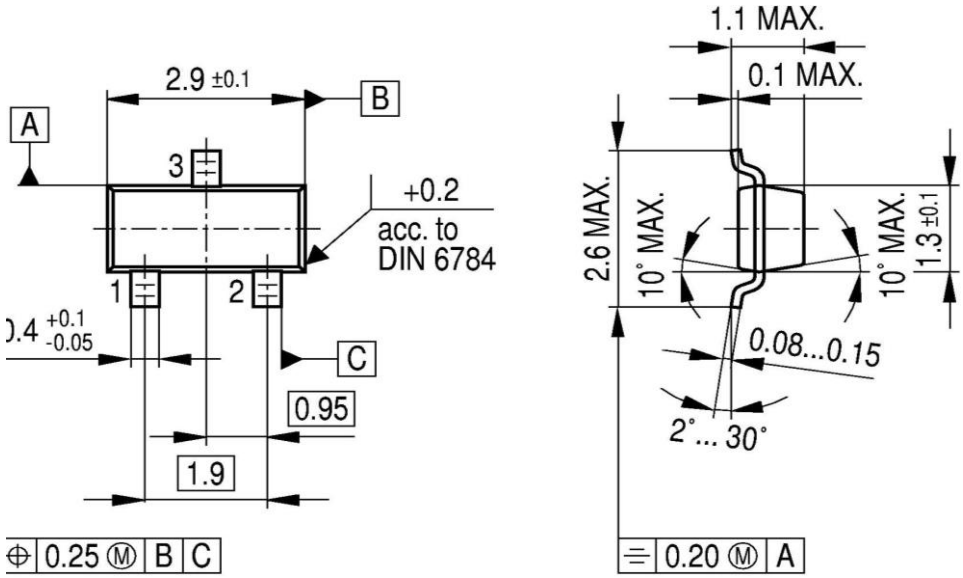
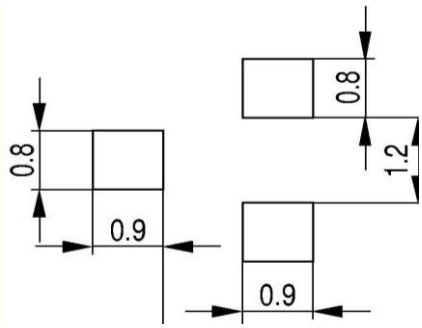
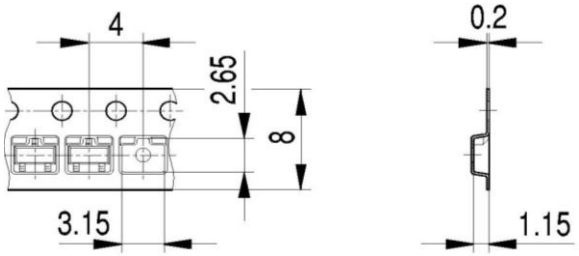
Package Outline:



Footprint:



Packaging:



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