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Application Note

AN-EVAL 2x8-ISO1H811G-1

Coreless Transformer Isolated High Side Switch Evaluation Board 2 x 8 Channel 0.6A with ISO1H811G

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Power Management & Drives

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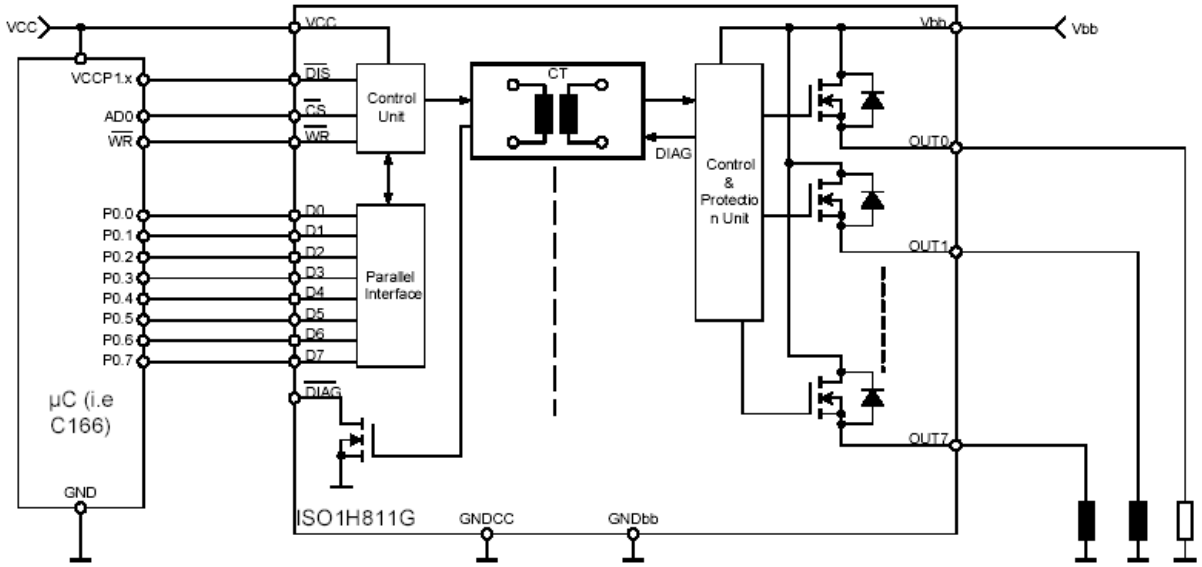
Introduction

Application

This Application Note describes a Demoboard with an isolated 2 x 8 Channel 0.6A Digital Output. The board is designed to show the performance of the ISOFACE® Part **ISO1H811G** providing an Isolated Interface output to drive resistive, capacitive or inductive loads directly. The input can be driven by applying 3.3V/5V CMOS compatible signals to connector K3 or using the On-Board DIP switches S1 and S2. The input operates in Micro Controller Mode by using Chip Select and Write Signals or in Direct Control Mode by pulling these signals to GND and setting the Data Input D0 to D7. The Output consists of 2 times 8 Channel High Side Switches with 0.6A Current rating. The Output is protected with a channel selected over-temperature switch (to off).



Typical Application

ISO1H811G

The **ISO1H811G** is a galvanic isolated 8-bit data interface in P-DSO-36 package that provides 8 fully protected high-side power switches that are able to handle currents up to 625 mA.

An 8-bit parallel microcontroller (µC) compatible interface allows connecting the IC directly to a µC system. The input interface also supports a direct control mode and is designed to operate with 3.3V/5V CMOS compatible levels. The data transfer from input to output side is realized by the integrated Coreless Transformer Technology.

The ISOface™ **ISO1H811G** includes 8 high-side power switches that are controlled by means of the integrated parallel interface. The interface is 8-bit µC compatible. Furthermore, a direct control mode can be selected that allows the direct control of the outputs OUT0...OUT7 by means of the inputs D0...D7 without any additional logic signal. The ISOFACE® can replace 8 optocouplers and the 8 high-side switches in conventional I/O-Applications as galvanic isolation is implemented by means of the integrated coreless transformer technology. The µC compatible interface allows a direct connection to the ports of a microcontroller without the need for other components. Each of the 8 high-side power switches is protected against short to Vbb, overload, over-temperature and against over-voltage by an active zener clamp.

The diagnostic logic on the power chip recognizes the over-temperature information of each power transistor. That information is sent via the internal coreless transformer to the pin DIAG at the input interface.

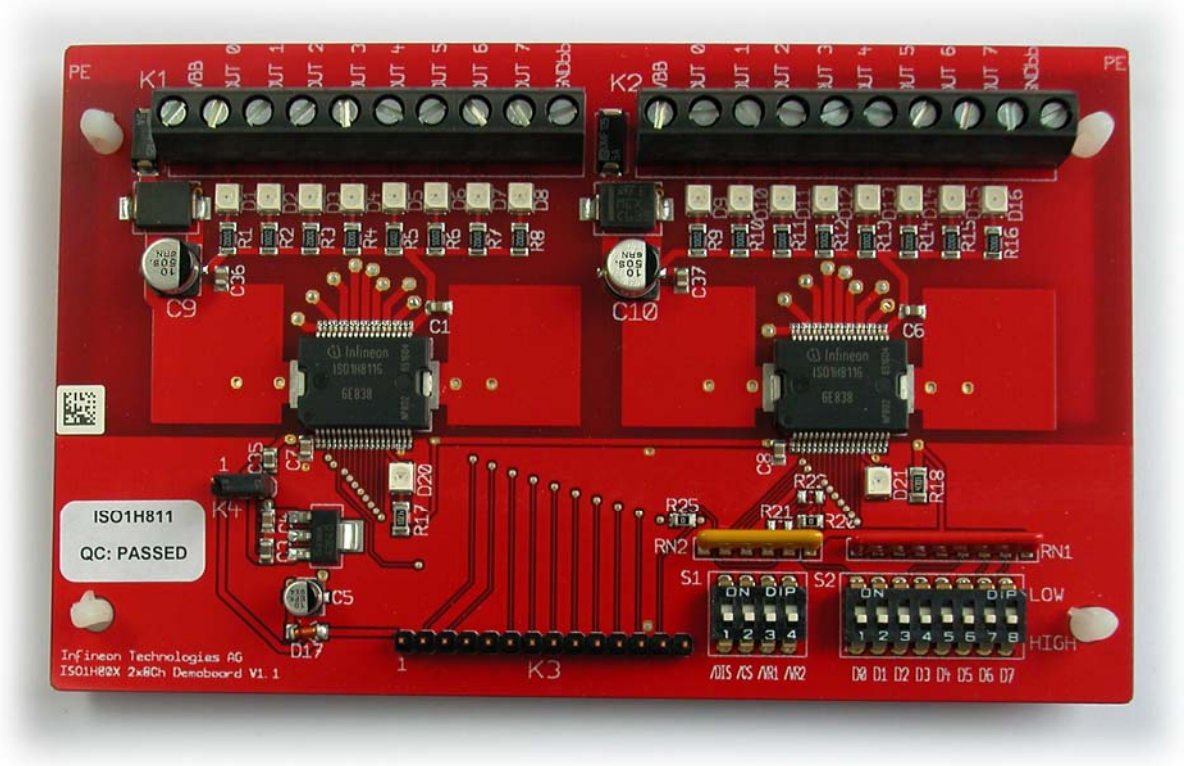


Figure 1– EVAL 2x8-ISO1H811G

Board Characteristics

Parameter	Min.	Max	Unit	Remarks
VCC Input Voltage	3.0	5.5	V	K4 Jumper 1-2
	8	12	V	K4 Jumper 2-3
VBB Input Voltage	11	45	V	
Input Signals	-0.3	0.3xVCC	V	low level
	0.7xVCC	VCC+0.3V	V	high level
Output Current Limit	0.7	1.9	A	
Output Clamping Voltage	47	60	V	

Functional Description

Power Supply

The Demo Board contains 2 galvanic isolated voltage domains that are independent from each other. The input interface is supplied by Pin1 and Pin14 of K3. Jumper K4 selects either direct supply with 3.3V/5V VCC (Jumper 1-2) or using the on-board 5V voltage regulator (Jumper 2-3). The output stage is supplied at pin1 and 10 of K2, and K2 with Vbb voltage. The different voltage domains can be switched on at different times. The output stage is only enabled once the input stage enters a stable state.

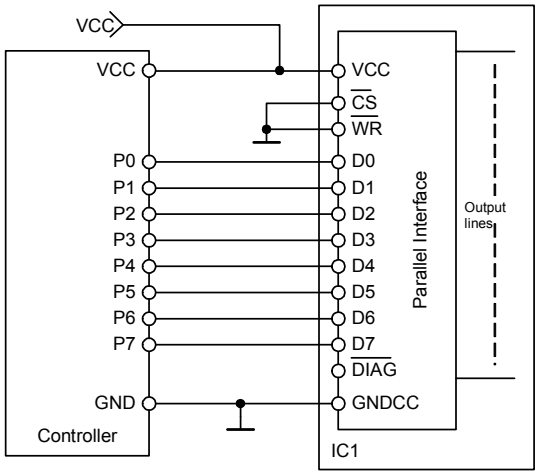
Parallel Interface

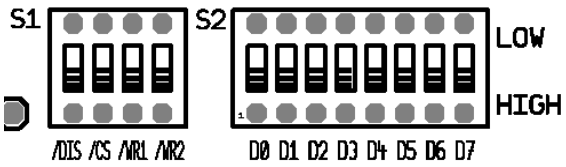
The ISO1H811G contains a parallel interface that can be directly controlled by the microcontroller output signals. The parallel interface can also be switched over to a direct control that allows direct changes of the outputs OUT0 ... OUT7 by means of the corresponding inputs D0 ... D7 on the Demo Board without additional logic signals. To activate the parallel direct control mode, both the /CS pin and /WR pin must be connected to ground.

Direct Control Mode

Beside the use of the parallel µC compatible interface, a parallel direct control mode can be chosen. In this mode, the output OUT0...OUT7 can be directly controlled via the inputs D0...D7 without the need for additional logic signals. To activate this mode, pin CS and WR must be connected to ground. To activate the parallel direct control mode, both pins /CS and /WR must be connected to ground.

On the Demo Board, this Mode can be easily operated by using the DIP Switches S1 and S2.





Truth Table for manual DIP-switch control:

Input				Output	
	/DIS	**/WRx**	**/CS**	**Dn**	**OUTn**
Direct Control Mode	H	L	L	H	ON
	H	L	L	L	OFF
Output Disabled	L	X	X	X	OFF

H = High Voltage Level; L = Low Voltage Level; X = Don't Care;

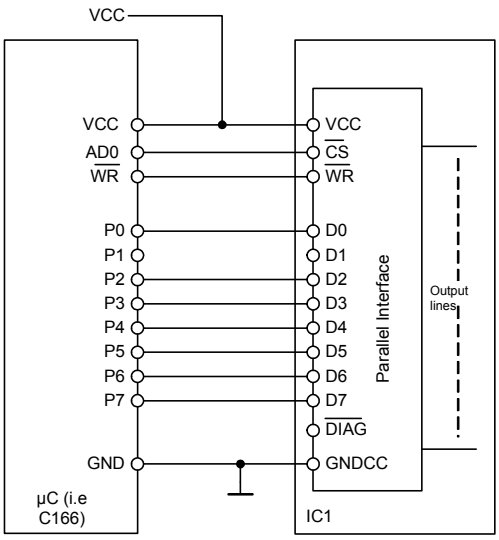
µC Control Mode

/CS - Chip select. The system microcontroller selects the ISO1H811G by means of the CS pin. Whenever the pin is in a logic low state, data can be transferred from the µC.

/WR - Write. The system controller enables the write procedure in the ISO1H811G by means of the signal WR. A logic low state signal at pin WR writes the input data into the input latches when the CS pin is in a logic low state.

D0…D7. The parallel input data is transferred to the input latches with a high-to-low transition of the signal /WR (write) while the /CS is logic low. Then a low-to-high transition of /CS transfers the data of the input latches to the output buffer.

The µC Control Mode can be operated by connecting a Processor Board to the corresponding Signals of Connector K3.

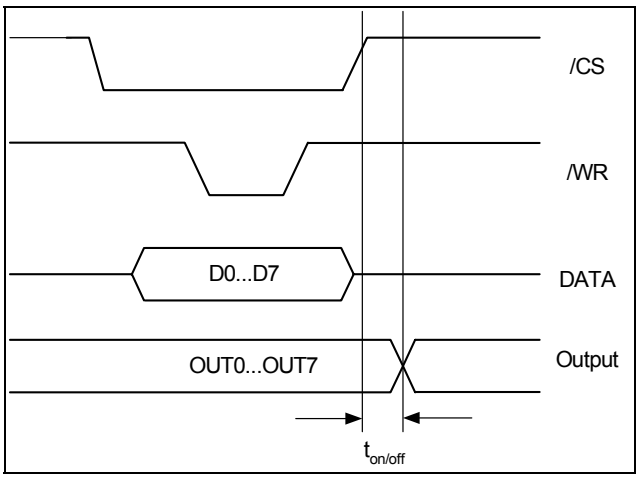


Truth Table for µC control:

Input				Output	
	/DIS	**/WR**	**/CS**	**Dn**	**OUTn**
µC Control Mode	H	↑	↑	H	ON
	H	↑	↑	L	OFF
Output Disabled	L	X	X	X	OFF

H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = positive slope

Timing Diagram µC Control Mode:



Output Stage

Each channel contains a high-side vertical power FET that is protected by embedded protection functions. The continuous current for each channel is 625mA (all channels ON).

Each output is independently controlled by an output latch and a common reset line via the pin /DIS that disables all eight outputs and reset the latches. A logic high input data bit turns the respective output channel ON. A logic low data bit turns that output channel OFF.

Power Transistor Over-Voltage Protection

Each of the eight output stages has it own zener clamp that causes a voltage limitation at the power transistor when inductive loads are switched off. V_{ON} is then clamped to 47V (min.).

Inductive and over-voltage output clamp (each channel)

Energy is stored in the load inductance.

$$E_L = 1 / 2 \times L \times I_L^2$$

Inductive load switch-off energy dissipation (each channel)

While demagnetizing the load inductance, the energy dissipation in the DMOS with an approximate solution for $R_L > 0\Omega$ is:

$$E_{AS} = \frac{I_L \times L}{2 \times R_L} \times (V_{bb} + |V_{ON(CL)}|) \times \ln\left(1 + \frac{I_L \times R_L}{|V_{ON(CL)}|}\right)$$

Power Transistor Over-current Protection

The outputs are provided with a current limitation that enters a repetitive switched mode after an initial peak current has been exceeded. The initial peak short circuit current limit $I_{L(SCp)}$ is set to a minimum of 0.7A at T_j = 125°C. During the repetitive mode, short circuit current limit $I_{L(SCr)}$ is set to 1.1A (typ.). If this operation leads to an over-temperature condition, a second protection level (T_j > 135°C) will change the output into a low Pulse-Width Modulated duty cycle (selective thermal shutdown with restart) to prevent critical chip temperatures.

Common Diagnostic Output

The over-temperature detection information of the channels is OR-wired in the common diagnostic output block. The information is send via the integrated coreless transformer to the input interface. The output stage at pin DIAG has an open drain functionality combined with a current source. The red LED D20 and D21 show the current state of the DIAG output.

LED ON: one of the Channels has over-temperature or the VBB Supply is below the operating range

Connectors

K1, K2:

	K1	K2
1	VBB1	VBB2
2	OUT10	OUT20
3	OUT11	OUT21
4	OUT12	OUT22
5	OUT13	OUT23
6	OUT14	OUT24
7	OUT15	OUT25
8	OUT16	OUT26
9	OUT17	OUT27
10	GNDbb1	GNDbb2

K3:

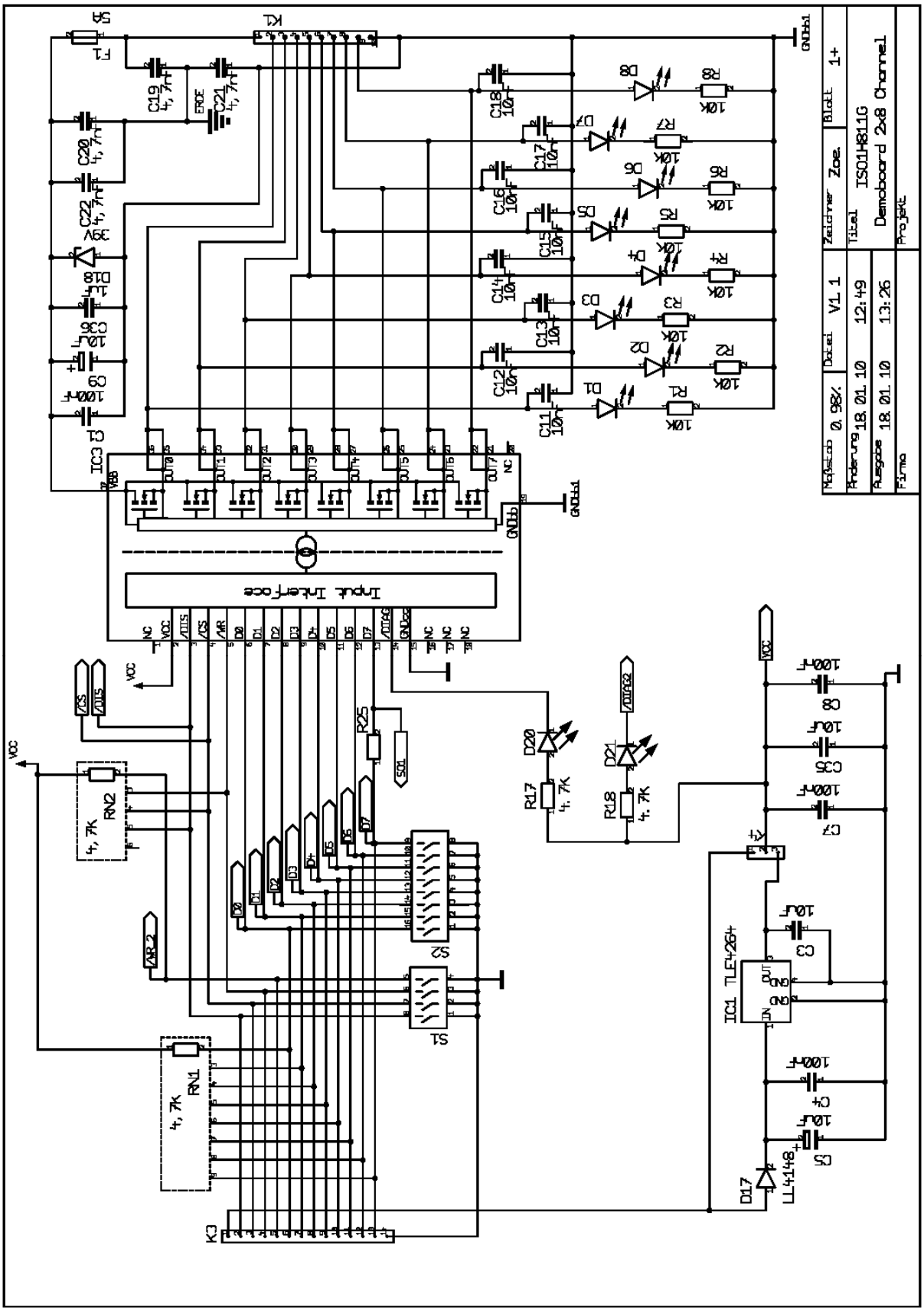
1	+Vin/VCC
2	/DIS
3	/CS
4	/WR1
5	/WR2
6	D0
7	D1
8	D2
9	D3
10	D4
11	D5
12	D6
13	D7
14	GNDCC

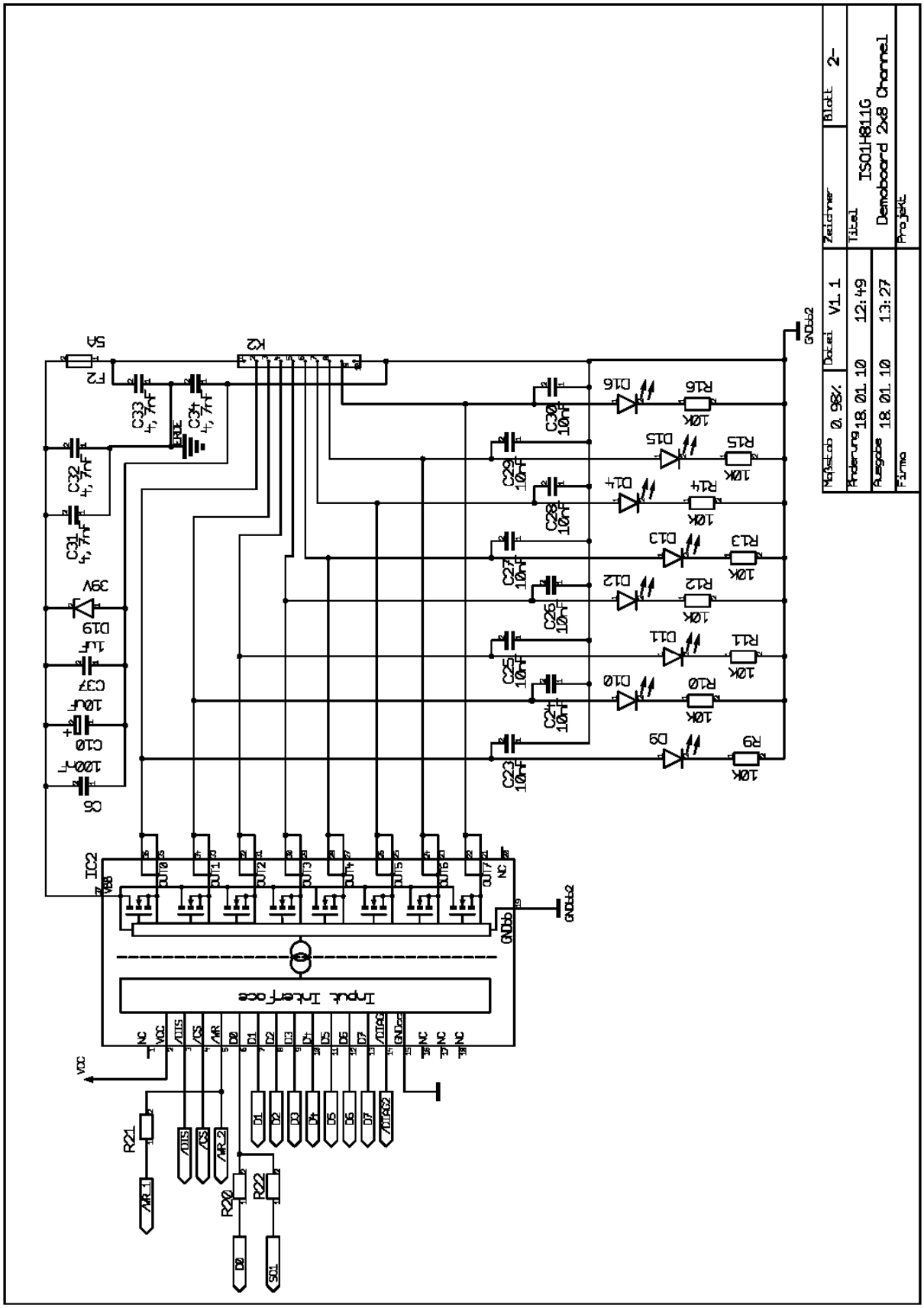
Note: When you are using connector K3 for applying Micro - Controller Signals to the Board, make sure that all DIP Switches are in “High” state!

K4:

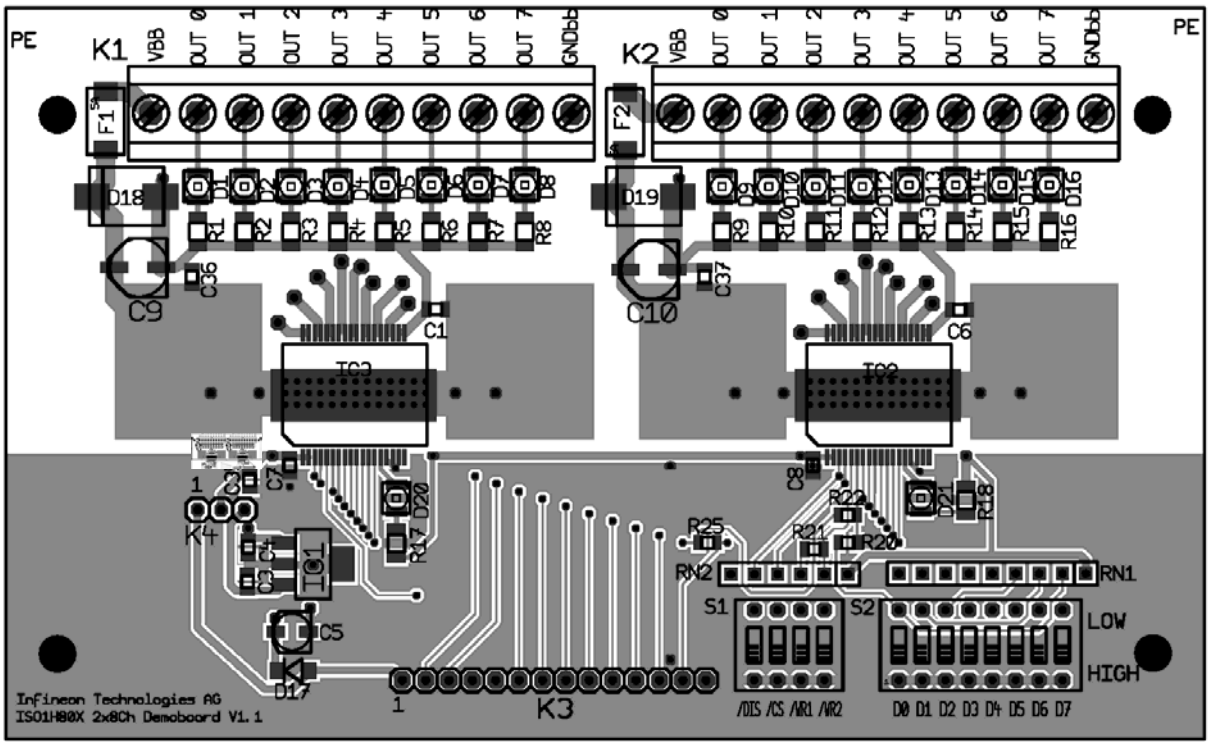
Jumper 1 - 2	VCC 3,3V/5V
Jumper 2 - 3	Vin 8V …12V

Schematic

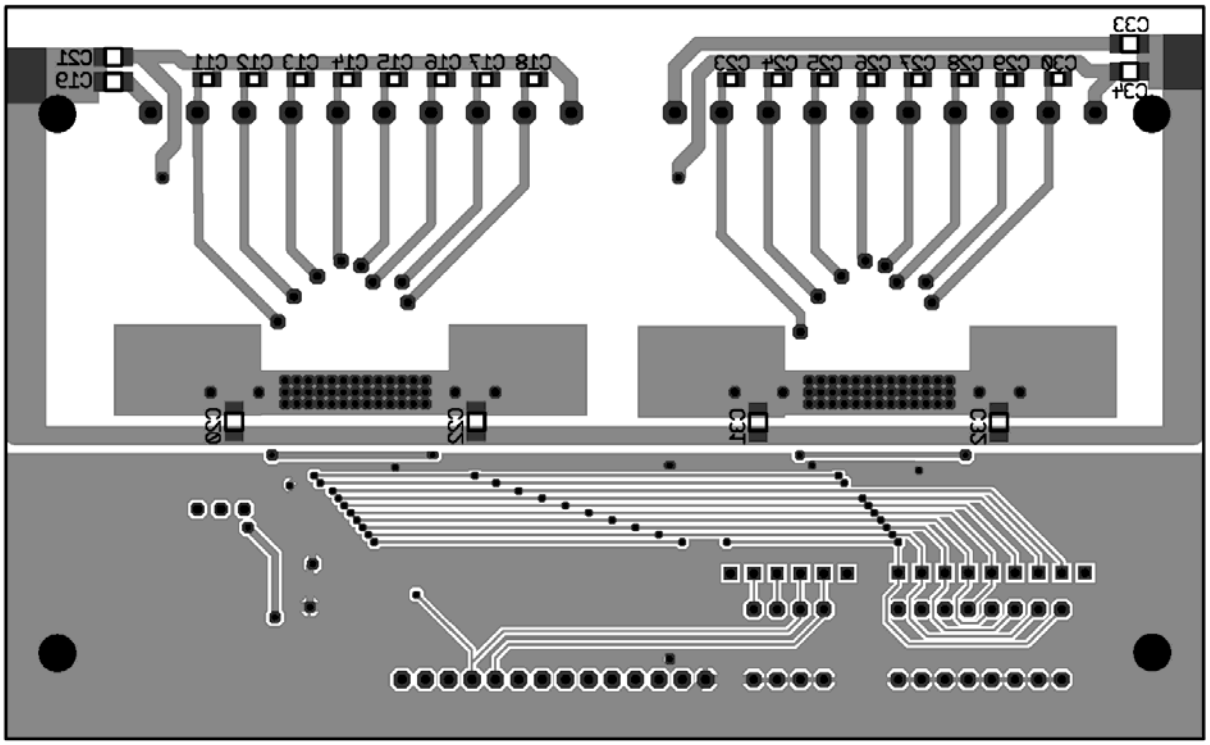




PCB Layout and Assembly



Board Layout - Component Side



Board Layout - Bottom Side (mirror view)

Bill of Material

Nr.	Quant.	Position	Value	Package
1	5	C1, C4, C6, C7, C8	100nF, 50V	0805
2	2	C36, C37	1uF, 50V	0805
3	2	C9, C10	10uF, 50V	SMD_E
4	2	C3, C35	10uF, 10V	0805
5	16	C11, C12, C13, C14, C15, C16, C17, C18, C23, C24, C25, C26, C27, C28, C29, C30	10nF, 50V	0805
6	8	C19, C20, C21, C22, C31, C32, C33, C34	4,7nF, 500V	1206
7	1	C5	10uF, 25V	SMD_B
8	16	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16	LED gn	P-LCC-2
9	2	D20, D21	LED rt	P-LCC-2
10	1	D17	LL4148	MM
11	2	D18, D19	SM15T39A	SMC
12	2	F1, F2	OMF125, 5A	SMD-D/E
13	1	IC1	TLE4264	SOT-223
14	2	IC2, IC3	ISO1H811G	P-DSO36
15	2	K1, K2	Terminal 10pol.	RM5,08
16	1	K3	Connector 14pol.	RM2,54
17	1	K4	Connector 3pol.	RM2,54
18	16	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16	10k	1206
19	2	R17, R18	4,7k	1206
20	2	R20, R25	0R	805
21	1	RN1	Winet 8x4,7k	9-SIL-1
22	1	RN2	Winet 5x4,7k	6-SIL-1
23	1	S1	DIP-Switch 4	DSS-04
24	1	S2	DIP-Switch 8	DSS-08
25	1	K4	Jumper	
26	4		Spacer	
27	1		Print Board	

References

[1] ISO1H811G Coreless Transformer Isolated Digital Output 8 Channel 0.625A High Side Switch, Data Sheet, Infineon Technologies

Change service

Revision History			
Application Note EVAL2x8-ISO1H811G-1			
Actual Release: V1.1	Date:15.02.2010		Previous Release:
Page of actual Rel.	Page of prev. Rel.	Subjects changed since last release	
11	----------	First Issue	

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