EiceDRIVER™

High voltage gate driver IC

Evaluation Board

Application Note

EVAL_1ED020I12-BT

Application Note

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Page or Item	**Subjects (major changes since last revision)**
Previous Version: 1.0	

Table of Contents

Warnings

The described board is an evaluation board dedicated for laboratory environment only. It operates at high voltages. This board must be operated by qualified, skilled personnel familiar with all applicable safety standards.

1 Introduction

The gate driver evaluation board EVAL_1ED020I12-BT was developed to show the functionalities and key features of the Infineon IGBT gate driver 1ED020I12-BT (also applied to 1ED020I12-FT).
The board is available from Infineon in sampling quantities. The properties of this part are described in the datasheet chapter of this document, whereas the remaining paragraphs provide information intended to enable the customer to copy, modify and qualify the design for production, according to their own specific requirements.
The design of the EVAL_1ED020I12-BT was performed with respect to the environmental conditions described in this document. The design was tested as described in this document, but not qualified regarding manufacturing, lifetime or over the full ambient operating conditions.
The boards provided by Infineon are subjected to functional testing only.
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2 Design feature

This chapter provides an overview of the main features, key datas, pin assignments and mechanical dimensions

2.1 Main features

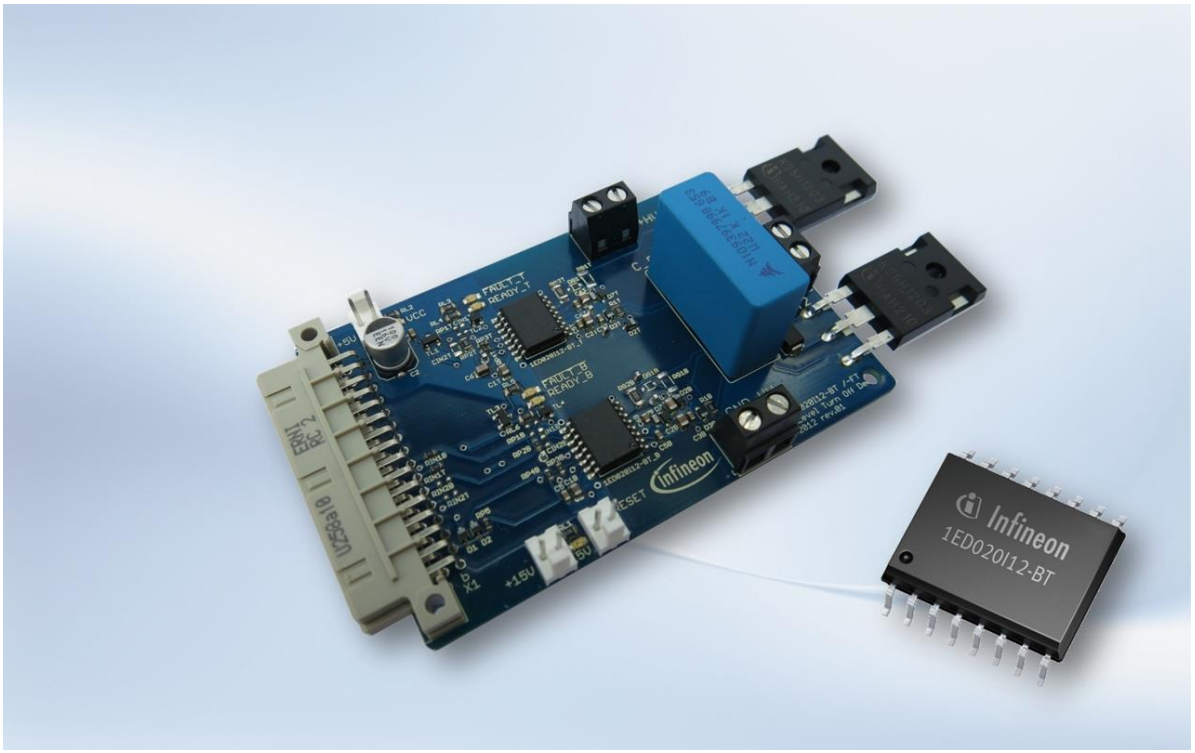


Figure 2-1 top view of the 1ED020I12-BT_EVAL

The EVAL_1ED020I12-BT contains two Infineon IGBT gate driver 1ED020I12-BT in a half bridge configuration driving two Infineon IGBT IKW25N120H3 in TO-247 package.
The evaluation board provides the following main features

- Galvanic isolation by the coreless transformer technology of the Infineon gate driver. The 1ED020I12-BT is suitable for basic isolation
- Isolation inside the half bridge by defined creepage
- Short circuit protection
- Under voltage lock out
- Active miller clamp
- Isolated DC-DC-converter for bipolar supply of the gate driver output with typ. +15V/-7V
- Connector for 5V digital supply, 15V supply, Reset, High voltage supply, external load
- Status LED for 5V supply, 15V supply, ready and fault separated for high- and lowside driver
- DC link capacitor

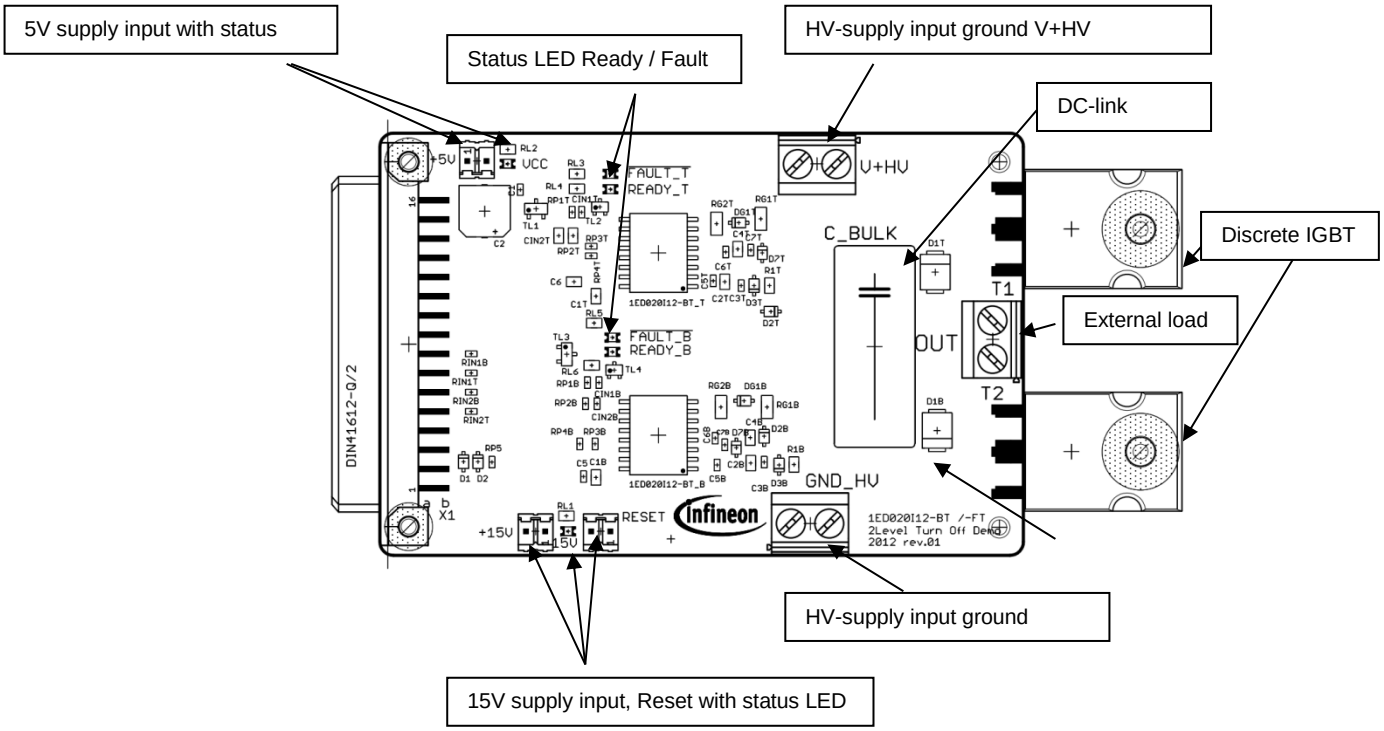


Figure 2-2 overview functionalities on top-side

2.2 Key data

All values are values at an ambient temperature of 25°C.

Table 2-1

Parameter	Description	Typ.	min	max	Unit
+15V	15V voltage supply	15	13	17.5	V
5V	5V voltage supply	5	4.5	5.5	V
HV	High voltage supply	-	-	800	V
I_{Out}	Output current	-	-	25	A
I_{Gmax}	Max. peak gate driver output current	-	-	2	A
R_{Gmin}	Min. gate resistor to limit gate driver output current	-	15	-	Ω

* Please make sure that the maximum rated values never get exceeded. Also the performance and quality can not be guaranteed when using the board with all parameters in maximum rated value at the same time.

2.3 Pin assignment

Table 2-2

Connector name	Pin no.	Pin name	Description
RESET	Right terminal	/RST	same as X1-B1
	Left terminal	GND	same as X1-A16
+5V (VCC1)	Left terminal	+5V	positive 5V logic supply
	Right terminal	GND	same as X1-A16
+15V (VCC2)	Left terminal	+15V	positive 15V supply for secondary side
	Right terminal	GND	
X1	A16	GND	reference for 5V supply and input signals
	B1	/RST	input – 0V to reset circuit
	B2	/FLT	output combined /Fault_T, /Fault_B, 0..5V
	B5	IN-T	inverting input top IGBT; internal pull up
	B6	IN-B	inverting input bottom IGBT; internal pull up
	B7	IN+T	non-inverting input top IGBT; 0V off; 5V on
	B8	IN+B	non-inverting input bottom IGBT; 0V off; 5V on
	B16	+5V	positive 5V supply
GND_HV			reference for high voltage supply (Power-GND, internally connected to GND)
V+HV			positive high voltage supply (up to 800V related to GND_HV)
OUT			Output HV half bridge (related to GND_HV)

3 Electrical features

3.1 Supply voltages +5V and +15V

The supply voltage for the digital part (+5V VCC1) and for the driver output (+15V VCC2) has to be supplied externally over the dedicated connectors. The evaluation board does not provide an over voltage supply monitoring, therefore the user has to ensure that the voltages are in the correct range. Voltages above the max values will lead to damages of the IGBT drivers. The availability of the supply voltages is visible over the green status LEDs.

The gate driver output of the 1ED020I12-BT is supplied with +15V (VCC2) and -7V (VEE2) by an isolated DC/DC-power supply which is integrated in the evaluation board. The negative supply at VEE2 prevents a parasitic turn on of the gate by switching on the opposite IGBT. The use of the negative voltage makes the clamp “Active Miller Clamp” functionality unnecessary.

3.2 Under voltage lockout

The +15V supply VCC2 is monitored by the 1ED020I12-BT. In case of an undervoltage of <13V at VCC2 the driver output is switched off. This status is visible over the yellow READY LEDs for top and bottom side. If the LED is on, the supply at VCC2 is >13V

3.3 V_{CEsat} monitoring for short circuit detection

The Infineon gate driver 1ED020I12-BT provides a short circuit detection by measuring the V_{CEsat} voltage of the IGBT. If a short circuit occurs, the collector current and the saturation voltage increase. If the IGBT is commanded on stated and the V_{CE} reaches 9V a short circuit is detected and the gate driver output is switched off. This status is reported by the /FLT signal and the dedicated FAULT LED is switched on.

Figure 3-1 shows the signals of the bottom side driver and IGBT during a shoot through.

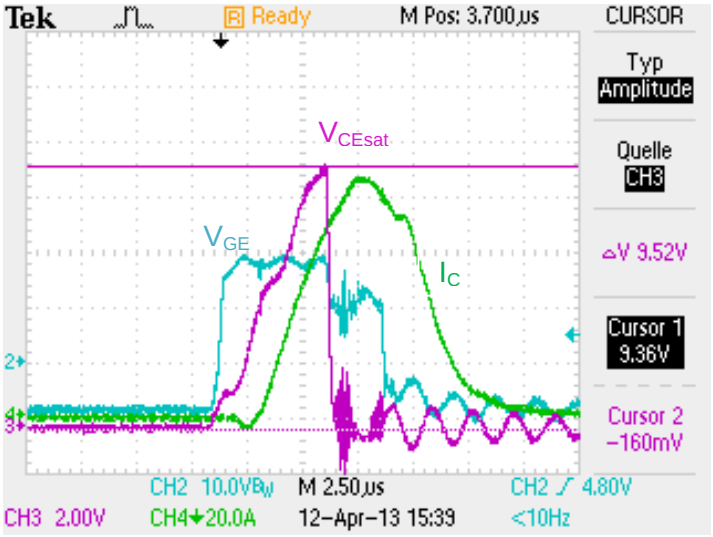


Figure 3-1 the signals of the bottom side driver and IGBT during a shoot through
(Ic curve with 1.2µs delay due to slow current probe)

The FAULT status is latched by the 1ED020I12-BT and must be resetted by switching the RESET Signal to ground.

3.4 Two level turn-off

The Two Level Turn-Off functionality introduces a second voltage level at the driver output in between ON- and OFF-level. This ensures lower V_{CE} overshoots at turn off by reducing the V_{GE} of the IGBT at short circuits or over current events.
The reference voltage level and hold up time can be adjusted at pin TLSET of the 1ED020I12-BT.
The reference voltage is set by the Zener diodes D7T and D7B. The holdup time is set by the capacitance connected between pin TLSET and Gnd2.

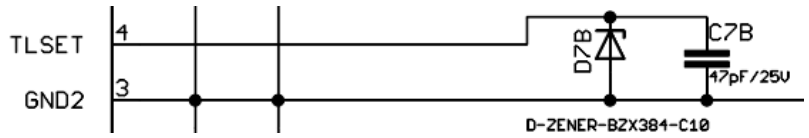


Figure 3-2 the components connected to pin TLSET of the 1ED020I12-BT bottom

In this case, the second voltage level is set to 10V by the Zener diodes and the holdup time is approximately 2.4µs with a capacitance of 47pF at pin TLEST. For more detailed information please refer to the datasheet of the 1ED020I12-BT available on the Infineon webpage.

Figure 3-3 shows the discharging and charging of the external capacitor C7B to set up the two level turn-off.

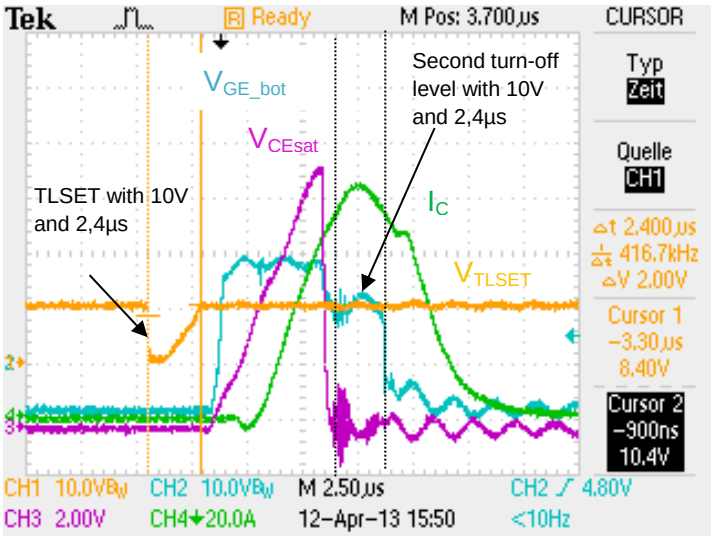


Figure 3-3 the signal at TLSET before a shoot through event

It is visible that there is second voltage level at the V_{GE_bot} during turn-off. This level has the same values like the signal at pin TLSET with 10V and ~2.4µs.

3.5 IGBT turn - on / off

The switching characteristic of the IGBTs is defined by the gate resistors RG1B, RG1T, RG2B and RG2T.

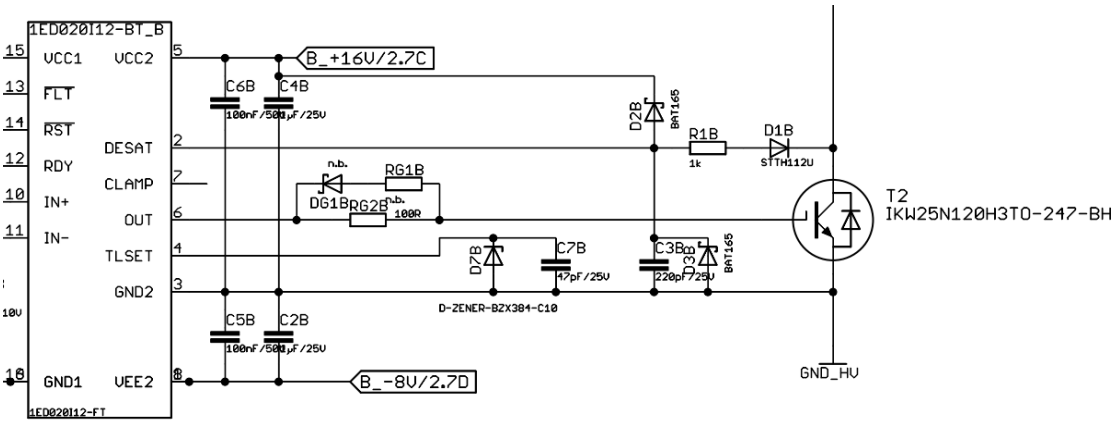
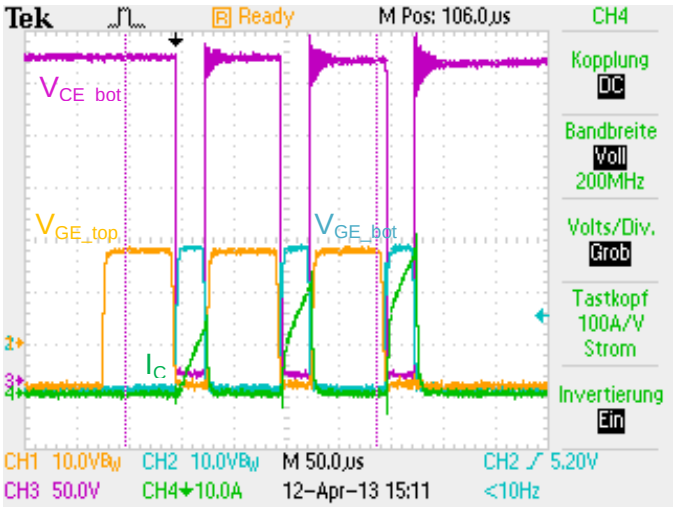


Figure 3-4 bottom side driver output

The gate resistors are adapted to the Infineon IGBT IKW25N120H3 to get signals with less oscillation as possible by keeping a fast slope at the output. There is the possibility to adapt the switching characteristic to specific applications or to different IGBTs by replacing the values of RG1B and RG1T. The use of RG2B and RG2T together with DG1B and DG1T makes it possible to change the on-switching and the off-switching slopes of the IGBT independent to each other.

To avoid a shoot through between top- and bottom IGBT, the operator needs ensure sufficient dead time. With this setup the dead time should be > 1.5µs.



Switching sequence with 3 pulses and the following parameters:

Supply Input: 300V

Duty cycle = 80% referred to the top IGBT

Figure 3-5 overview switching sequence with 3 pulses

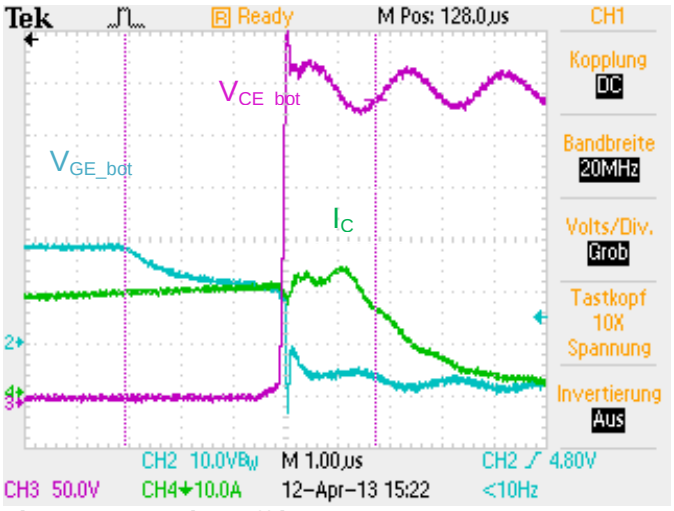


Figure 3-6 turning off bottom IGBT

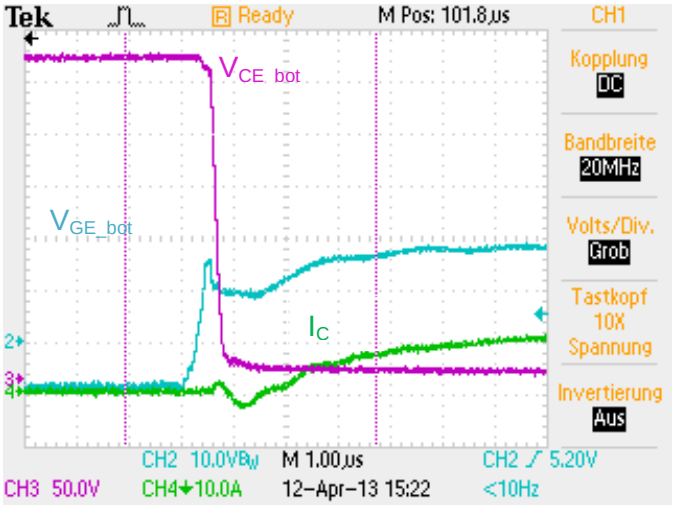


Figure 3-7 turning on bottom IGBT

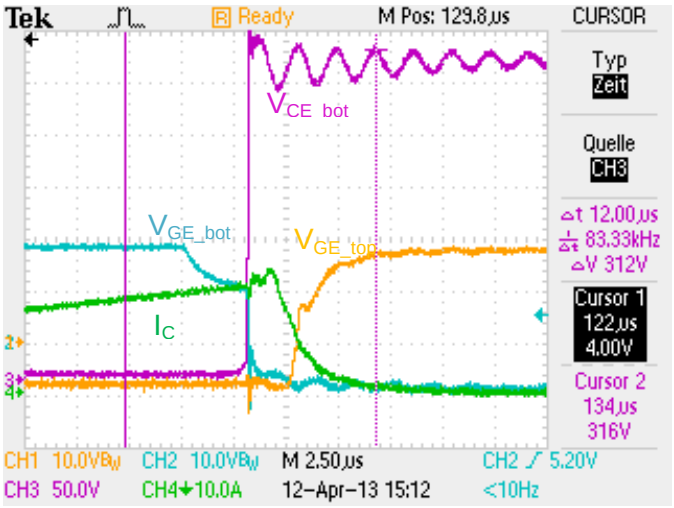


Figure 3-8 turning off bottom IGBT and turning on top IGBT with delay of 2.5µs

3.6 DC-Link capacitor

Due to the available space there is only a small DC-Link capacitor of 220nF available. If a bigger DC-Link capacity is necessary it has to be connected externally to the connectors V+HV and GND_HV.

3.7 Input PWM-Signals

The PWM input pins of the 1ED020I12-BT can be configured in non-inverting input logic or inverting input logic.

- IN+ Non Inverting Driver Input
  IN+ control signal for the driver output if IN- is set to low, e.g. the IGBT is on if IN+ = high and IN- = low
- IN- Inverting Driver Input
  IN- control signal for the driver output if IN+ is set to high, e.g. the IGBT is on if IN- = low and IN+ = high

The EVAL_1ED020I12-BT is designed in that way, that the non-inverting input is used. There is the possibility to use also the inverting input logic by replace RIN1T, RIN1B and RP1T and RP1B.

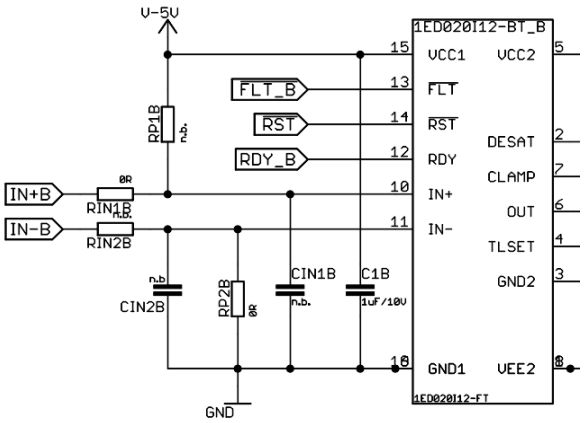


Figure 3-9 bottom side driver input

There is also the possibility to use low pass filters inside the PWM input signals to avoid a undesired switch on an IGBT by disturbances. This feature is not used in this evaluation board, but there is the possibility to test it by changing the resistors RIN1T, RIN1B, RIN2T, RIN2B and the capacitors CIN1T, CIN1B, CIN2T, CIN2B.

4 Schematic and Layout

4.1 Schematic

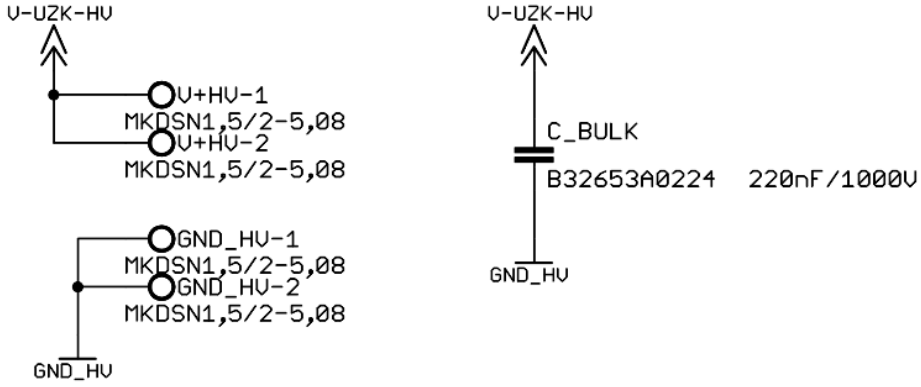


Figure 4-1 HV supply input and DC-Link

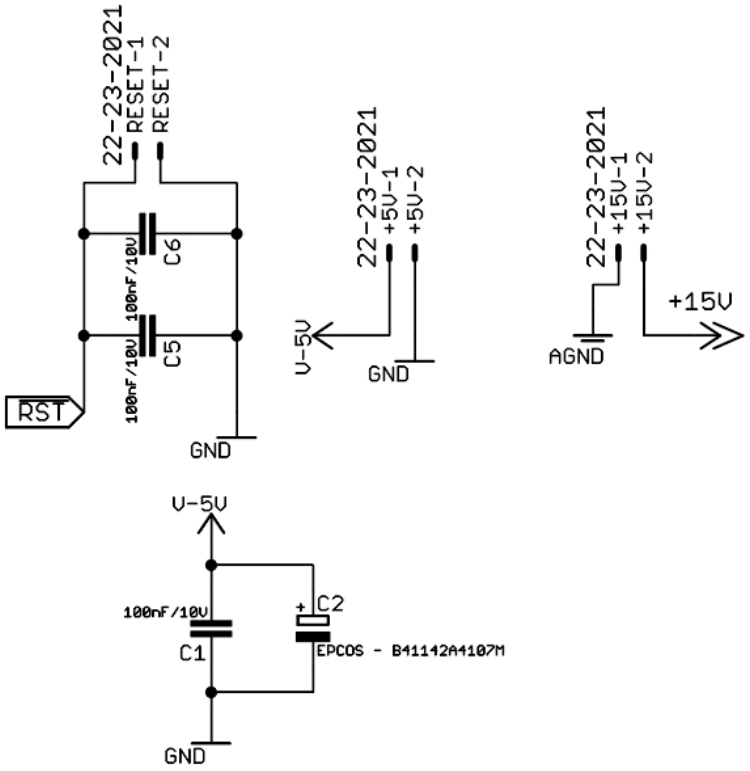


Figure 4-2 LV Supply and Reset Input

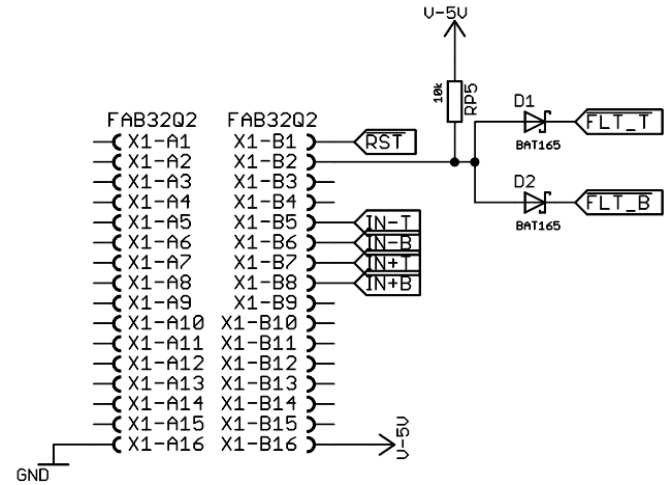


Figure 4-3 connector X1

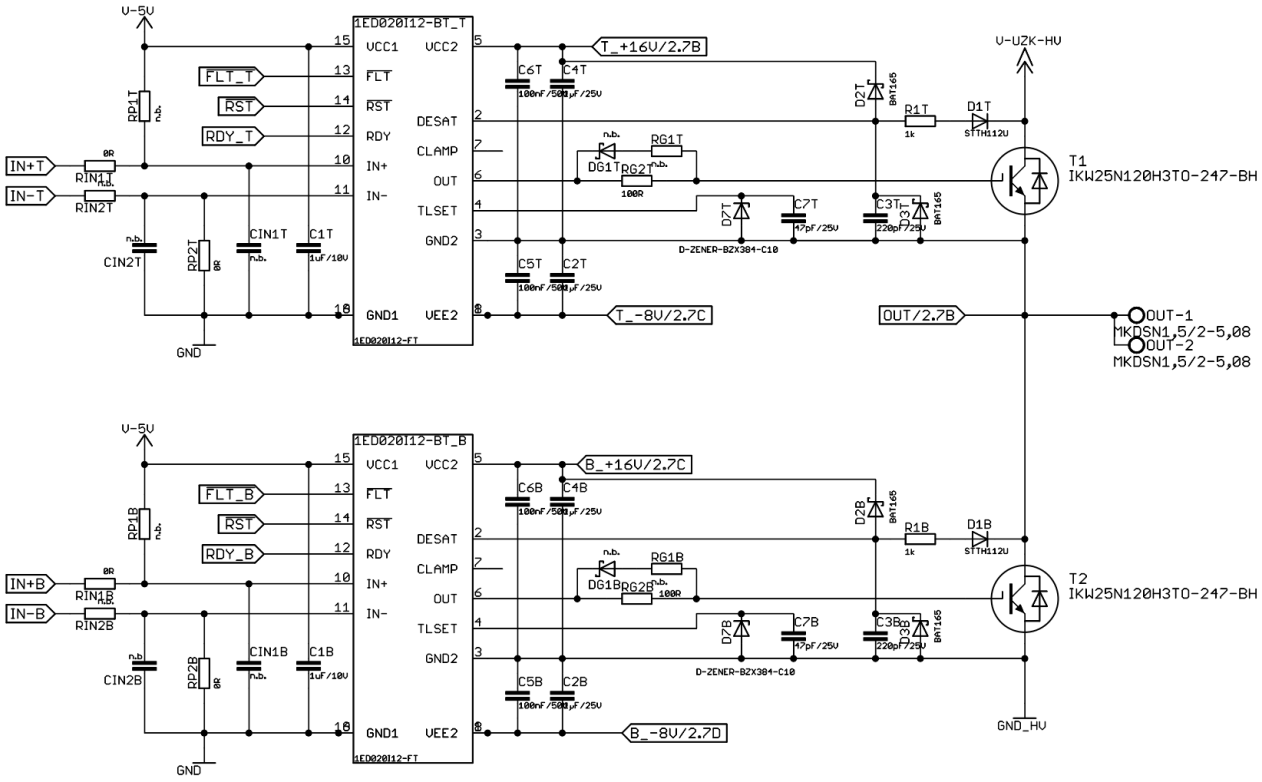


Figure 4-4 Infineon driver 1ED020I12 top and bottom

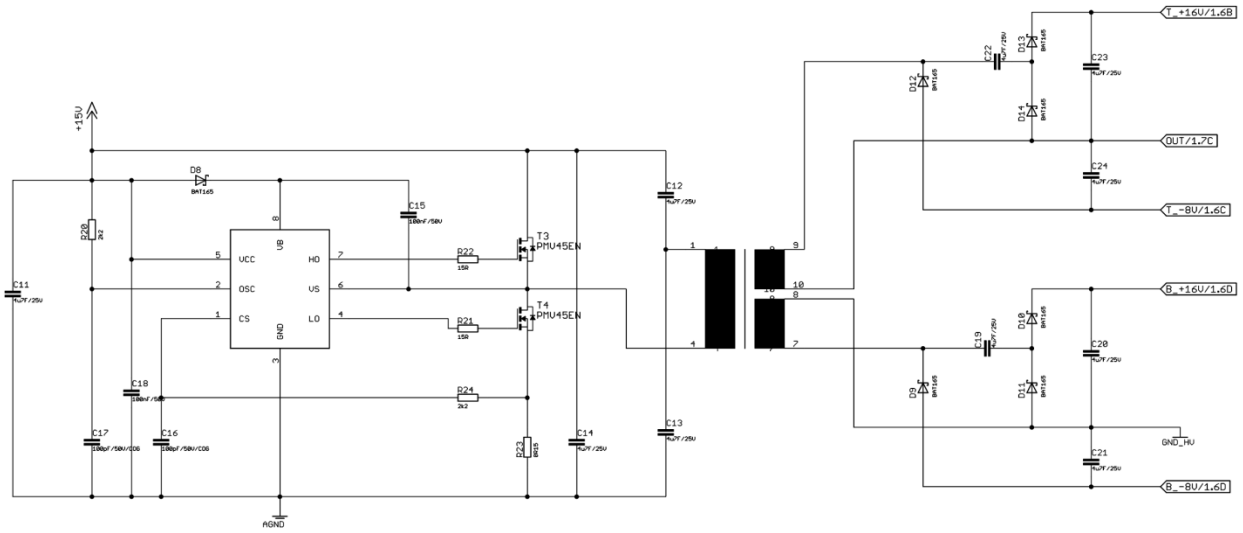


Figure 4-5 DC/DC-converter

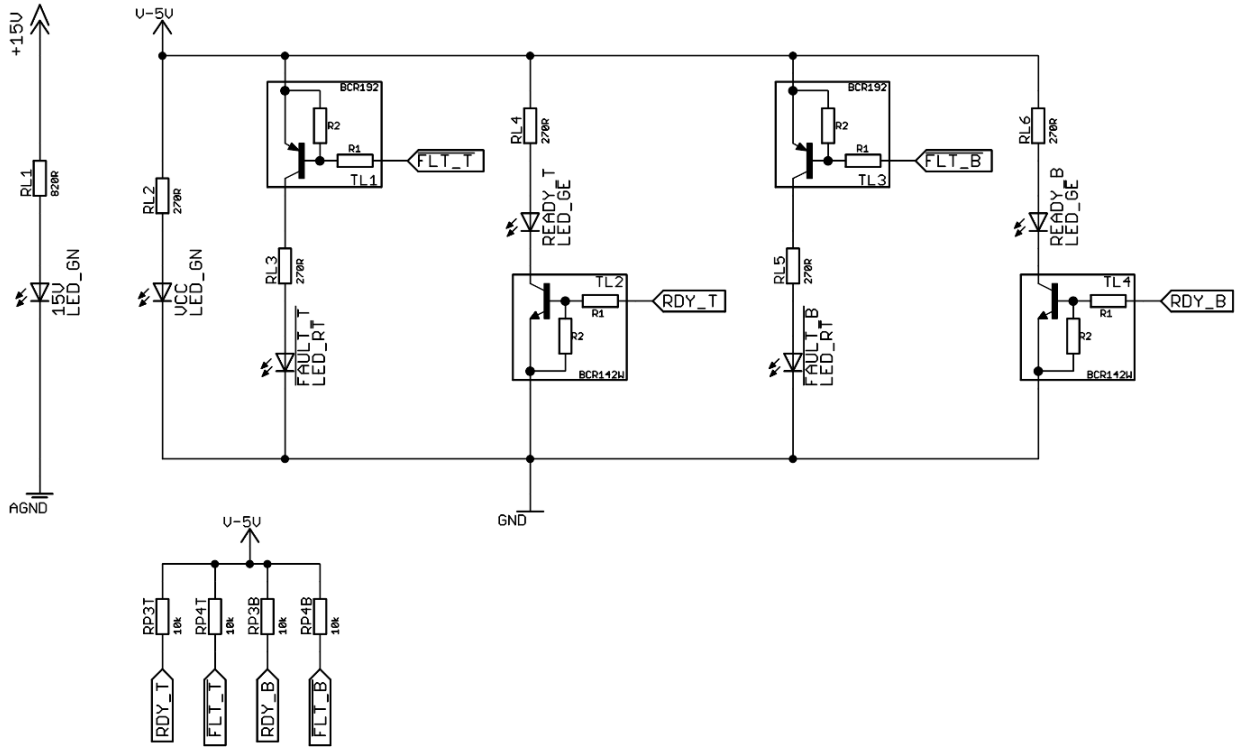


Figure 4-6 LEDs, FAULT and READY logic

4.2 Layout

4.2.1 Creepage distance

The isolation between input and output is ensured by the coreless transformer of the 1ED020I12-BT IGBT gate driver. The creepage distance ensured by the layout is 8mm between low- and high voltage supply and 2.4mm inside the high voltage supply area.

4.2.2 Layout top

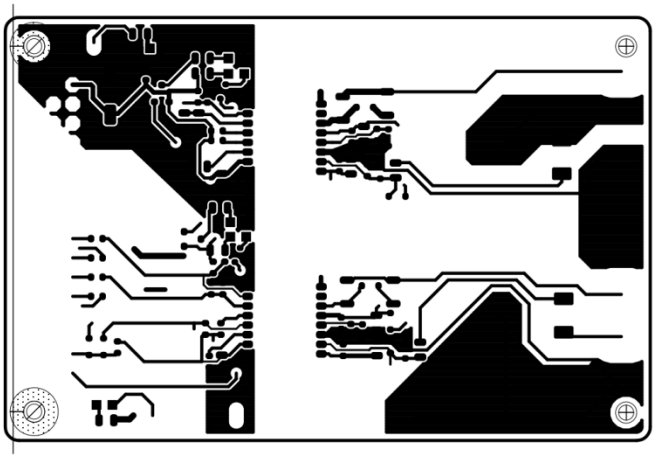


Figure 4-7 Layout top of the EVAL_1ED020I12-BT

4.2.3 Layout bottom

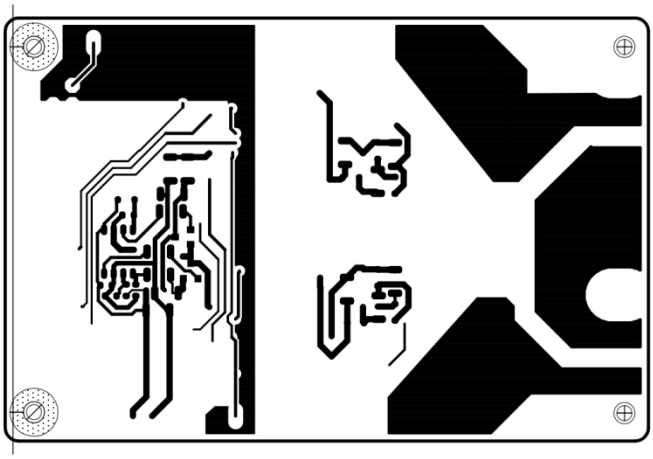


Figure 4-8 Layout bottom of the EVAL_1ED020I12-BT

4.2.4 Top place

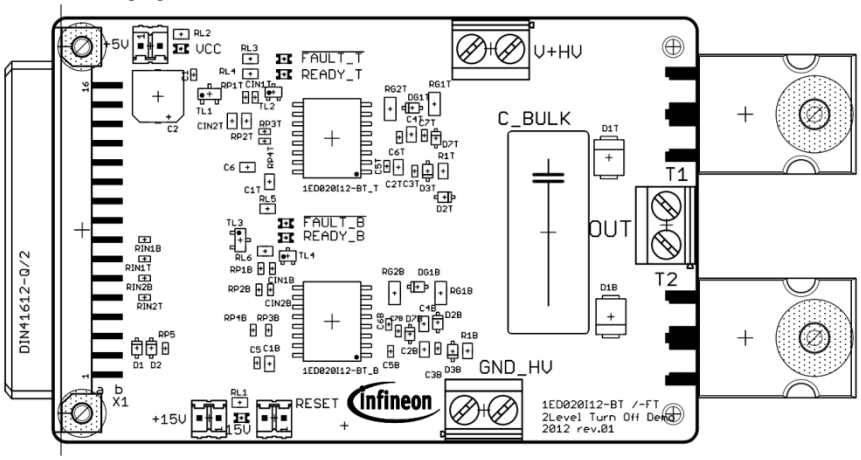


Figure 4-9 top place view of the EVAL_1ED020I12-BT

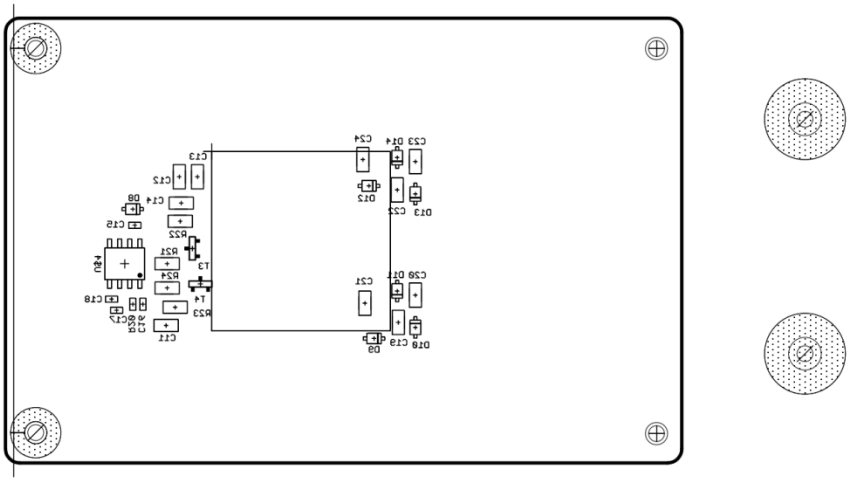


Figure 4-10 bottom place view of the EVAL_1ED020I12-BT

4.3 Bill of material

Part	Value	Package
C1, C5	100nF/10V X7R	SMD0603
C1B, C1T	1uF/10V X7R	SMD0805
C2	100µF / 16V	6.3 x 6.3 x 7.7mm
C2B, C2T, C4B, C4T	1µF/25V X7R	SMD0805
C3B, C3T	220pF/25V X7R	SMD0603
C5B, C5T, C6B, C6T, C15, C18	100nF/50V X7R	SMD0603
C6	100nF/10V X7R	SMD0805
C7B, C7T	47pF/25V X7R	SMD0603
C11, C12, C13, C14, C19, C20, C21, C22, C23, C24	4u7F/25V X7R	SMD1206
C16, C17	100pF/50V/COG	SMD0603
C_BULK	220nF/1000V	C22.5B10
D1, D2, D2B, D2T, D3B, D3T, D8, D9, D10, D11, D12, D13, D14	BAT165	SOD323F
D1B, D1T	STTH112U	SMB_DO-214AA
D7B, D7T	D-ZENER-BZX384-C10	SOD323
R1B, R1T	1k	SMD0805
R20	2k2	SMD0603
R21, R22	15R	SMD1206
R23	0R15	SMD1206
R24	2k2	SMD1206
RG2B, RG2T	100R	SMD1206
RIN1B, RIN1T, RP2B	0R	SMD0603
RL1	820R	SMD0805
RL2, RL3, RL4, RL5, RL6	270R	SMD0805
RP2T	0R	SMD0805
RP3B, RP3T, RP4B, RP4T, RP5	10k	SMD0603
T1, T2	IKW25N120H3	TO247BH
T3, T4	PMV45EN	SOT-23
TL1, TL3	BCR192	SOT23
TL2, TL4	BCR142W	SOT323
TR1	Trafo 1:1.2	T60403-D4615-X054
U$4	IR2085S	SO-8
1ED020I12-BT_B, 1ED020I12-BT_T	1ED020I12-BT	PG-DSO-16-15
X1	FAB32Q2	FAB32Q2
+5V, +15V, RESET	22-23-2021	22-23-2021
GND_HV, OUT, V+HV	MKDSN1,5/2-5,08	MKDSN1,5/2-5,08
!FAULT_B, !FAULT_T	LED_RT	CHIPLED_0805
15V, VCC	LED_GN	CHIPLED_0805
READY_B, READY_T	LED_GE	CHIPLED_0805

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