LITIX™ Basic

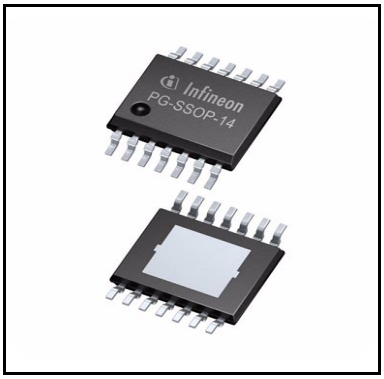
TLD1120EL

1 Channel High-Side Current Source

AEC Qualified

RoHS

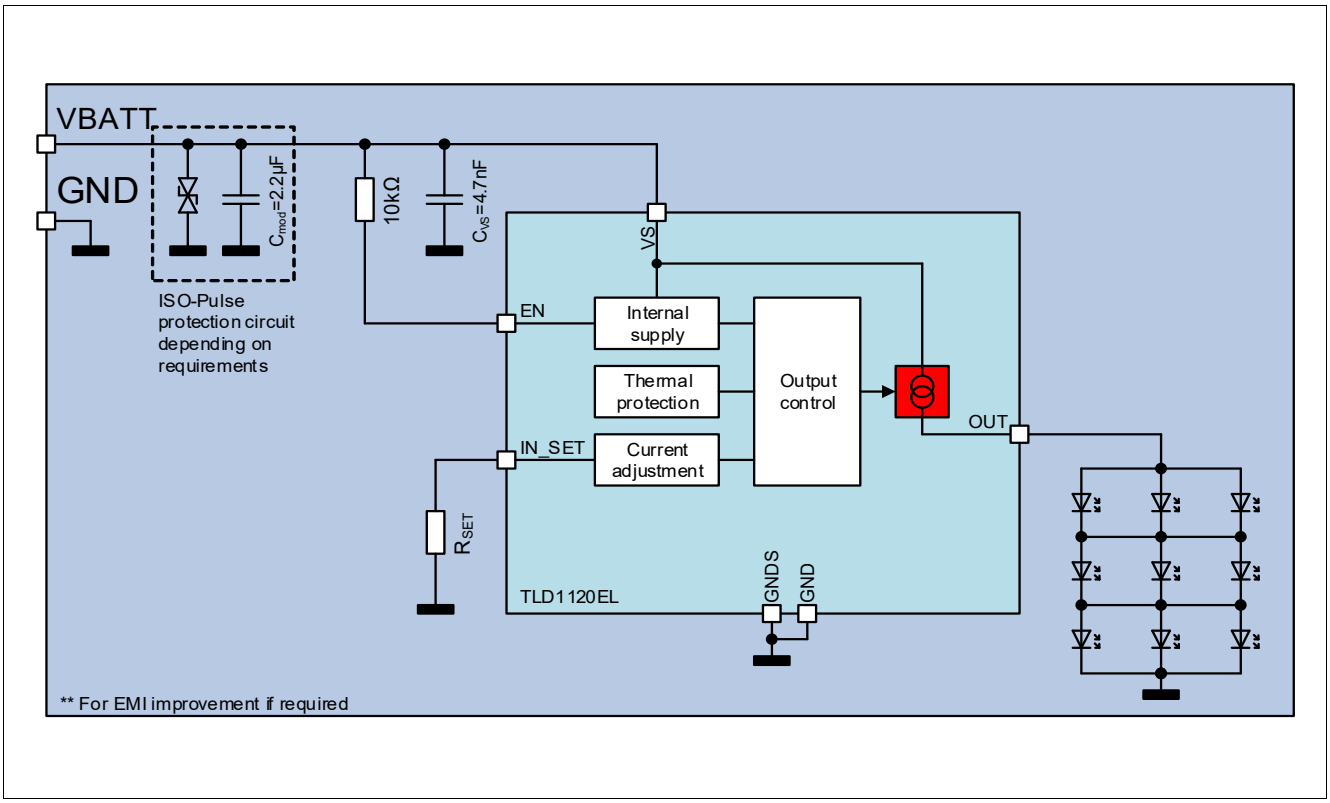
Package	PG-SSOP-14
Marking	TLD1120



1 Overview

Applications

- Exterior LED lighting applications such as tail/brake light, turn indicator, position light, side marker,...
- Interior LED lighting applications such as ambient lighting, interior illumination and dash board lighting.



Application Diagram with TLD1120EL

Overview

Basic Features

- 1 Channel device with integrated output stage (current source), optimized to drive LEDs with output current up to 360 mA
- Low current consumption in sleep mode
- PWM-operation supported via VS- and EN-pin
- Output current adjustable via external low power resistor and possibility to connect PTC resistor for LED protection during over temperature conditions
- Reverse polarity protection and overload protection
- Undervoltage detection
- Wide temperature range: -40°C < T_j < 150°C
- PG-SSOP-14 package with exposed heatslug

Description

The LITIX™ Basic TLD1120EL is a one channel high side driver IC with integrated output stage. It is designed to control LEDs with a current up to 360 mA. In typical automotive applications the device is capable to drive i.e. 3 red LEDs with a current up to 180 mA, which is limited by thermal cooling aspects. The output current is controlled practically independent of load and supply voltage changes.

Table 1 Product Summary

Parameter	Symbol	Value
Operating voltage range	$V_{S(nom)}$	5.5 V ... 40 V
Maximum voltage	$V_{S(max)}$ $V_{OUT(max)}$	40 V
Nominal output (load) current	$I_{OUT(nom)}$	180 mA when using a supply voltage range of 8 V - 18 V (e.g. Automotive car battery). Currents up to $I_{OUT(max)}$ possible in applications with low thermal resistance R_{thJA}
Maximum output (load) current	$I_{OUT(max)}$	360 mA; depending on thermal resistance R_{thJA}
Output current accuracy at R_{SET} = 12 kΩ	k_{LT}	2250 ± 7%
Current consumption in sleep mode	$I_{S(sleep,typ)}$	0.1 µA

Protective Functions

- ESD protection
- Under voltage lock out
- Over Load protection
- Over Temperature protection
- Reverse Polarity protection

2 Block Diagram

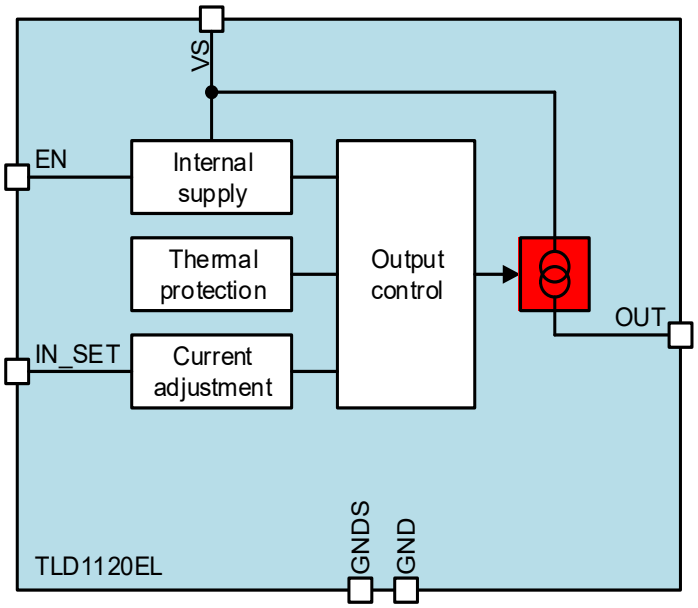


Figure 1 Basic Block Diagram

3 Pin Configuration

3.1 Pin Assignment

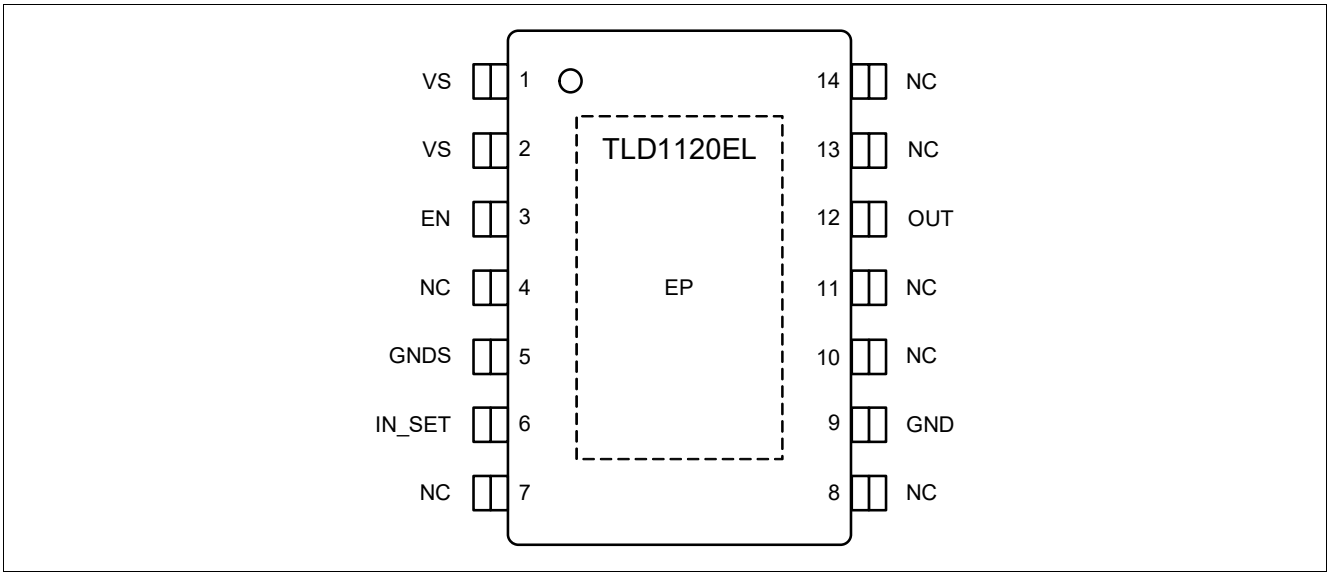


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Input/ Output	Function
1, 2	VS	–	**Supply Voltage;** battery supply, connect a decoupling capacitor (100 nF - 1 µF) to GND
3	EN	I	**Enable pin**
4	NC	–	**Pin not connected**
5	GNDS	–	[1] **GNDS;** Signal GND, connect to GND
6	IN_SET	I/O	**Input / SET pin;** Connect a low power resistor to adjust the output current
7	NC	–	**Pin not connected**
8	NC	–	**Pin not connected**
9	GND	–	[1] **Ground**
10	NC	–	**Pin not connected**
11	NC	–	**Pin not connected**
12	OUT	O	**Output**
13	NC	–	**Pin not connected**
14	NC	–	**Pin not connected**
Exposed Pad	GND	–	[1] **Exposed Pad;** connect to GND in application

1) Connect all GND-pins together.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	V_S	-16	40	V	–
4.1.2	Input voltage EN	V_{EN}	-16	40	V	–
4.1.3	Input voltage EN related to V_S	$V_{EN(VS)}$	V_S - 40	V_S + 16	V	–
4.1.4	Input voltage EN related to V_{OUT} V_{EN} - V_{OUT}	V_{EN} - V_{OUT}	-16	40	V	–
4.1.5	Output voltage	V_{OUT}	-1	40	V	–
4.1.6	Power stage voltage $V_{PS} = V_S - V_{OUT}$	V_{PS}	-16	40	V	–
4.1.7	IN_SET voltage	V_{IN_SET}	-0.3	6	V	–
Currents						
4.1.8	IN_SET current	I_{IN_SET}	–	2	mA	–
4.1.9	Output current	I_{OUT}	–	390	mA	–
Temperatures						
4.1.10	Junction temperature	T_j	-40	150	°C	–
4.1.11	Storage temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.12	ESD resistivity to GND	V_{ESD}	-2	2	kV	Human Body Model (100 pF via 1.5 kΩ)[2)]
4.1.13	ESD resistivity all pins to GND	V_{ESD}	-500	500	V	CDM[3)]
4.1.14	ESD resistivity corner pins to GND	V_{ESD}	-750	750	V	CDM[3)]

1) Not subject to production test, specified by design
2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001-2011
3) ESD susceptibility, Charged Device Model “CDM” according to JESD22-C101E

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.15	Supply voltage range for normal operation	$V_{S(nom)}$	5.5	40	V	–
4.2.16	Power on reset threshold	$V_{S(POR)}$	–	5	V	$V_{EN} = V_S$ R_{SET} = 12 kΩ I_{OUT} = 80% $I_{OUT(nom)}$ V_{OUT} = 2.5 V
4.2.17	Junction temperature	T_j	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case	R_{thJC}	–	8	10	K/W	1) 2)
4.3.2	Junction to Ambient 1s0p board	R_{thJA1}				K/W	1) 3)
			–	61	–		T_a = 85 °C
			–	56	–		T_a = 135 °C
4.3.3	Junction to Ambient 2s2p board	R_{thJA2}				K/W	1) 4)
			–	45	–		T_a = 85 °C
			–	43	–		T_a = 135 °C

1) Not subject to production test, specified by design. Based on simulation results.

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed Pad are fixed to ambient temperature). T_a = 85°C, Total power dissipation 1.5 W.

3) The R_{thJA} values are according to Jedec JESD51-3 at natural convection on 1s0p FR4 board. The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 70 µm Cu, 300 mm^2 cooling area. Total power dissipation 1.5 W distributed statically and homogenously over power stage.

4) The R_{thJA} values are according to Jedec JESD51-5,-7 at natural convection on 2s2p FR4 board. The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 2 inner copper layers (outside 2 x 70 µm Cu, inner 2 x 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer. Total power dissipation 1.5 W distributed statically and homogenously over power stage.

5 EN Pin

The EN pin is a dual function pin:

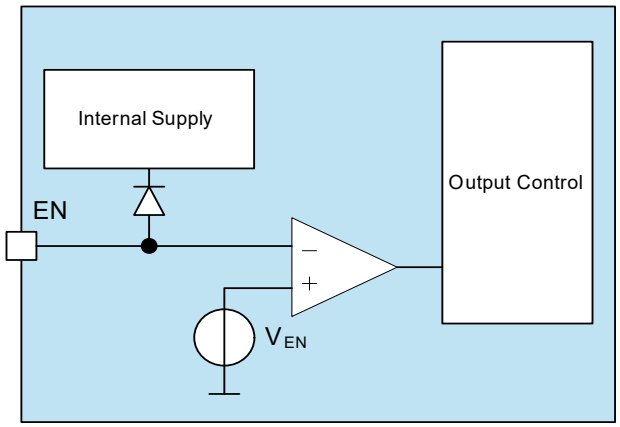


Figure 3 Block Diagram EN pin

Note: The current consumption at the EN-pin I_{EN} needs to be added to the total device current consumption. The total current consumption is the sum of the currents at the VS-pin I_S and the EN-pin I_{EN}.

5.1 EN Function

If the voltage at the pin EN is below a threshold of $V_{EN(off)}$ the LITIX™ Basic IC will enter Sleep mode. In this state all internal functions are switched off, the current consumption is reduced to $I_{S(sleep)}$. A voltage above $V_{EN(on)}$ at this pin enables the device after the Power on reset time t_{POR}.

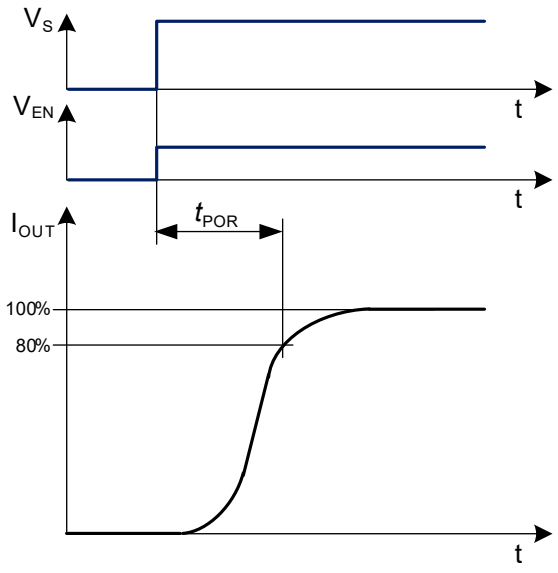


Figure 4 Power on reset

5.2 Internal Supply Pin

The EN pin can be used to supply the internal logic. There are two typical application conditions, where this feature can be used:

1) In “DC/DC control Buck” configurations, where the voltage V_S can be below 5.5V.

2) In configurations, where a PWM signal is applied at the Vbatt pin of a light module. The buffer capacitor C_{BUF} is used to supply the LITIX™ Basic IC during Vbatt low (V_S low) periods. This feature can be used to minimize the turn-on time to the values specified in **Pos. 7.2.11**. Otherwise, the power-on reset delay time t_{POR} (**Pos. 5.4.4**) has to be considered.

The capacitor can be calculated using the following formula:

$$C_{BUF} = t_{LOW(max)} \cdot \frac{I_{EN(LS)}}{V_S - V_{D1} - V_{S(POR)}} \quad (1)$$

See also a typical application drawing in **Chapter 8**.

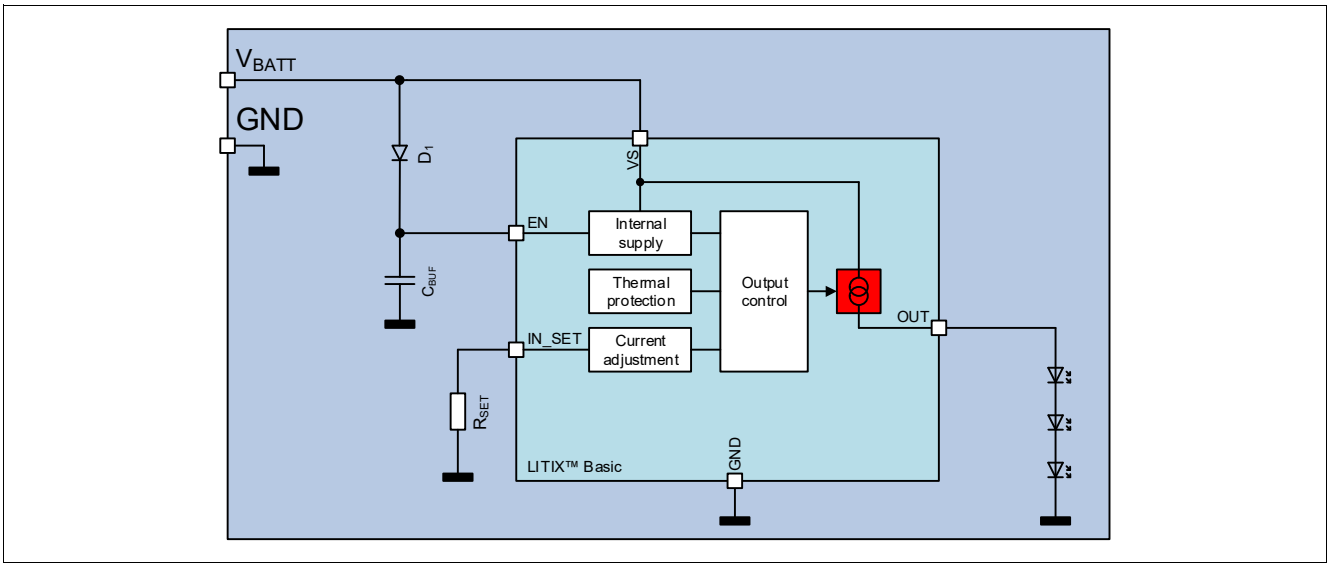


Figure 5 External circuit when applying a fast PWM signal on V_{BATT}

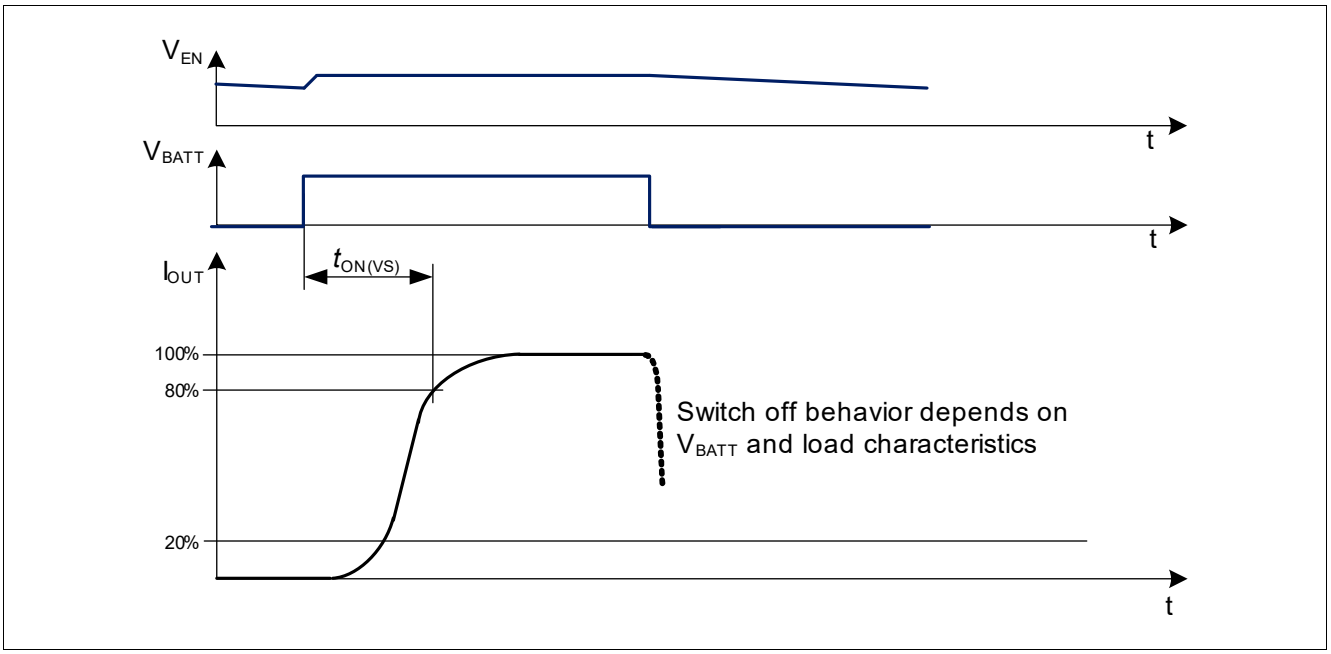


Figure 6 Typical waveforms when applying a fast PWM signal on V_{BATT}

The parameter $t_{ON(VS)}$ is defined at **Pos. 7.2.11**. The parameter $t_{OFF(VS)}$ depends on the load and supply voltage V_{BATT} characteristics.

5.3 EN Unused

In case of an unused EN pin, there are two different ways to connect it:

5.3.1 EN - Pull Up to VS

The EN pin can be connected with a pull up resistor (e.g. 10 kΩ) to V_s potential. In this configuration the LITIX™ Basic IC is always enabled.

5.3.2 EN - Direct Connection to VS

The EN pin can be connected directly to the VS pin (IC always enabled). This configuration has the advantage (compared to the configuration described in **Chapter 5.3.1**) that no additional external component is required.

5.4 Electrical Characteristics Internal Supply / EN Pin

Electrical Characteristics Internal Supply / EN pin

Unless otherwise specified, V_S = 5.5 V to 40 V, T_j = -40°C to +150°C, R_{SET} = 12 kΩ all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.1	Current consumption, sleep mode	$I_{S(sleep)}$	–	0.1	2	µA	[1] V_{EN} = 0.5 V T_j < 85 °C V_S = 18 V V_{OUT} = 3.6 V
5.4.2	Current consumption, active mode	$I_{S(on)}$				mA	[2] I_{IN_SET} = 0 µA T_j < 105 °C V_S = 18 V V_{OUT} = 3.6V
			–	–	1.4		V_{EN} = 5.5 V
			–	–	0.75		V_{EN} = 18 V
			–	–	1.5		[1] R_{EN} = 10 kΩ between VS and EN-pin
5.4.3	Current consumption, device disabled via IN_SET	$I_{S(dis,IN\_SET)}$				mA	[2] V_S = 18 V T_j < 105 °C V_{IN_SET} = 5 V
			–	–	1.4		V_{EN} = 5.5 V
			–	–	0.7		V_{EN} = 18 V
			–	–	1.4		[1] R_{EN} = 10 kΩ between VS and EN-pin
5.4.4	Power-on reset delay time [3]	t_{POR}	–	–	25	µs	[1] V_S = V_{EN} = 0 →13.5 V $V_{OUT(nom)}$ = 3.6 ± 0.3V I_{OUT} = 80% $I_{OUT(nom)}$
5.4.5	Required supply voltage for output activation	$V_{S(on)}$	–	–	4	V	V_{EN} = 5.5 V V_{OUT} = 3 V I_{OUT} = 50% $I_{OUT(nom)}$
5.4.6	Required supply voltage for current control	$V_{S(CC)}$	–	–	5.2	V	V_{EN} = 5.5 V V_{OUT} = 3.6 V I_{OUT} ≥ 90% $I_{OUT(nom)}$
5.4.7	EN turn on threshold	$V_{EN(on)}$	–	–	2.5	V	–
5.4.8	EN turn off threshold	$V_{EN(off)}$	0.8	–	–	V	–

EN Pin

Electrical Characteristics Internal Supply / EN pin (cont'd)

Unless otherwise specified, V_S = 5.5 V to 40 V, T_j = -40°C to +150°C, R_{SET} = 12 kΩ all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.9	EN input current during low supply voltage	$I_{EN(LS)}$	–	–	1.8	mA	[1] V_S = 4.5 V T_j < 105 °C V_{EN} = 5.5 V
5.4.10	EN high input current	$I_{EN(H)}$				mA	T_j < 105 °C
			–	–	0.1		V_S = 13.5 V, V_{EN} = 5.5 V
			–	–	0.1		V_S = 18 V, V_{EN} = 5.5 V
			–	–	1.65		V_S = V_{EN} = 18 V
			–	–	0.45		[1] V_S = 18 V, R_{EN} = 10 kΩ between VS and EN-pin

1) Not subject to production test, specified by design
2) The total device current consumption is the sum of the currents I_S and $I_{EN(H)}$, please refer to **Pos. 5.4.10**
3) See also **Figure 4**

6 IN_SET Pin

The IN_SET pin is a multiple function pin for output current definition and input:

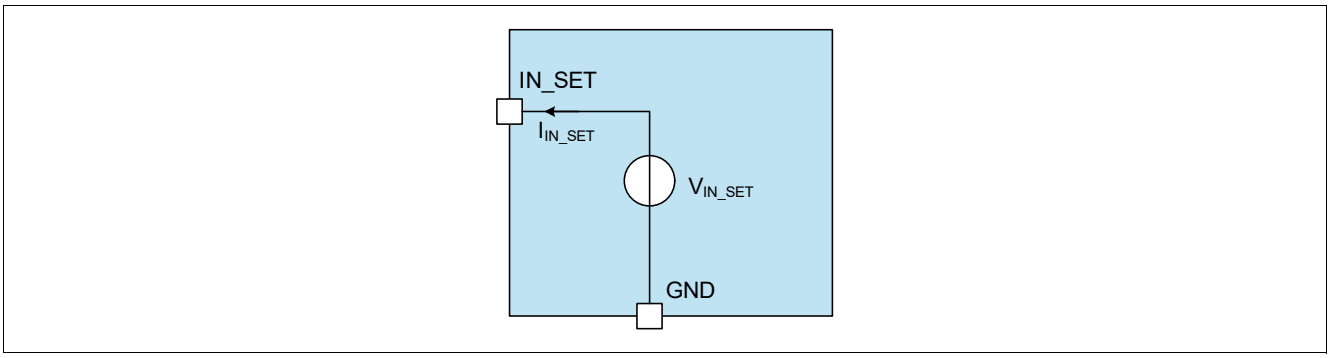


Figure 7 Block Diagram IN_SET pin

6.1 Output Current Adjustment via RSET

The current adjustment can be done by placing a low power resistor (R_{SET}) at the IN_SET pin to ground. The dimensioning of the resistor can be done using the formula below:

$$R_{SET} = \frac{k}{I_{OUT}} \quad (2)$$

The gain factor k (R_{SET} * output current) is specified in **Pos. 7.2.4** and **Pos. 7.2.5**. The current through the R_{SET} is defined by the resistor itself and the reference voltage $V_{IN\_SET(ref)}$, which is applied to the IN_SET during supplied device.

6.2 Input Pin

The IN_SET pin can be connected via R_{SET} to the open-drain output of a µC or to an external NMOS transistor as described in **Figure 8**. This signal can be used to turn off the output stage of the IC. A minimum IN_SET current of $I_{IN\_SET(act)}$ is required to turn on the output stage. This feature is implemented to prevent glimming of LEDs caused by leakage currents on the IN_SET pin, see **Figure 10** for details.

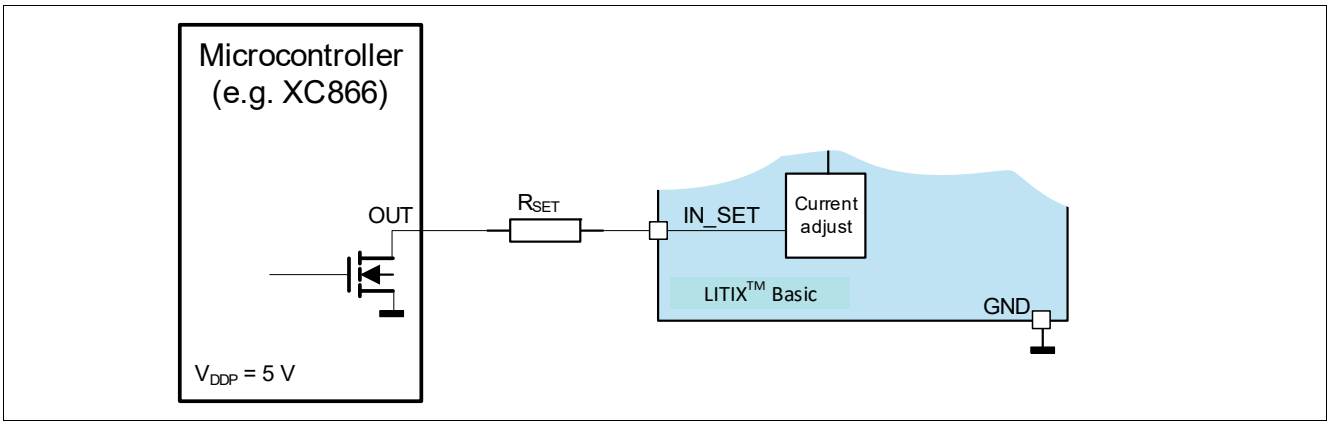


Figure 8 Schematics IN_SET interface to µC

The resulting switching times are shown in **Figure 9**:

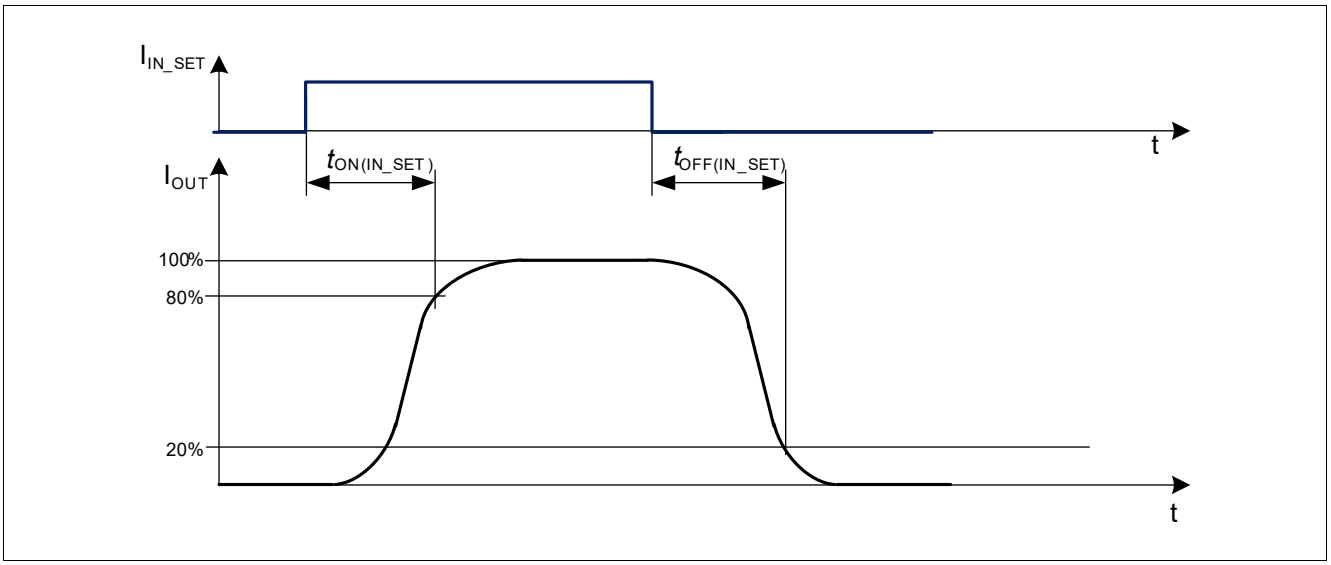


Figure 9 Switching times via IN_SET

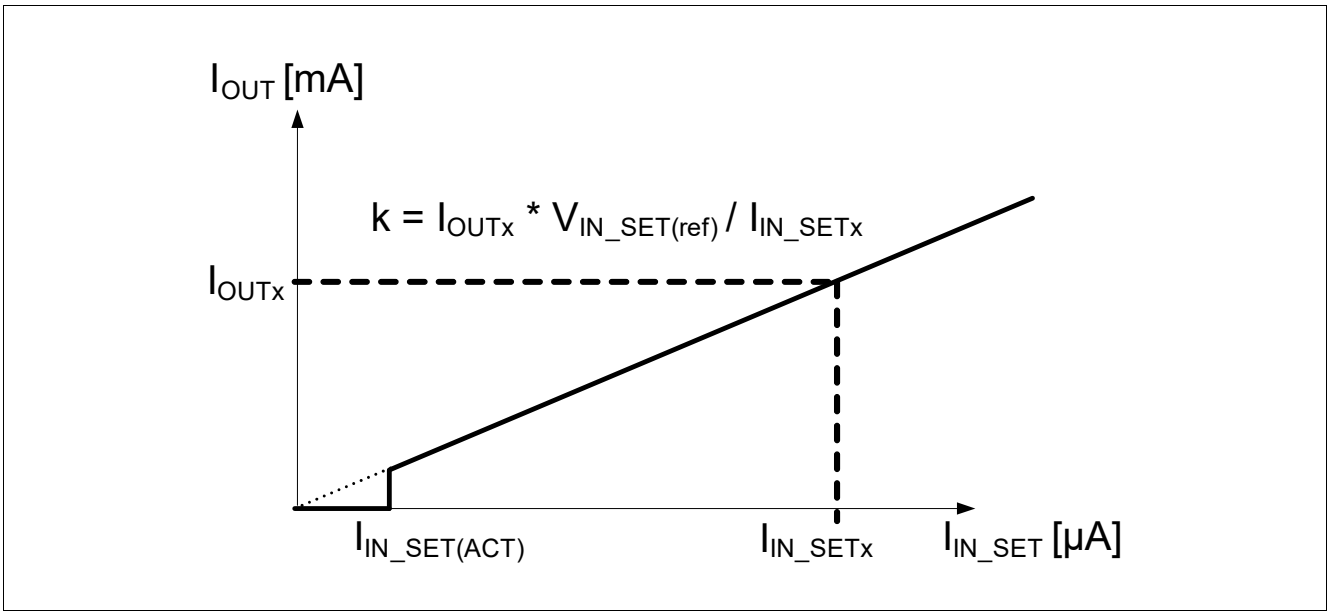


Figure 10 I_{OUT} versus I_{INSET}

6.3 Electrical Characteristics IN_SET Pin

Electrical Characteristics IN_SET pin

Unless otherwise specified, V_S = 5.5 V to 40 V, T_j = -40°C to +150°C, R_{SET} = 12 kΩ, all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.1	IN_SET reference voltage	$V_{IN\_SET(ref)}$	1.19	1.23	1.27	V	1) V_{OUT} = 3.6 V T_j = 25...115 °C
6.3.2	IN_SET activation current without turn on of output stage	$I_{IN\_SET(act)}$	2	–	15	µA	See **Figure 10**

1) Not subject to production test, specified by design

7 Power Stage

The output stage is realized as high side current source with a current of 360 mA. During off state the leakage current at the output stage is minimized in order to prevent a slightly glowing LED.

The maximum current of the channel is limited by the power dissipation and used PCB cooling areas (which results in the applications R_{thJA}).

For an operating current control loop the supply and output voltages according to the following parameters have to be considered:

- Required supply voltage for current control $V_{S(CC)}$, **Pos. 5.4.6**
- Voltage drop over output stage during current control $V_{PS(CC)}$, **Pos. 7.2.6**
- Required output voltage for current control $V_{OUT(CC)}$, **Pos. 7.2.7**

7.1 Protection

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

7.1.1 Over Load Behavior

An over load detection circuit is integrated in the LITIX™ Basic IC. It is realized by a temperature monitoring of the output stage (OUT).

As soon as the junction temperature exceeds the current reduction temperature threshold $T_{j(CRT)}$ the output current will be reduced by the device by reducing the IN_SET reference voltage $V_{IN\_SET(ref)}$. This feature avoids LED’s flickering during static output overload conditions. Furthermore, it protects LEDs against over temperature, which are mounted thermally close to the device. If the device temperature still increases, the output current decreases close to 0 A. As soon as the device cools down the output current rises again.

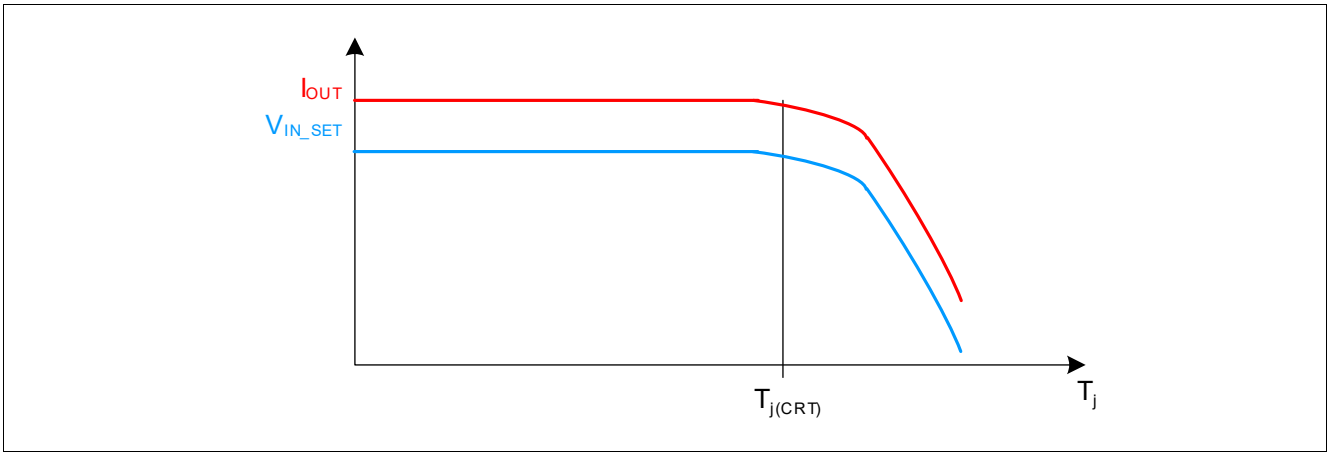


Figure 11 Output current reduction at high temperature

*Note: This high temperature output current reduction is realized by reducing the IN_SET reference voltage voltage (**Pos. 6.3.1**). In case of very high power loss applied to the device and very high junction temperature the output current may drop down to I_{OUT} = 0 mA, after a slight cooling down the current increases again.*

7.1.2 Reverse Battery Protection

The TLD1120EL has an integrated reverse battery protection feature. This feature protects the driver IC itself, but also connected LEDs. The output reverse current is limited to $I_{OUTx(rev)}$ by the reverse battery protection.

Note: Due to the reverse battery protection a reverse protection diode for the light module may be obsolete. In case of high ISO-pulse requirements and only minor protecting components like capacitors a reverse protection diode may be reasonable. The external protection circuit needs to be verified in the application.

7.2 Electrical Characteristics Power Stage

Electrical Characteristics Power Stage

Unless otherwise specified: V_S = 5.5 V to 18 V, T_j = -40°C to +150°C, V_{OUT} = 3.6 V, all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
7.2.1	Output leakage current	$I_{OUT(leak)}$	 – –	 – –	 21 9	µA	V_{EN} = 5.5 V I_{IN_SET} = 0 µA V_{OUT} = 2.5 V T_j = 150 °C 1) T_j = 85 °C
7.2.2	Output leakage current in boost over battery setup	$-I_{OUT(leak,B2B)}$	–	–	150	µA	1) V_{EN} = 5.5 V I_{IN_SET} = 0 µA V_{OUT} = V_S = 40 V
7.2.3	Reverse output current	$-I_{OUT(rev)}$	–	–	3	µA	1) V_S = -16 V Output load: LED with break down voltage < -0.6 V
7.2.4	Output current accuracy limited temperature range	k_{LT}	 2092 1935	 2250 2250	 2408 2565		1) T_j = 25...115 °C V_S = 8...18 V V_{PS} = 2 V R_{SET} = 6...12 kΩ R_{SET} = 30 kΩ
7.2.5	Output current accuracy over temperature	k_{ALL}	 2092 1935	 2250 2250	 2408 2565		1) T_j = -40...115 °C V_S = 8...18 V V_{PS} = 2 V R_{SET} = 6...12 kΩ R_{SET} = 30 kΩ
7.2.6	Voltage drop over power stage during current control $V_{PS(CC)} = V_S - V_{OUT}$	$V_{PS(CC)}$	0.75	–	–	V	1) V_S = 13.5 V R_{SET} = 12 kΩ I_{OUT} ≥ 90% of ($k_{LT(typ)}/R_{SET}$)
7.2.7	Required output voltage for current control	$V_{OUT(CC)}$	2.3	–	–	V	1) V_S = 13.5 V R_{SET} = 12 kΩ I_{OUT} ≥ 90% of ($k_{LT(typ)}/R_{SET}$)

Electrical Characteristics Power Stage (cont'd)

Unless otherwise specified: V_S = 5.5 V to 18 V, T_j = -40°C to +150°C, V_{OUT} = 3.6 V, all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
7.2.8	Maximum output current	$I_{OUT(max)}$	360	–	–	mA	R_{SET} = 4.7 kΩ The maximum output current is limited by the thermal conditions. Please refer to **Pos. 4.3.1** - **Pos. 4.3.3**
7.2.9	IN_SET turn on time	$t_{ON(IN\_SET)}$	–	–	15	µs	V_S = 13.5 V I_{IN_SET} = 0 → 100 µA I_{OUT} = 80% of $(k_{LT(typ)}/R_{SET})$
7.2.10	IN_SET turn off time	$t_{OFF(IN\_SET)}$	–	–	10	µs	V_S = 13.5 V I_{IN_SET} = 100 → 0 µA I_{OUT} = 20% of $(k_{LT(typ)}/R_{SET})$
7.2.11	VS turn on time	$t_{ON(VS)}$	–	–	20	µs	1) 2) V_{EN} = 5.5 V R_{SET} = 12 kΩ V_S = 0 → 13.5 V I_{OUT} = 80% of $(k_{LT(typ)}/R_{SET})$
7.2.12	Current reduction temperature threshold	$T_{j(CRT)}$	–	140	–	°C	1) I_{OUT} = 95% of $(k_{LT(typ)}/R_{SET})$
7.2.13	Output current during current reduction at high temperature	$I_{OUT(CRT)}$	85% of $(k_{LT(typ)}/R_{SET})$	–	–	A	1) R_{SET} = 12 kΩ T_j = 150 °C

1) Not subject to production test, specified by design

2) see also **Figure 6**

8 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

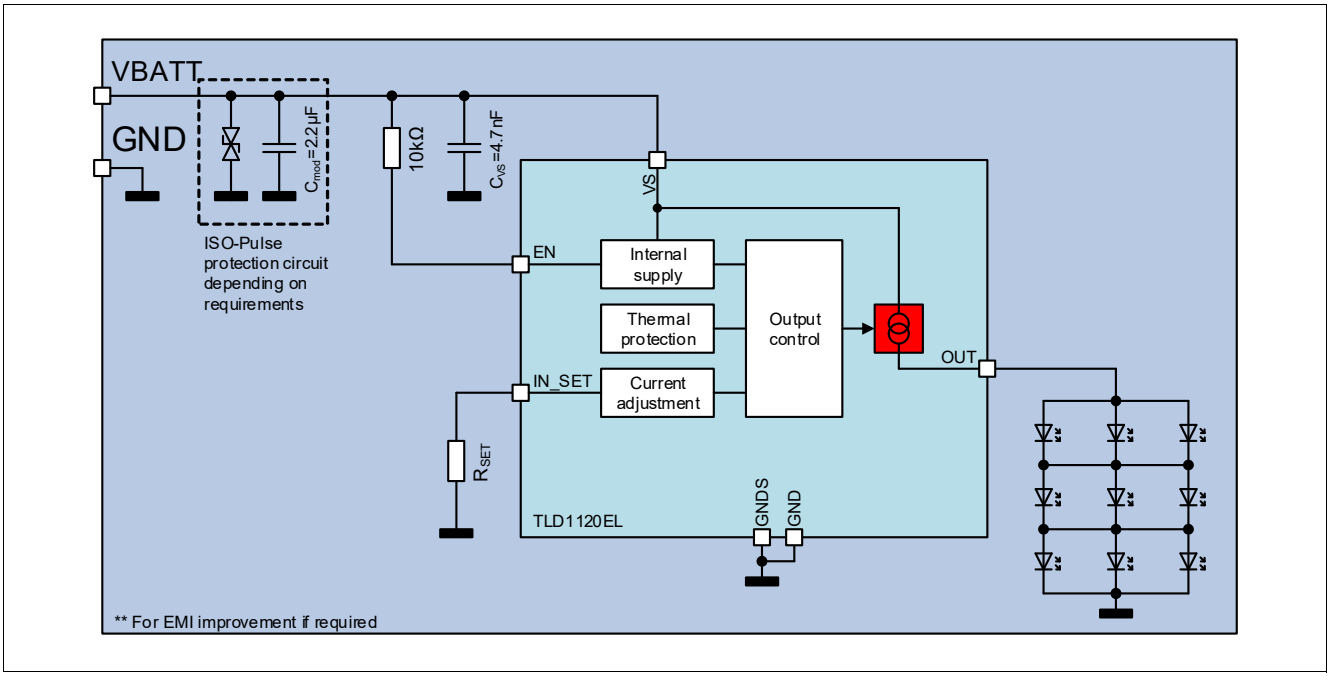


Figure 12 Application Diagram

Note: This is a very simplified example of an application circuit. In case of high ISO-pulse requirements a reverse protection diode may be used for LED protection. The function must be verified in the real application.

8.1 Further Application Information

- For further information you may contact **http://www.infineon.com/**

9 Package Outlines

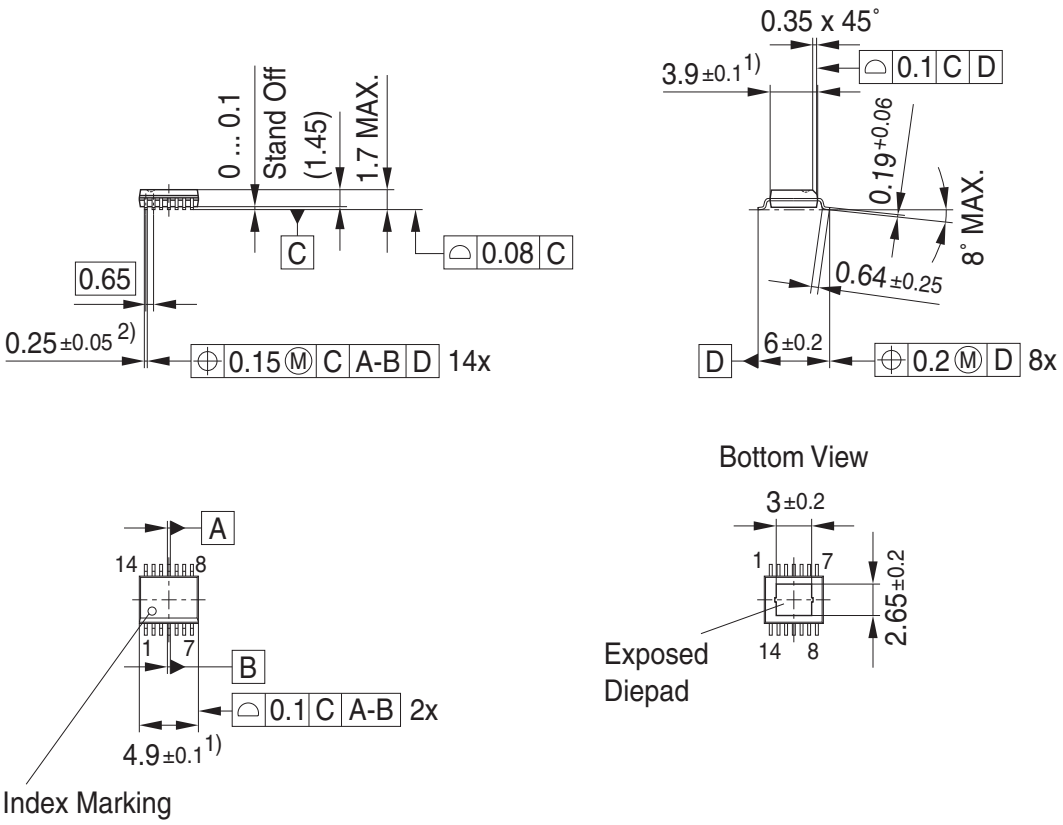


Figure 13 PG-SSOP-14

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

10 Revision History

Revision	Date	Changes
1.0	2013-08-08	Inital revision of data sheet
1.1	2015-03-19	Updated parameters K_{LT} and K_{ALL} in the chapter Power Stage
1.2	2018-04-26	Updated to latest template
1.2	2018-04-26	Updated application drawing
1.2	2018-04-26	Updated package marking
1.2	2018-04-26	Updated package figure
1.21	2021-07-05	Corrected Application diagrams in **Chapter 1** and **Chapter 8**

Table of Contents

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