

# LITIX™ Basic

**TLD2314EL**

**3 Channel High-Side Current Source**

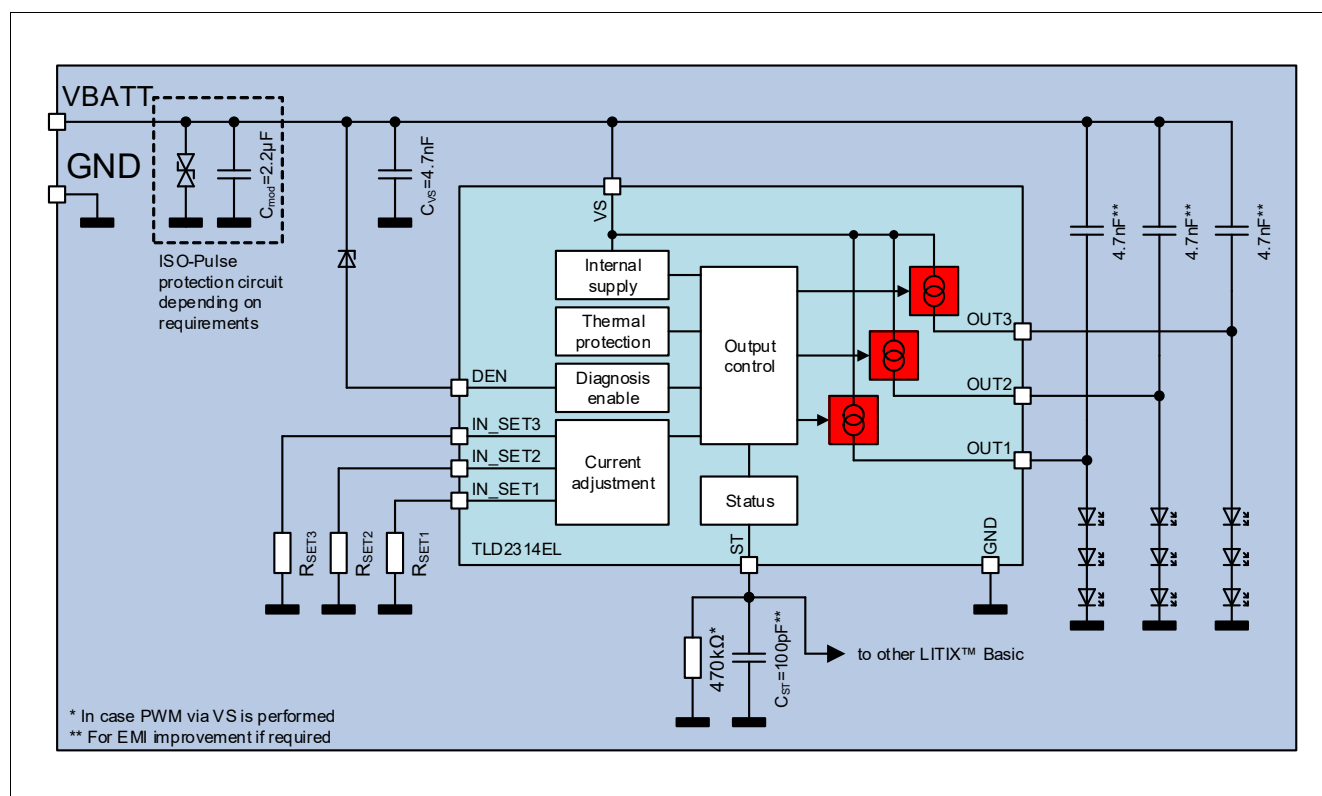
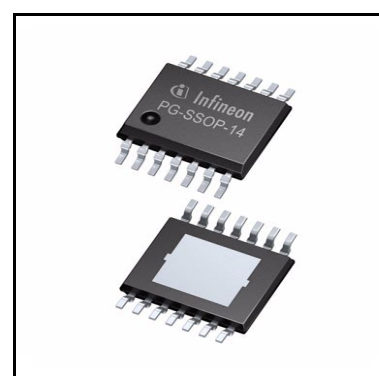


<b>Package</b>	PG-SSOP-14
<b>Marking</b>	TLD2314

## 1 Overview

### Applications

- Exterior LED lighting applications such as tail/brake light, turn indicator, position light, side marker,...
- Interior LED lighting applications such as ambient lighting (e.g. RGB), interior illumination and dash board lighting.



**Application Diagram with TLD2314EL**

## Overview

### Basic Features

- 3 Channel device with integrated output stages (current sources), optimized to drive LEDs with output current up to 120 mA per channel
- Low current consumption
- PWM-operation supported via VS-pin
- Output current adjustable via external low power resistor and possibility to connect PTC resistor for LED protection during over temperature conditions
- Reverse polarity protection and overload protection
- Undervoltage detection
- Open load and short circuit to GND diagnosis
- Wide temperature range:  $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$
- PG-SSOP-14 package with exposed heatslug

### Description

The LITIX™ Basic TLD2314EL is a three channel high side driver IC with integrated output stages. It is designed to control LEDs with a current up to 120 mA. In typical automotive applications the device is capable to drive i.e. 3 red LEDs per chain (total 9 LEDs) with a current up to 60 mA, which is limited by thermal cooling aspects. The output current is controlled practically independent of load and supply voltage changes.

**Table 1 Product Summary**

Parameter	Symbol	Value
Operating voltage range	$V_{S(nom)}$	5.5 V ... 40 V
Maximum voltage	$V_{S(max)}$ $V_{OUTx(max)}$	40 V
Nominal output (load) current	$I_{OUTx(nom)}$	60 mA when using a supply voltage range of 8 V - 18 V (e.g. Automotive car battery). Currents up to $I_{OUT(max)}$ possible in applications with low thermal resistance $R_{thJA}$
Maximum output (load) current	$I_{OUTx(max)}$	120 mA; depending on thermal resistance $R_{thJA}$
Output current accuracy at $R_{SETx} = 12 \text{ k}\Omega$	$k_{LT}$	$750 \pm 7\%$

### Protective Functions

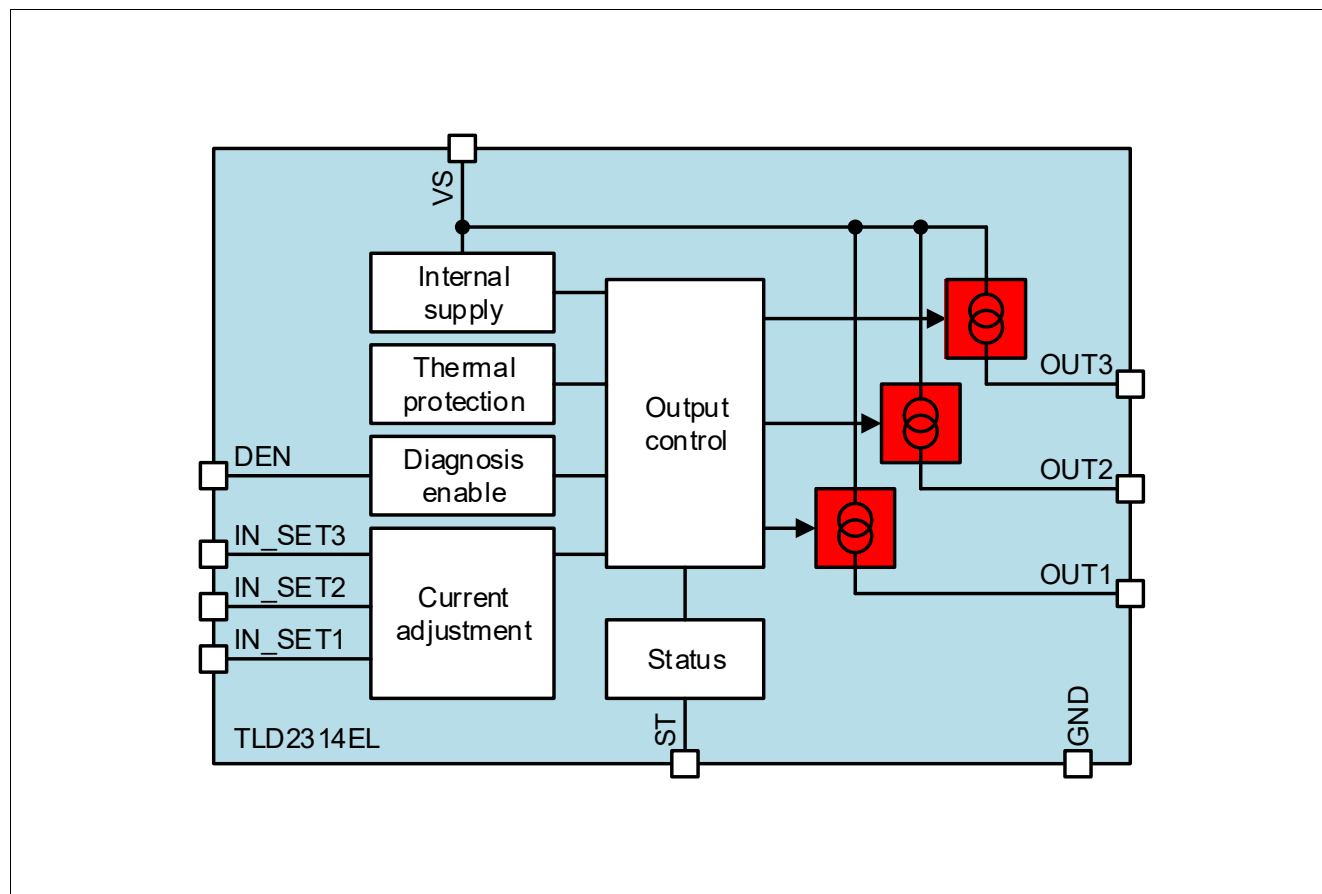
- ESD protection
- Under voltage lock out
- Over Load protection
- Over Temperature protection
- Reverse Polarity protection

### Diagnostic Functions

- Diagnosis enable function
- OL detection
- SC to Vs (indicated by OL diagnosis)
- SC to GND detection

## Block Diagram

### 2 Block Diagram



**Figure 1 Basic Block Diagram**

### 3 Pin Configuration

#### 3.1 Pin Assignment

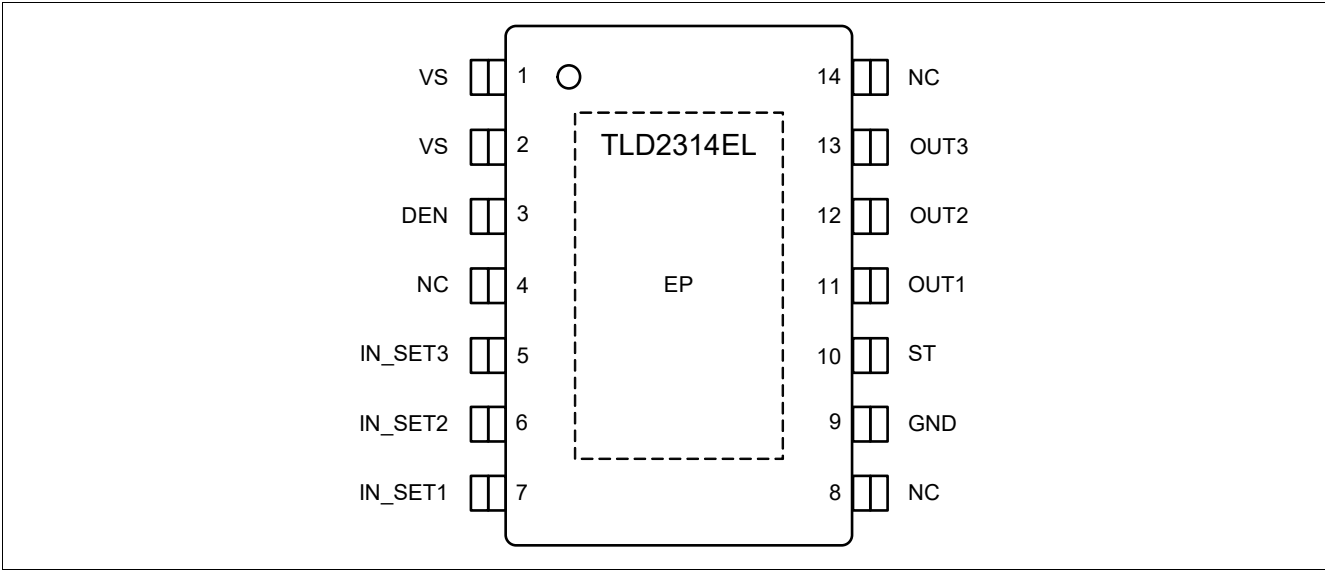


Figure 2 Pin Configuration

## Pin Configuration

### 3.2 Pin Definitions and Functions

Pin	Symbol	Input/ Output	Function
1, 2	VS	–	<b>Supply Voltage;</b> battery supply, connect a decoupling capacitor (100 nF - 1 µF) to GND
3	DEN	I	<b>Diagnosis enable pin</b>
4	NC	–	<b>Pin not connected</b>
5	IN_SET3	I/O	<b>Input / SET pin 3;</b> Connect a low power resistor to adjust the output current
6	IN_SET2	I/O	<b>Input / SET pin 2;</b> Connect a low power resistor to adjust the output current
7	IN_SET1	I/O	<b>Input / SET pin 1;</b> Connect a low power resistor to adjust the output current
8	NC	–	<b>Pin not connected</b>
9	GND	–	<sup>1)</sup> <b>Ground</b>
10	ST	I/O	<b>Status pin</b>
11	OUT1	O	<b>Output 1</b>
12	OUT2	O	<b>Output 2</b>
13	OUT3	O	<b>Output 3</b>
14	NC	–	<b>Pin not connected</b>
Exposed Pad	GND	–	<sup>1)</sup> <b>Exposed Pad;</b> connect to GND in application

1) Connect all GND-pins together.

## General Product Characteristics

### 4 General Product Characteristics

#### 4.1 Absolute Maximum Ratings

##### Absolute Maximum Ratings <sup>1)</sup>

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	$V_S$	-16	40	V	–
4.1.2	Diagnosis enable voltage DEN	$V_{\text{DEN}}$	-16	40	V	–
4.1.3	Diagn. enable voltage DEN related to $V_S$	$V_{\text{DEN}(V_S)}$	$V_S - 40$	$V_S + 16$	V	–
4.1.4	Diagn. enable voltage DEN related to $V_{\text{OUTx}}$ $V_{\text{DEN}} - V_{\text{OUTx}}$	$V_{\text{DEN}} - V_{\text{OUTx}}$	-16	40	V	–
4.1.5	Output voltage	$V_{\text{OUTx}}$	-1	40	V	–
4.1.6	Power stage voltage $V_{\text{PS}} = V_S - V_{\text{OUTx}}$	$V_{\text{PS}}$	-16	40	V	–
4.1.7	IN_SETx voltage	$V_{\text{IN\_SETx}}$	-0.3	6	V	–
4.1.8	Status voltage	$V_{\text{ST}}$	-0.3	6	V	–
Currents						
4.1.9	IN_SETx current	$I_{\text{IN\_SETx}}$	– –	2 3	mA	– Diagnosis output
4.1.10	Output current	$I_{\text{OUTx}}$	–	130	mA	–
Temperatures						
4.1.11	Junction temperature	$T_j$	-40	150	°C	–
4.1.12	Storage temperature	$T_{\text{stg}}$	-55	150	°C	–
ESD Susceptibility						
4.1.13	ESD resistivity to GND	$V_{\text{ESD}}$	-2	2	kV	Human Body Model (100 pF via 1.5 kΩ) <sup>2)</sup>
4.1.14	ESD resistivity all pins to GND	$V_{\text{ESD}}$	-500	500	V	CDM <sup>3)</sup>
4.1.15	ESD resistivity corner pins to GND	$V_{\text{ESD}}$	-750	750	V	CDM <sup>3)</sup>

1) Not subject to production test, specified by design

2) ESD susceptibility, Human Body Model "HBM" according to ANSI/ESDA/JEDEC JS-001-2011

3) ESD susceptibility, Charged Device Model "CDM" according to JESD22-C101E

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## General Product Characteristics

### 4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.16	Supply voltage range for normal operation	$V_{S(nom)}$	5.5	40	V	–
4.2.17	Power on reset threshold	$V_{S(POR)}$	–	5	V	$R_{SETx} = 12 \text{ k}\Omega$ $I_{OUTx} = 80\% I_{OUTx(nom)}$ $V_{OUTx} = 2.5 \text{ V}$
4.2.18	Junction temperature	$T_j$	–40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

### 4.3 Thermal Resistance

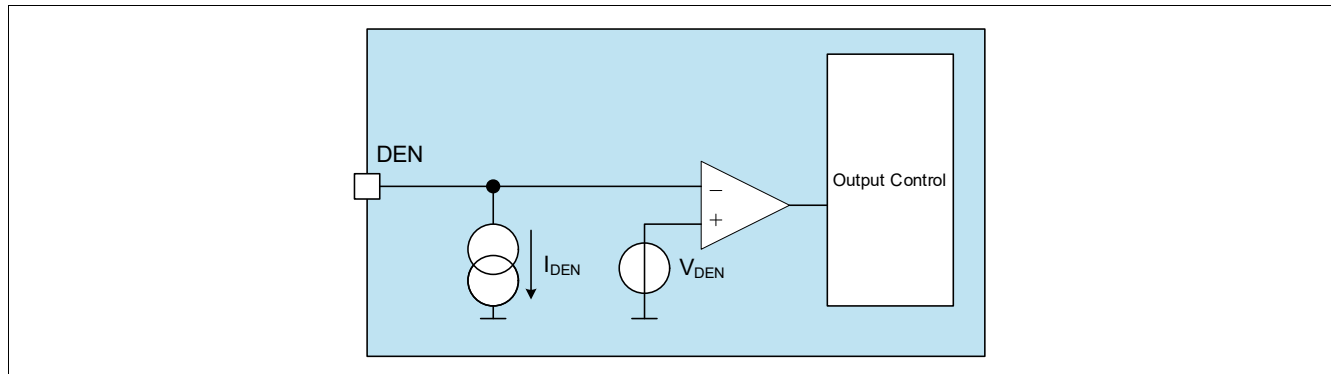
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case	$R_{thJC}$	–	8	10	K/W	<sup>1) 2)</sup>
4.3.2	Junction to Ambient 1s0p board	$R_{thJA1}$	–	61	–	K/W	<sup>1) 3)</sup> $T_a = 85 \text{ °C}$ $T_a = 135 \text{ °C}$
			–	56	–		
4.3.3	Junction to Ambient 2s2p board	$R_{thJA2}$	–	45	–	K/W	<sup>1) 4)</sup> $T_a = 85 \text{ °C}$ $T_a = 135 \text{ °C}$
			–	43	–		

- 1) Not subject to production test, specified by design. Based on simulation results.
- 2) Specified  $R_{thJC}$  value is simulated at natural convection on a cold plate setup (all pins and the exposed Pad are fixed to ambient temperature).  $T_a = 85 \text{ °C}$ , Total power dissipation 1.5 W.
- 3) The  $R_{thJA}$  values are according to Jedec JESD51-3 at natural convection on 1s0p FR4 board. The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 70 µm Cu, 300 mm<sup>2</sup> cooling area. Total power dissipation 1.5 W distributed statically and homogeneously over all power stages.
- 4) The  $R_{thJA}$  values are according to Jedec JESD51-5,-7 at natural convection on 2s2p FR4 board. The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 2 inner copper layers (outside 2 x 70 µm Cu, inner 2 x 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer. Total power dissipation 1.5 W distributed statically and homogeneously over all power stages.

## DEN Pin

### 5 DEN Pin

The DEN pin is a single function pin:



**Figure 3 Block Diagram DEN pin**

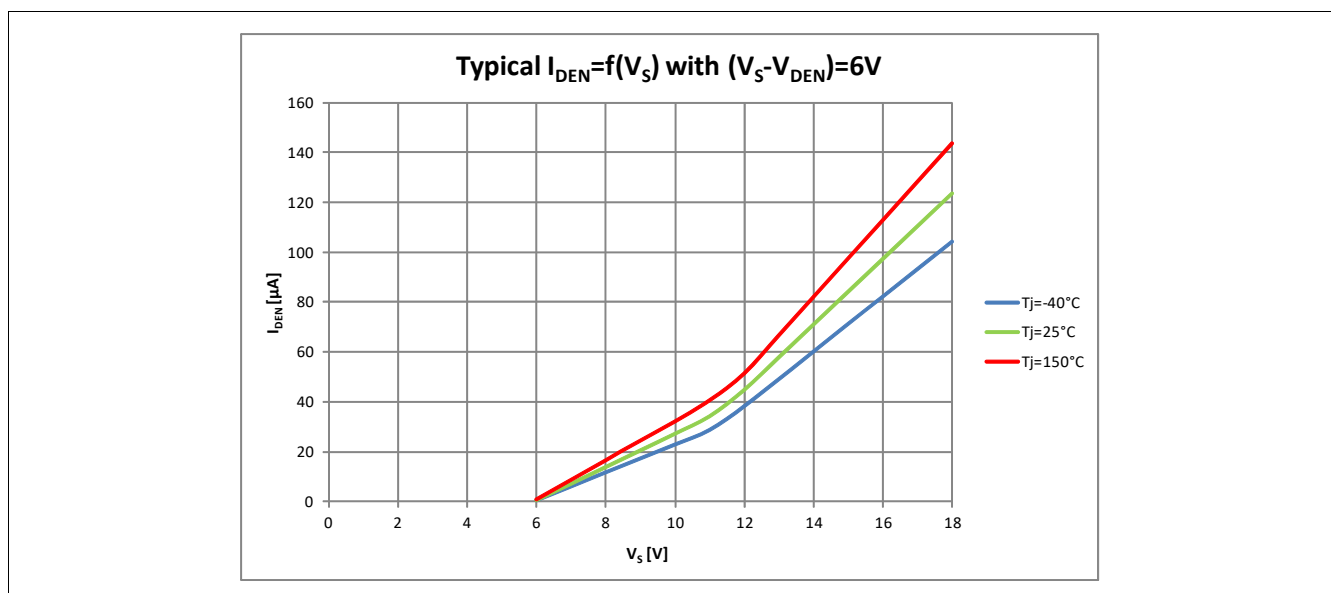
This pin is used to activate or deactivate the device internal diagnosis functions. The diagnostic functions are described in [Chapter 6.2](#), [Chapter 7](#) and [Chapter 8](#). The diagnosis is activated, if the voltage applied at the DEN pin  $V_{DEN}$  is higher than  $V_{DEN(act)}$ . The diagnosis is disabled for voltages below  $V_{DEN(dis)}$ .

A possibility to use the DEN pin is via a Zener diode, which is connected between  $V_S$  and DEN pin. A circuit example is shown in the application information section [Chapter 10](#).

The diagnosis is activated, if the following condition is fulfilled:

$$V_S \geq V_{DEN(act)} + V_{ZD} \quad (1)$$

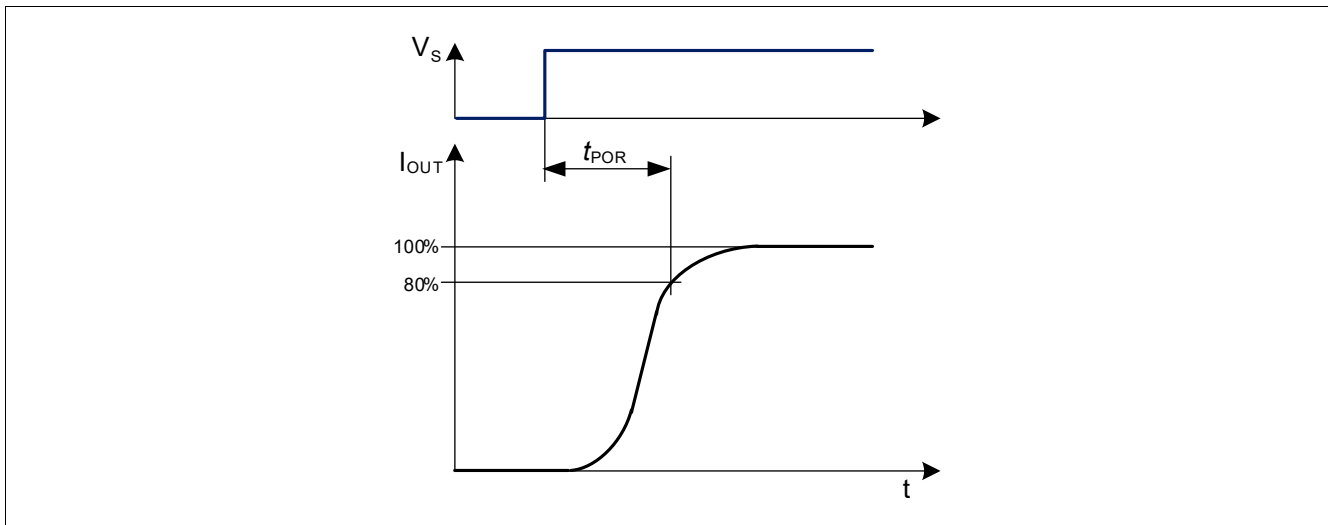
The current consumption on the DEN pin has to be considered for the total device current consumption. The current is specified in [Pos. 5.1.9](#). The typical current consumption  $I_{DEN(H)}$  as a function of the supply voltage  $V_S$  for a Zener diode voltage of  $V_{ZD} = 6\text{ V}$  is shown in the following diagram.



**Figure 4 Typical  $I_{DEN(H)}$  current for a Zener diode voltage of 6 V**

The device and channel turn on is independent of the  $V_{DEN}$ -voltage. After applying a supply voltage the device is activated after the power on reset time  $t_{POR}$ .

DEN Pin



**Figure 5 Power on reset**

The DEN voltage  $V_{\text{DEN}}$  does not influence the disable function via the ST pin. If  $V_{\text{DEN}} < V_{\text{DEN(dis)}}$  the device can still be disabled via the ST pin, if  $V_{\text{ST}} > V_{\text{ST(H)}}$ . For details, please refer to [Chapter 7.3](#).

## 5.1 Electrical Characteristics Internal Supply / DEN Pin

### Electrical Characteristics Internal Supply / DEN pin

Unless otherwise specified:  $V_S = 5.5 \text{ V to } 40 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ,  $R_{\text{SETx}} = 12 \text{ k}\Omega$  all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Current consumption, active mode	$I_{\text{S(on)}}$	–	–	1.9	mA	<sup>1)</sup> $I_{\text{IN\_SET}} = 0 \mu\text{A}$ $T_j < 105^\circ\text{C}$ $V_S = 18 \text{ V}$ $V_{\text{OUTx}} = 3.6 \text{ V}$
5.1.2	Current consumption, device disabled via ST	$I_{\text{S(dis,ST)}}$	–	–	1.7	mA	<sup>1)</sup> $V_S = 18 \text{ V}$ $T_j < 105^\circ\text{C}$ $V_{\text{ST}} = 5 \text{ V}$
5.1.3	Current consumption, device disabled via IN_SETx	$I_{\text{S(dis,IN\_SET)}}$	–	–	1.7	mA	<sup>1)</sup> $V_S = 18 \text{ V}$ $T_j < 105^\circ\text{C}$ $V_{\text{IN\_SETx}} = 5 \text{ V (all)}$
5.1.4	Current consumption, active mode in single fault detection condition with ST-pin unconnected	$I_{\text{S(fault,STu)}}$	–	–	2.1	mA	<sup>1)</sup> $V_S = 18 \text{ V}$ $T_j < 105^\circ\text{C}$ $R_{\text{SETx}} = 12 \text{ k}\Omega$ $V_{\text{OUTx}} = 18 \text{ V or } 0 \text{ V}$

**DEN Pin**

**Electrical Characteristics Internal Supply / DEN pin (cont'd)**

Unless otherwise specified:  $V_S = 5.5 \text{ V}$  to  $40 \text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $R_{SETx} = 12 \text{ k}\Omega$  all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.5	Current consumption, active mode in single fault detection condition with ST-pin connected to GND	$I_{S(\text{fault,STG})}$	–	–	6.2	mA	<sup>1)</sup> $V_S = 18 \text{ V}$ $T_j < 105^\circ\text{C}$ $R_{SET1} = 12 \text{ k}\Omega$ $R_{SET2,3} = \text{unconnected}$ $V_{OUTx} = 18 \text{ V}$ or $0 \text{ V}$ $V_{ST} = 0 \text{ V}$
5.1.6	Current consumption, active mode in double fault detection condition one output disabled via IN_SETx and with ST-pin connected to GND	$I_{S(\text{dfault,STG})}$	–	–	9.2	mA	<sup>1)</sup> $V_S = 18 \text{ V}$ $T_j < 105^\circ\text{C}$ $R_{SET1,2} = 12 \text{ k}\Omega$ $R_{SET3} = \text{unconnected}$ $V_{OUTx} = 18 \text{ V}$ or $0 \text{ V}$ $V_{ST} = 0 \text{ V}$
5.1.7	Power-on reset delay time <sup>2)</sup>	$t_{POR}$	–	–	25	$\mu\text{s}$	<sup>3)</sup> $V_S = 0 \rightarrow 13.5 \text{ V}$ $V_{OUTx(\text{nom})} = 3.6 \pm 0.3 \text{ V}$ $I_{OUTx} = 80\% I_{OUTx(\text{nom})}$
5.1.8	Required supply voltage for current control	$V_{S(\text{CC})}$	–	–	5.5	V	$V_{OUTx} = 3.6 \text{ V}$ $I_{OUTx} \geq 90\% I_{OUTx(\text{nom})}$
5.1.9	DEN high input current	$I_{\text{DEN(H)}}$	–	–	0.1 0.1 0.2 0.4	mA	$T_j < 105^\circ\text{C}$ $V_S = 13.5 \text{ V}$ , $V_{\text{DEN}} = 5.5 \text{ V}$ $V_S = 18 \text{ V}$ , $V_{\text{DEN}} = 5.5 \text{ V}$ $V_S = 18 \text{ V}$ , $V_{\text{DEN}} = 12 \text{ V}$ $V_S = V_{\text{DEN}} = 18 \text{ V}$
5.1.10	DEN activation threshold (diagnosis enabled above $V_{\text{DEN(act)}}$ )	$V_{\text{DEN(act)}}$	2.45	–	3.2	V	$V_S = 8 \dots 18 \text{ V}$
5.1.11	DEN deactivation threshold (diagnosis disabled below $V_{\text{DEN(dis)}}$ )	$V_{\text{DEN(dis)}}$	1.5	–	2.3	V	$V_S = 8 \dots 18 \text{ V}$

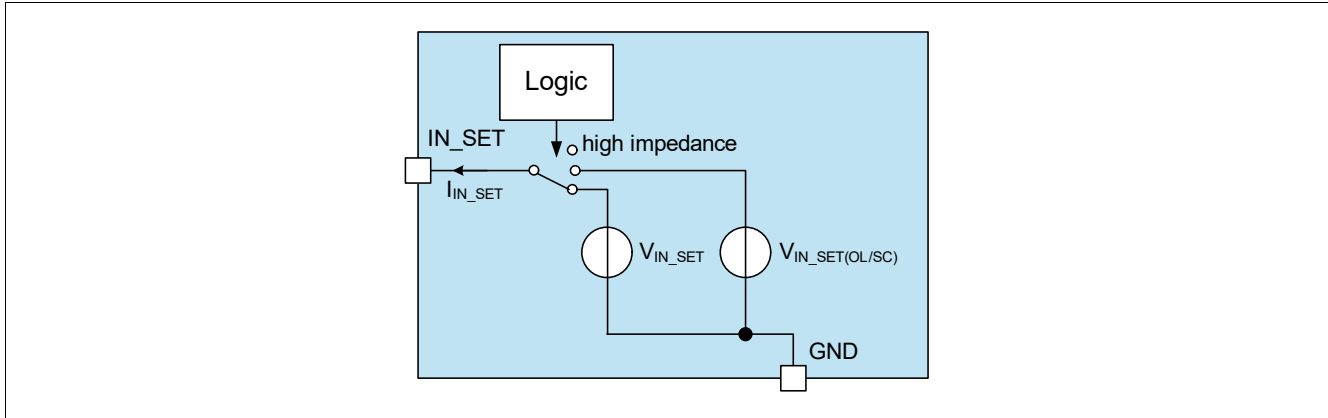
1) The total device current consumption is the sum of the currents  $I_S$  and  $I_{\text{DEN(H)}}$ , please refer to **Pos. 5.1.9**

2) See also **Figure 5**

3) Not subject to production test, specified by design

## 6 IN\_SETx Pin

The IN\_SET pin is a multiple function pin for output current definition, input and diagnostics:



**Figure 6** Block Diagram IN\_SET pin

### 6.1 Output Current Adjustment via RSET

The output current of each channel can be adjusted independently. The current adjustment can be done by placing a low power resistor ( $R_{SET}$ ) at the IN\_SETx pin to ground. The dimensioning of the resistor can be done using the formula below:

$$R_{SET} = \frac{k}{I_{OUT}} \quad (2)$$

The gain factor  $k$  ( $R_{SET} \cdot \text{output current}$ ) is specified in **Pos. 9.2.4** and **Pos. 9.2.5**. The current through the  $R_{SET}$  is defined by the resistor itself and the reference voltage  $V_{IN\_SET(ref)}$ , which is applied to the IN\_SET during supplied device.

### 6.2 Smart Input Pin

The IN\_SETx pin can be connected via  $R_{SET}$  to the open-drain output of a  $\mu C$  or to an external NMOS transistor as described in **Figure 7**. This signal can be used to turn off the output stages of the IC. A minimum IN\_SET current of  $I_{IN\_SET(act)}$  is required to turn on the output stages. This feature is implemented to prevent glimming of LEDs caused by leakage currents on the IN\_SET pin, see **Figure 10** for details. In addition, the IN\_SET pin offers the diagnostic feedback information, if the status pin is connected to GND and  $V_{DEN} > V_{DEN(act)}$  (refer to **Chapter 5**). Another diagnostic possibility is shown in **Figure 8**, where the diagnosis information is provided via the ST pin (refer to **Chapter 7** and **Chapter 8**) to a micro controller. In case of a fault event with the ST pin connected to GND the IN\_SET voltage is increased to  $V_{IN\_SET(OL/SC)}$  **Pos. 8.4.2**. Therefore, the device has two voltage domains at the IN\_SET-pin, which is shown in **Figure 11**.

*Note: If one output has a present fault (open load or short circuit) and one or both of the other channels are dimmed via PWM at the IN\_SET-pins a short spike to  $V_{IN\_SET(OL/SC)}$  is possible. Please refer to **Chapter 8.3**.*

IN\_SETx Pin

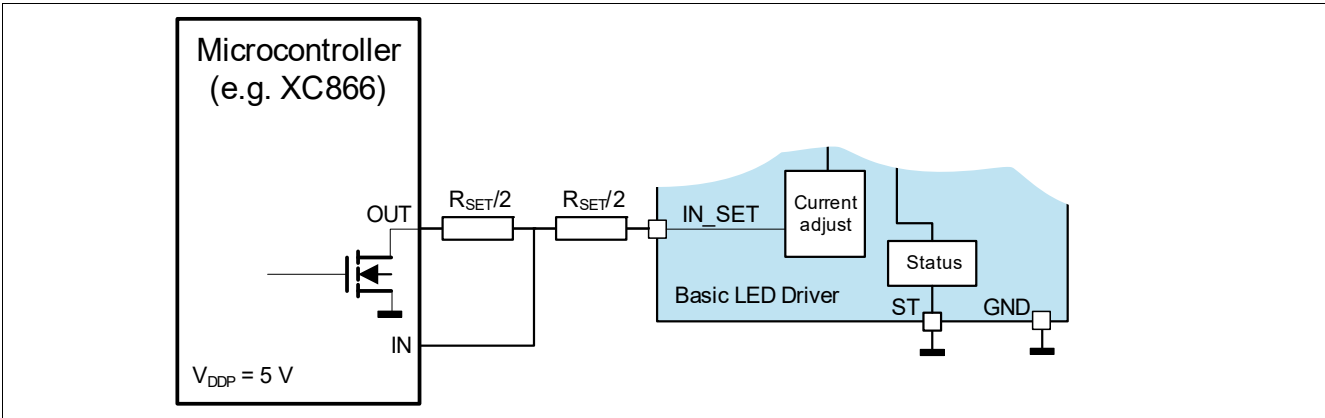


Figure 7 Schematics IN\_SET interface to  $\mu$ C, diagnosis via IN\_SET pin

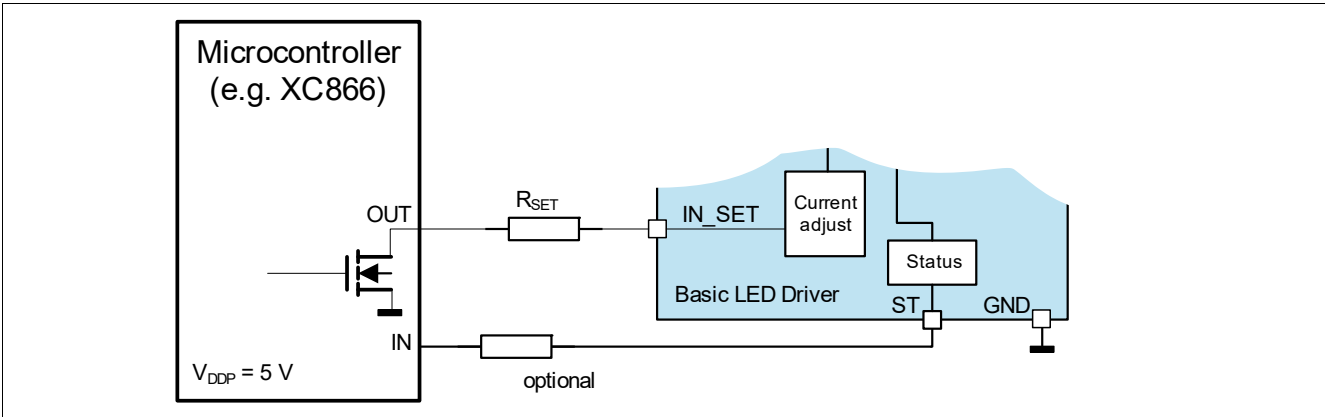


Figure 8 Schematics IN\_SET interface to  $\mu$ C, diagnosis via ST pin

The resulting switching times are shown in [Figure 9](#):

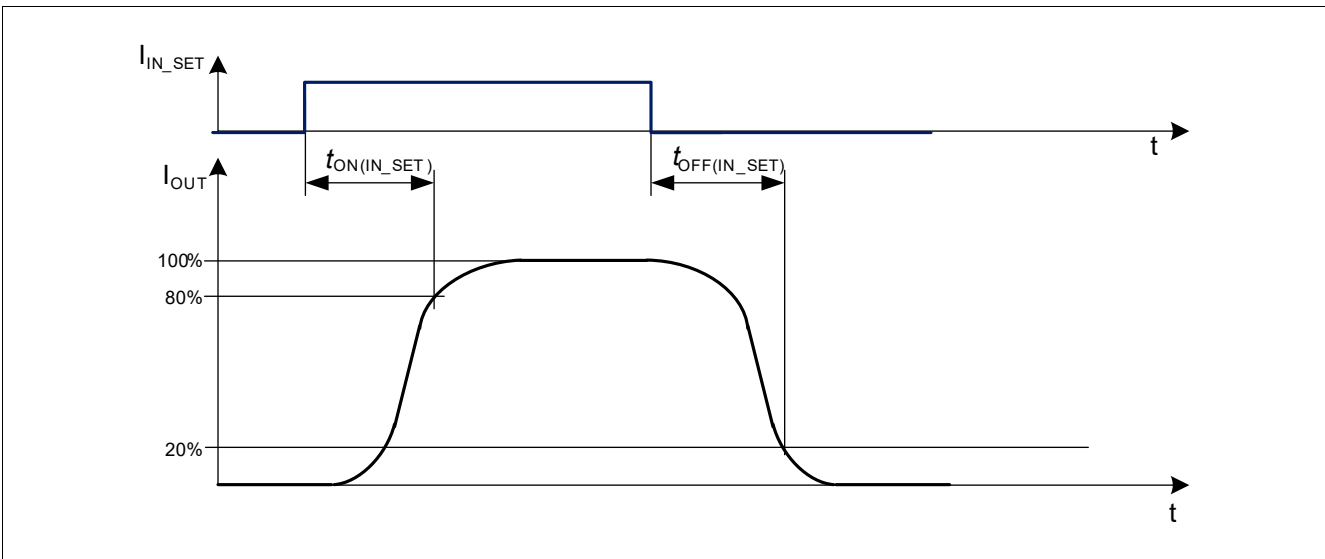


Figure 9 Switching times via IN\_SET

IN\_SETx Pin

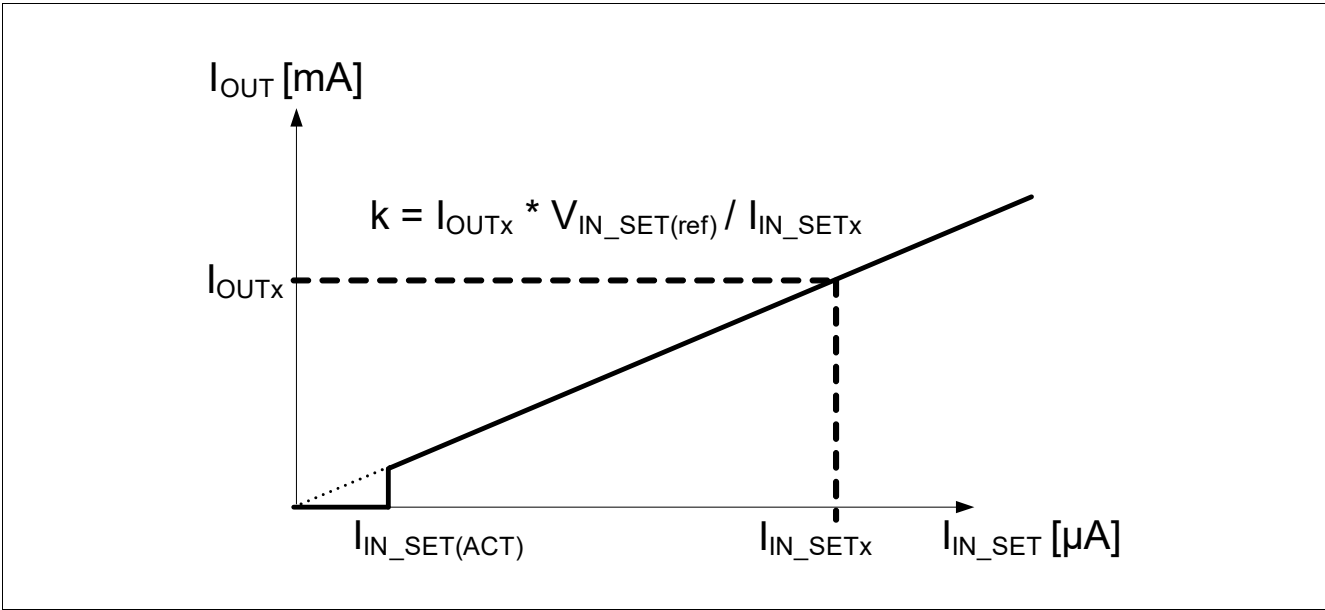


Figure 10  $I_{OUT}$  versus  $I_{IN\_SET}$

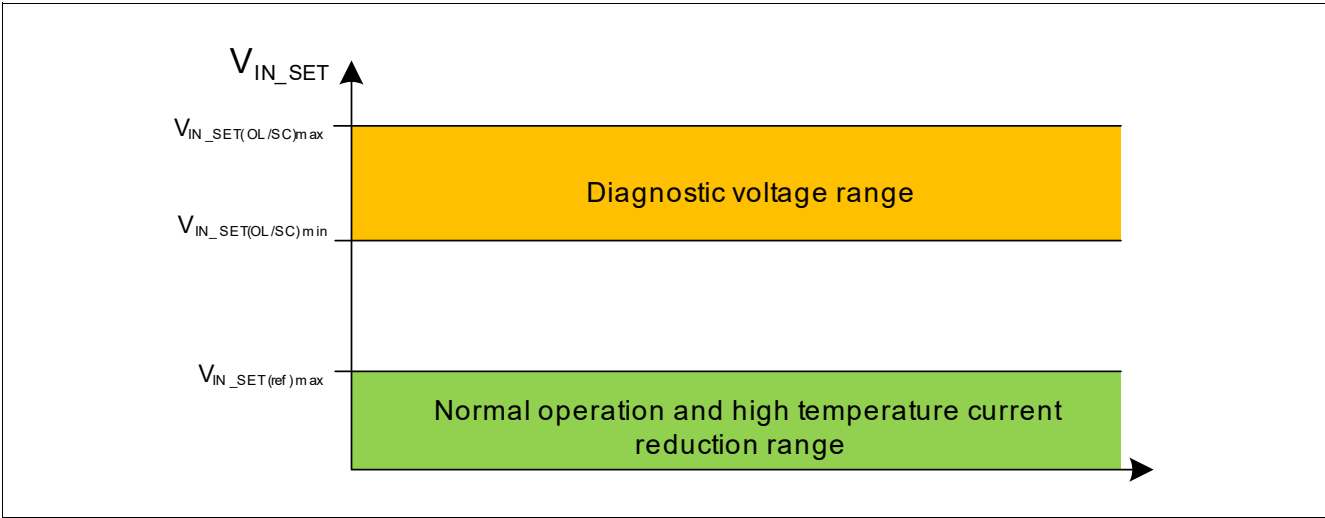


Figure 11 Voltage domains for IN\_SET pin, if ST pin is connected to GND

## ST Pin

### 7 ST Pin

The ST pin is a multiple function pin.

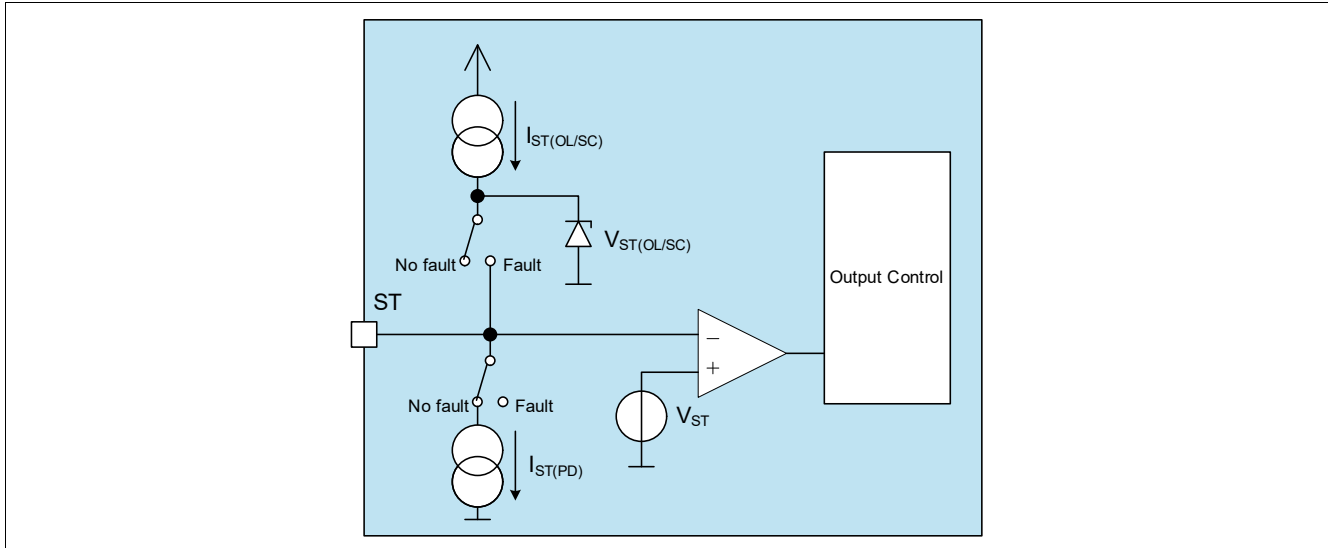


Figure 12 Block Diagram ST pin

#### 7.1 Diagnosis Selector

If the voltage at the DEN pin  $V_{DEN}$  is higher than  $V_{DEN(act)}$ , the diagnosis is activated. For details, please refer to [Chapter 5](#). If the status pin is unconnected or connected to GND via a high ohmic resistor ( $V_{ST}$  to be below  $V_{ST(L)}$ ), the ST pin acts as diagnosis output pin. In normal operation (device is activated) the ST pin is pulled to GND via the internal pull down current  $I_{ST(PD)}$ . In case of an open load or short circuit to GND condition the ST pin is switched to  $V_{ST(OL/SC)}$  after the open load or short circuit detection filter time ([Pos. 8.4.9](#), [Pos. 8.4.12](#)).

If the device is operated in PWM operation via the VS pin the ST pin should be connected to GND via a high ohmic resistor (e.g. 470 kΩ) to ensure proper device behavior during fast rising VS slope.

If the ST pin is shorted to GND the diagnostic feedback is performed via the IN\_SET-pin, which is shown in [Chapter 6.2](#) and [Chapter 8](#).

#### 7.2 Diagnosis Output

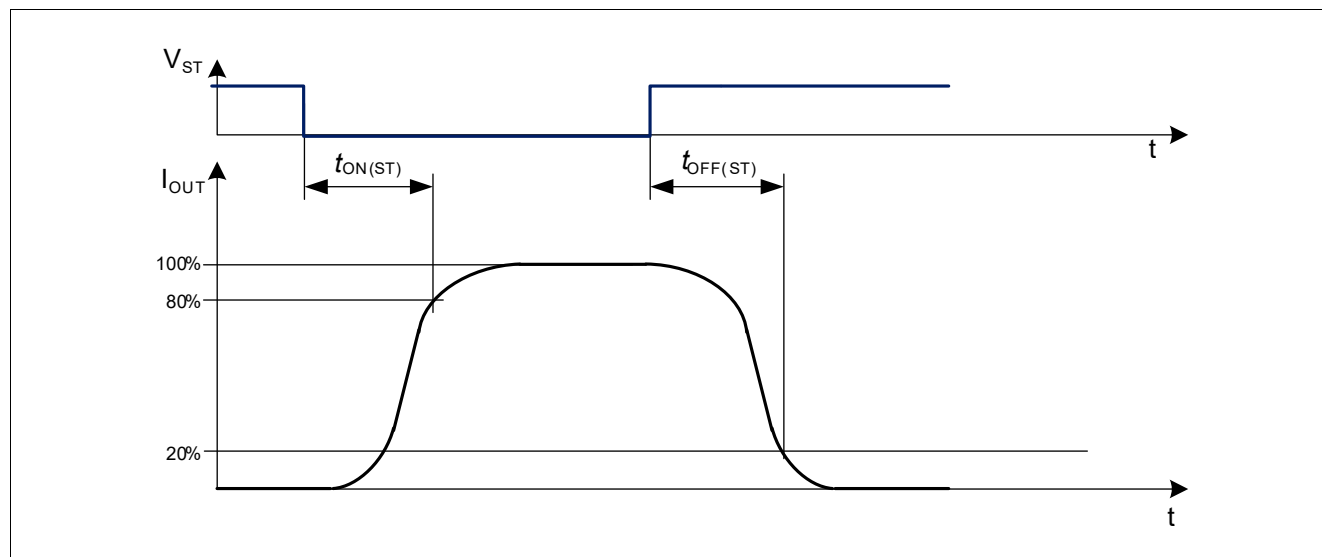
If the status pin is unconnected or connected to GND via a high ohmic resistor ( $V_{ST}$  to be below  $V_{ST(L)}$ ), it acts as a diagnostic output, if the voltage at the DEN pin is above  $V_{DEN(act)}$ . In case of a fault condition the ST pin rises its voltage to  $V_{ST(OL/SC)}$  ([Pos. 8.4.7](#)). Details are shown in [Chapter 8](#).

#### 7.3 Disable Input

If an external voltage higher than  $V_{ST(H)}$  ([Pos. 8.4.5](#)) is applied to the ST pin, the device is switched off. This function is working independently of the voltage at the DEN pin. Even if the diagnosis is disabled via  $V_{DEN} < V_{DEN(dis)}$  the disable function of the ST pin is working. This function is used for applications, where multiple drivers should be used for one light function. It is possible to combine the drivers' fault diagnosis via the ST pins. If a single LED chain fails, the entire light function is switched off. In this scenario e.g. the diagnostic circuit on the body control module can easily distinguish between the two cases (normal load or load fault), because nearly no current is flowing into the LED module during the fault scenario - the drivers consume a current of  $I_{S(fault,STu)}$  ([Pos. 5.1.4](#)) or  $I_{S(dis,ST)}$  ([Pos. 5.1.2](#)).

## ST Pin

As soon as one LED chain fails, the ST-pin of this device is switched to  $V_{ST(OL/SC)}$ . The other devices used for the same light function can be connected together via the ST pins. This leads to a switch off of all devices connected together.



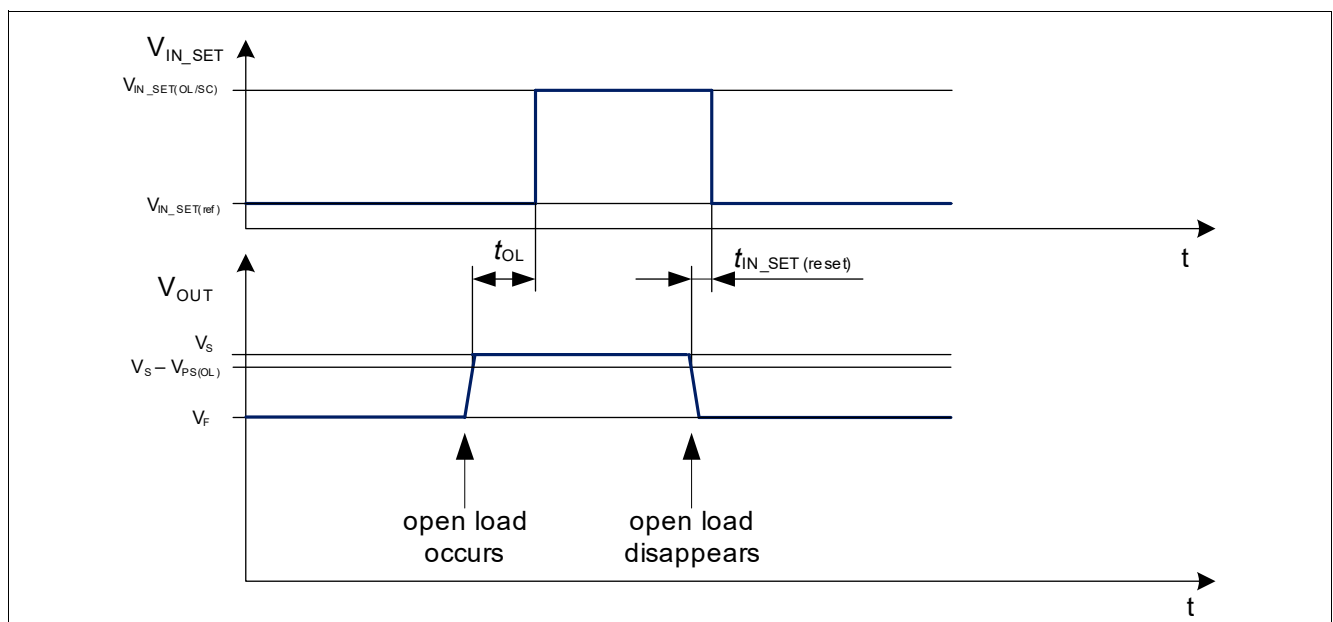
**Figure 13** Switching times via ST Pin

## 8 Load Diagnosis

The diagnosis function is enabled, if the voltage at the DEN pin  $V_{\text{DEN}}$  is above  $V_{\text{DEN(act)}}$  as described in [Chapter 5](#).

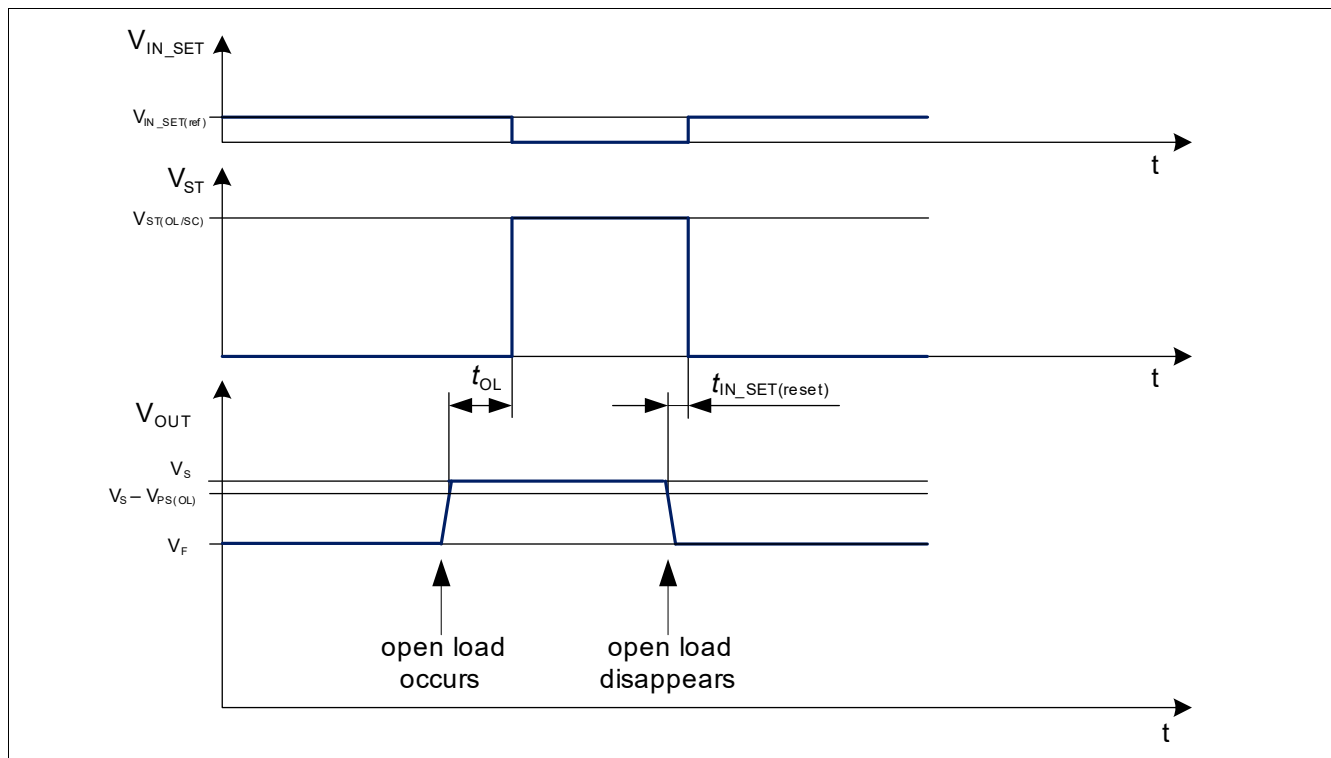
### 8.1 Open Load

An open load diagnosis feature is integrated in the TLD2314EL driver IC. If there is an open load on one of the outputs, the respective output is turned off. The potential on the IN\_SET pin rises up to  $V_{\text{IN\_SET(OL/SC)}}$ , if the ST is connected to GND. This high voltage can be used as input signal for a  $\mu\text{C}$  as shown in [Figure 8](#). If the ST pin is open or connected to GND via a high ohmic resistor, the ST pin rises to a high potential as described in [Chapter 7](#). More details are shown in [Figure 17](#). The open load status is not latched, as soon as the open load condition is no longer present, the output stage will be turned on again. An open load condition is detected, if the voltage drop over the output stage  $V_{\text{PS}}$  is below the threshold according [Pos. 8.4.10](#) and a filter time of  $t_{\text{OL}}$  is passed.



**Figure 14** IN\_SET behavior during open load condition with ST pin connected to GND and  $V_{\text{DEN}} > V_{\text{DEN(act)}}$

## Load Diagnosis



**Figure 15** IN\_SET and ST behavior during open load condition (ST unconnected) and  $V_{DEN} > V_{DEN(act)}$

## 8.2 Short Circuit to GND detection

The TLD2314EL has an integrated SC to GND detection. If the output stage is turned on and the voltage at the output falls below  $V_{OUT(SC)}$  the potential on the IN\_SET pin is increased up to  $V_{IN\_SET(OL/SC)}$  after  $t_{SC}$ , if the ST pin is connected to GND. If the ST is open or connected to GND via a high ohmic resistor the fault is indicated on the ST pin according to [Chapter 7](#) after  $t_{SC}$ . More details are shown in [Figure 17](#). This condition is not latched. For detecting a normal condition after a short circuit detection an output current according to  $I_{OUT(SC)}$  is driven by the channel.

Load Diagnosis

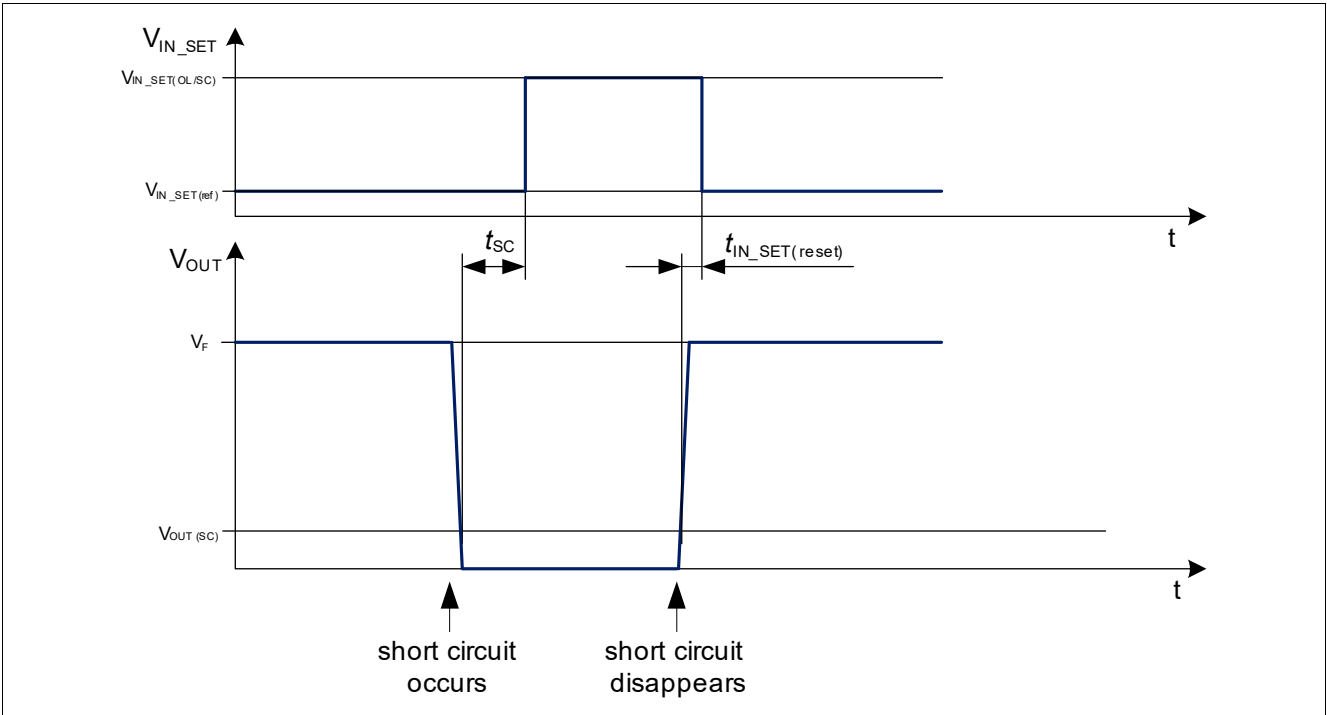


Figure 16  $V_{IN\_SET}$  behavior during short circuit to GND condition with ST connected to GND and  $V_{DEN} > V_{DEN(act)}$

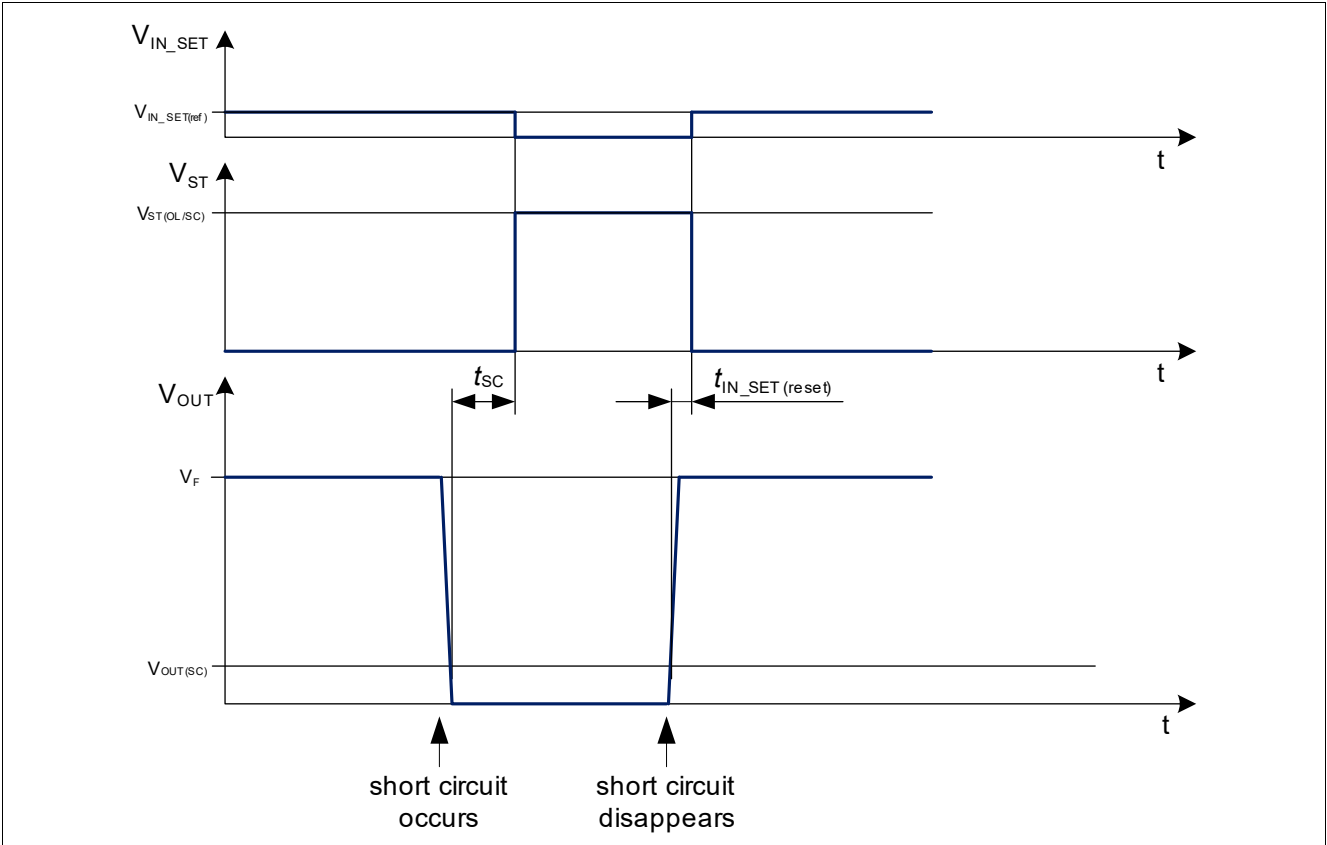
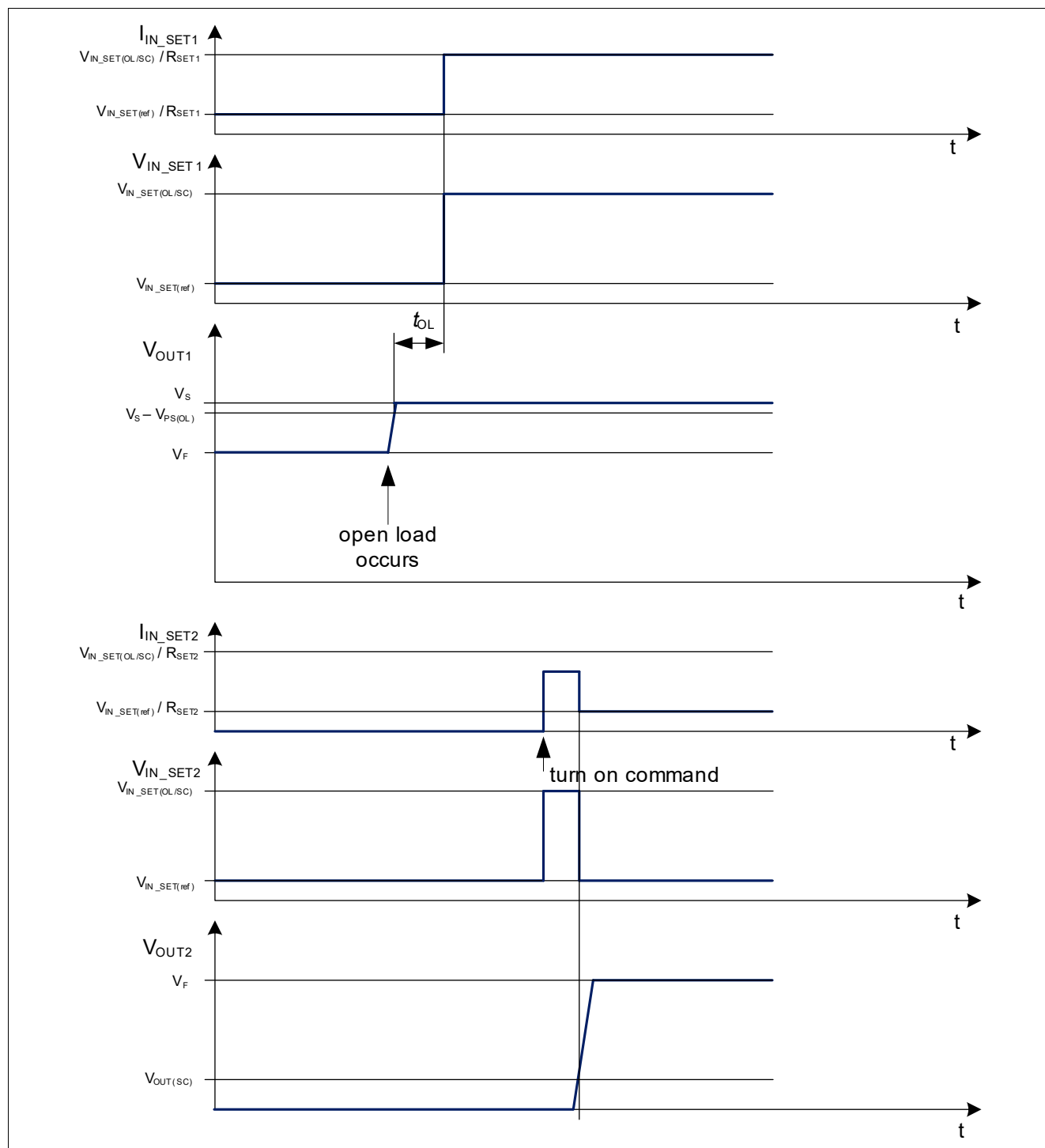


Figure 17  $V_{IN\_SET}$  and  $V_{ST}$  behavior during short circuit to GND condition (ST unconnected) and  $V_{DEN} > V_{DEN(act)}$

### 8.3 Double Fault Conditions

The TLD2314EL allows the diagnosis of each channel separately, as long as the ST-pin is shorted to GND. The diagnosis filter times  $t_{OL}$  and  $t_{SC}$  ([Pos. 8.4.9](#) and [Pos. 8.4.12](#)) are valid only for the channel, which diagnoses first the fault condition. For the other channel or channels with a subsequential fault the diagnosis is reported immediately without the diagnosis filter time, if the filter time  $t_{OL}$  has been elapsed for the channel with the first fault. During activation via IN\_SET of a non-faulty output, where one channel has already a fault detected, a short spike to  $V_{IN\_SET(OL/SC)}$  could occur on the channel, which should be activated. Therefore, in general a diagnosis should be done earliest after the diagnosis filter times  $t_{OL}$  and  $t_{SC}$  to avoid any incorrect diagnosis readout. In the scenario mentioned above the turn on time  $t_{ON(IN\_SET)}$  could be extended. The following figure shows the example behavior, if OUT1 has a fault and OUT2 is operated in PWM-mode. OUT3 is disabled.

## Load Diagnosis



**Figure 18** Example single channel fault on OUT1 and PWM-operation on OUT2 with ST pin connected to GND and  $V_{DEN} > V_{DEN(act)}$

## Load Diagnosis

### 8.4 Electrical Characteristics IN\_SET Pin and Load Diagnosis

#### Electrical Characteristics IN\_SET pin and Load Diagnosis

Unless otherwise specified:  $V_S = 5.5 \text{ V}$  to  $40 \text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $R_{SETX} = 12 \text{ k}\Omega$ ,  $V_{DEN} = 5.5 \text{ V}$ , all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.4.1	IN_SET reference voltage	$V_{IN\_SET(ref)}$	1.19	1.23	1.27	V	<sup>1)</sup> $V_{OUTx} = 3.6 \text{ V}$ $T_j = 25...115^\circ\text{C}$
8.4.2	IN_SET open load/short circuit voltage	$V_{IN\_SET(OL/SC)}$	4	–	5.5	V	<sup>1)</sup> $V_S > 8 \text{ V}$ $T_j = 25...150^\circ\text{C}$ $V_S = V_{OUTx} \text{ (OL) or } V_{OUTx} = 0 \text{ V (SC)}$
8.4.3	IN_SET open load/short circuit current	$I_{IN\_SET(OL/SC)}$	0.5	–	2.5	mA	<sup>1)</sup> $V_S > 8 \text{ V}$ $T_j = 25...150^\circ\text{C}$ $V_{IN\_SET} = 4 \text{ V}$ $V_S = V_{OUTx} \text{ (OL) or } V_{OUT} = 0 \text{ V (SC)}$
8.4.4	ST device turn on threshold (active low) in case of voltage applied from external (ST-pin acting as input)	$V_{ST(L)}$	0.8	–	–	V	–
8.4.5	ST device turn off threshold (active low) in case of voltage applied from external (ST-pin acting as input)	$V_{ST(H)}$	–	–	2.5	V	–
8.4.6	ST pull down current	$I_{ST(PD)}$	–	–	15	$\mu\text{A}$	$V_{ST} = 0.8 \text{ V}$
8.4.7	ST open load/short circuit voltage (ST-pin acting as diagnosis output)	$V_{ST(OL/SC)}$	4	–	5.5	V	<sup>1)</sup> $V_S > 8 \text{ V}$ $T_j = 25...150^\circ\text{C}$ $R_{ST} = 470 \text{ k}\Omega$ $V_S = V_{OUTx} \text{ (OL) or } V_{OUT} = 0 \text{ V (SC)}$
8.4.8	ST open load/short circuit current (ST-pin acting as diagnosis output)	$I_{ST(OL/SC)}$	100	–	220	$\mu\text{A}$	<sup>1)</sup> $V_S > 8 \text{ V}$ $T_j = 25...150^\circ\text{C}$ $V_{ST} = 2.5 \text{ V}$ $V_S = V_{OUTx} \text{ (OL) or } V_{OUT} = 0 \text{ V (SC)}$
8.4.9	OL detection filter time	$t_{OL}$	10	22	35	$\mu\text{s}$	<sup>1)</sup> $V_S > 8 \text{ V}$
8.4.10	OL detection voltage $V_{PS(OL)} = V_S - V_{OUTx}$	$V_{PS(OL)}$	0.2	–	0.4	V	$V_S > 8 \text{ V}$
8.4.11	Short circuit to GND detection threshold	$V_{OUT(SC)}$	0.8	–	1.4	V	$V_S > 8 \text{ V}$
8.4.12	SC detection filter time	$t_{SC}$	10	22	35	$\mu\text{s}$	<sup>1)</sup> $V_S > 8 \text{ V}$

## Load Diagnosis

### Electrical Characteristics IN\_SET pin and Load Diagnosis (cont'd)

Unless otherwise specified:  $V_S = 5.5 \text{ V}$  to  $40 \text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $R_{SETx} = 12 \text{ k}\Omega$ ,  $V_{DEN} = 5.5 \text{ V}$ , all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.4.13	IN_SET diagnosis reset time	$t_{IN\_SET(reset)}$	–	5	20	$\mu\text{s}$	<sup>1)</sup> $V_S > 8 \text{ V}$
8.4.14	SC detection current in case of unconnected ST-pin	$I_{OUT(SC,STu)}$	100	200	300	$\mu\text{A}$	$V_S > 8 \text{ V}$ $V_{OUTx} = 0 \text{ V}$
8.4.15	SC detection current in case of ST-pin shorted to GND	$I_{OUT(SC,STG)}$	0.1	2	4.75	$\text{mA}$	$V_S > 8 \text{ V}$ $V_{OUTx} = 0 \text{ V}$ $V_{ST} = 0 \text{ V}$
8.4.16	IN_SET activation current without turn on of output stages	$I_{IN\_SET(act)}$	2	–	15	$\mu\text{A}$	See <b>Figure 10</b>

1) Not subject to production test, specified by design

## Power Stage

## 9 Power Stage

The output stages are realized as high side current sources with a current of 120 mA. During off state the leakage current at the output stage is minimized in order to prevent a slightly glowing LED. To increase the overall output current for high brightness LED applications it is possible to connect two or all three output stages in parallel.

The maximum current of each channel is limited by the power dissipation and used PCB cooling areas (which results in the applications  $R_{thJA}$ ).

For an operating current control loop the supply and output voltages according to the following parameters have to be considered:

- Required supply voltage for current control  $V_{S(CC)}$ , **Pos. 5.1.8**
- Voltage drop over output stage during current control  $V_{PS(CC)}$ , **Pos. 9.2.6**
- Required output voltage for current control  $V_{OUTx(CC)}$ , **Pos. 9.2.7**

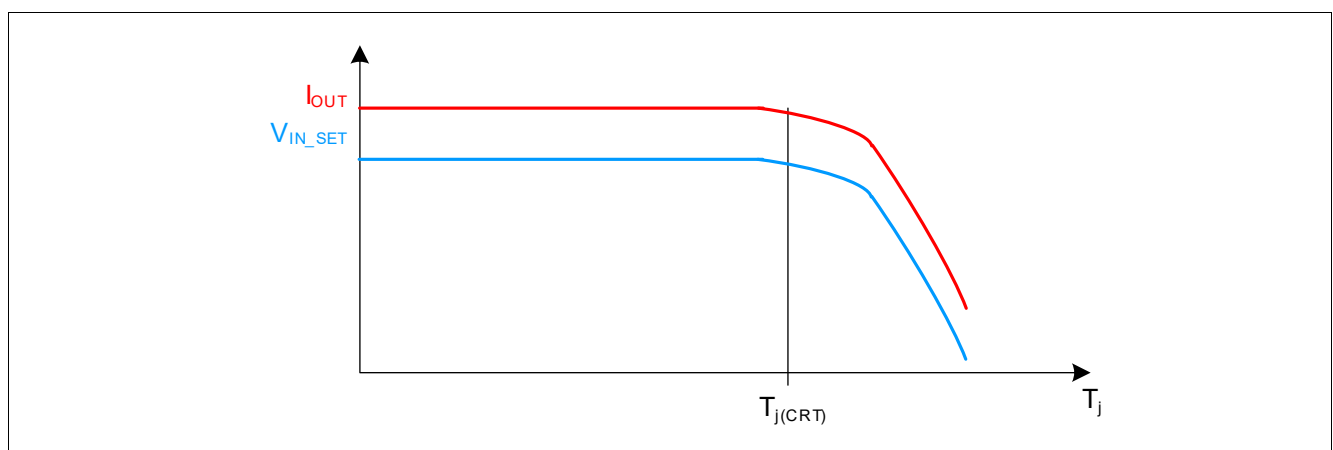
### 9.1 Protection

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

#### 9.1.1 Over Load Behavior

An over load detection circuit is integrated in the LITIX™ Basic IC. It is realized by a temperature monitoring of the output stages (OUTx).

As soon as the junction temperature exceeds the current reduction temperature threshold  $T_{j(CRT)}$  the output current will be reduced by the device by reducing the IN\_SET reference voltage  $V_{IN\_SET(ref)}$ . This feature avoids LED's flickering during static output overload conditions. Furthermore, it protects LEDs against over temperature, which are mounted thermally close to the device. If the device temperature still increases, the three output currents decrease close to 0 A. As soon as the device cools down the output currents rise again.



**Figure 19 Output current reduction at high temperature**

*Note: This high temperature output current reduction is realized by reducing the IN\_SET reference voltage (**Pos. 8.4.1**). In case of very high power loss applied to the device and very high junction temperature the output current may drop down to  $I_{OUTx} = 0$  mA, after a slight cooling down the current increases again.*

## Power Stage

### 9.1.2 Reverse Battery Protection

The TLD2314EL has an integrated reverse battery protection feature. This feature protects the driver IC itself, but also connected LEDs. The output reverse current is limited to  $I_{OUTx(Rev)}$  by the reverse battery protection.

*Note: Due to the reverse battery protection a reverse protection diode for the light module may be obsolete. In case of high ISO-pulse requirements and only minor protecting components like capacitors a reverse protection diode may be reasonable. The external protection circuit needs to be verified in the application.*

## 9.2 Electrical Characteristics Power Stage

### Electrical Characteristics Power Stage

Unless otherwise specified:  $V_S = 5.5\text{ V to }18\text{ V}$ ,  $T_j = -40^\circ\text{C to }+150^\circ\text{C}$ ,  $V_{OUTx} = 3.6\text{ V}$ , all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.2.1	Output leakage current	$I_{OUTx(leak)}$	–	–	7 3	$\mu\text{A}$	$I_{IN\_SET} = 0\text{ }\mu\text{A}$ $V_{OUTx} = 2.5\text{ V}$ $T_j = 150^\circ\text{C}$ <sup>1)</sup> $T_j = 85^\circ\text{C}$
9.2.2	Output leakage current in boost over battery setup	$I_{OUTx(leak,B2B)}$	–	–	50	$\mu\text{A}$	<sup>1)</sup> $I_{IN\_SET} = 0\text{ }\mu\text{A}$ $V_{OUTx} = V_S = 40\text{ V}$
9.2.3	Reverse output current	$-I_{OUTx(Rev)}$	–	–	1	$\mu\text{A}$	<sup>1)</sup> $V_S = -16\text{ V}$ Output load: LED with break down voltage < -0.6 V
9.2.4	Output current accuracy limited temperature range	$k_{LT}$	697 645	750 750	803 855		<sup>1)</sup> $T_j = 25...115^\circ\text{C}$ $V_S = 8...18\text{ V}$ $V_{PS} = 2\text{ V}$ $R_{SETx} = 6...12\text{ k}\Omega$ $R_{SETx} = 30\text{ k}\Omega$
9.2.5	Output current accuracy over temperature	$k_{ALL}$	697 645	750 750	803 855		<sup>1)</sup> $T_j = -40...115^\circ\text{C}$ $V_S = 8...18\text{ V}$ $V_{PS} = 2\text{ V}$ $R_{SETx} = 6...12\text{ k}\Omega$ $R_{SETx} = 30\text{ k}\Omega$
9.2.6	Voltage drop over power stage during current control $V_{PS(CC)} = V_S - V_{OUTx}$	$V_{PS(CC)}$	0.75	–	–	V	<sup>1)</sup> $V_S = 13.5\text{ V}$ $R_{SETx} = 12\text{ k}\Omega$ $I_{OUTx} \geq 90\%$ of $(k_{LT(typ)}/R_{SETx})$
9.2.7	Required output voltage for current control	$V_{OUTx(CC)}$	2.3	–	–	V	<sup>1)</sup> $V_S = 13.5\text{ V}$ $R_{SETx} = 12\text{ k}\Omega$ $I_{OUTx} \geq 90\%$ of $(k_{LT(typ)}/R_{SETx})$

**Power Stage**

**Electrical Characteristics Power Stage (cont'd)**

Unless otherwise specified:  $V_S = 5.5 \text{ V}$  to  $18 \text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{\text{OUTx}} = 3.6 \text{ V}$ , all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.2.8	Maximum output current	$I_{\text{OUT(max)}}$	120	–	–	mA	$R_{\text{SETx}} = 4.7 \text{ k}\Omega$ The maximum output current is limited by the thermal conditions. Please refer to <b>Pos. 4.3.1 - Pos. 4.3.3</b>
9.2.9	ST turn on time	$t_{\text{ON(ST)}}$	–	–	15	$\mu\text{s}$	<sup>2)</sup> $V_S = 13.5 \text{ V}$ $R_{\text{SETx}} = 12 \text{ k}\Omega$ ST $\rightarrow$ L $I_{\text{OUTx}} = 80\%$ of $(k_{\text{LT(typ)}}/R_{\text{SETx}})$
9.2.10	ST turn off time	$t_{\text{OFF(ST)}}$	–	–	10	$\mu\text{s}$	<sup>2)</sup> $V_S = 13.5 \text{ V}$ $R_{\text{SETx}} = 12 \text{ k}\Omega$ ST $\rightarrow$ H $I_{\text{OUTx}} = 20\%$ of $(k_{\text{LT(typ)}}/R_{\text{SETx}})$
9.2.11	IN_SET turn on time	$t_{\text{ON(IN\_SET)}}$	–	–	15	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ $I_{\text{IN\_SET}} = 0 \rightarrow 100 \mu\text{A}$ $I_{\text{OUTx}} = 80\%$ of $(k_{\text{LT(typ)}}/R_{\text{SETx}})$
9.2.12	IN_SET turn off time	$t_{\text{OFF(IN\_SET)}}$	–	–	10	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ $I_{\text{IN\_SET}} = 100 \rightarrow 0 \mu\text{A}$ $I_{\text{OUTx}} = 20\%$ of $(k_{\text{LT(typ)}}/R_{\text{SETx}})$
9.2.13	Current reduction temperature threshold	$T_{j(\text{CRT})}$	–	140	–	$^\circ\text{C}$	<sup>1)</sup> $I_{\text{OUTx}} = 95\%$ of $(k_{\text{LT(typ)}}/R_{\text{SETx}})$
9.2.14	Output current during current reduction at high temperature	$I_{\text{OUT(CRT)}}$	85% of $(k_{\text{LT(typ)}}/R_{\text{SETx}})$	–	–	A	<sup>1)</sup> $R_{\text{SETx}} = 12 \text{ k}\Omega$ $T_j = 150^\circ\text{C}$

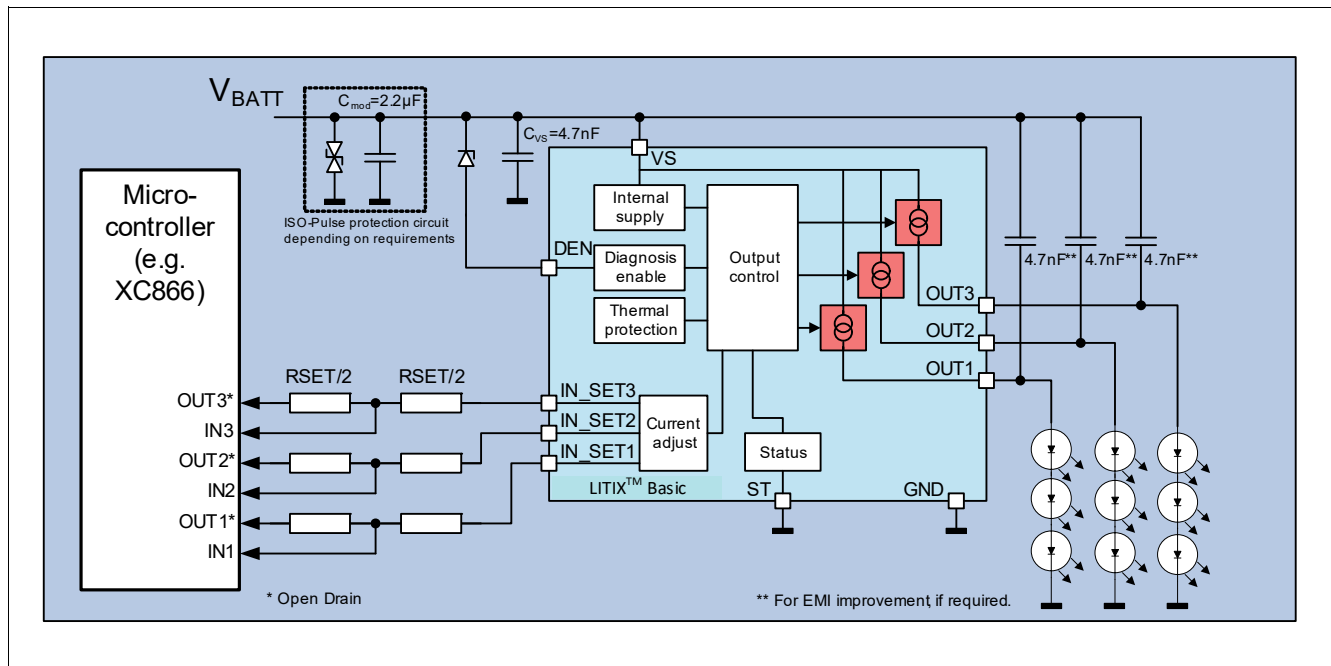
1) Not subject to production test, specified by design

2) see also **Figure 13**

## Application Information

### 10 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*



**Figure 20 Application Diagram with Diagnosis for each channel**

*Note: This is a very simplified example of an application circuit. In case of high ISO-pulse requirements a reverse protection diode may be used for LED protection. The function must be verified in the real application.*

#### 10.1 Further Application Information

- For further information you may contact <http://www.infineon.com/>

**Figure 21 PG-SSOP-14**

## Revision History

## 12 Revision History

Revision	Date	Changes
1.0	2013-08-08	Initial revision of data sheet
1.1	2015-03-19	Updated parameters $K_{LT}$ and $K_{ALL}$ in the chapter Power Stage
1.2	2018-04-26	Updated to latest template
1.2	2018-04-26	Updated application drawing
1.2	2018-04-26	Updated package marking
1.2	2018-04-26	Updated package figure
1.21	2021-07-05	Corrected cross references in <a href="#">Chapter 5.1</a> Footnote <sup>2)</sup>

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