REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18															

REV STATUS	REV													
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
15-11-02

REVISION LEVEL

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, HYBRID, LINEAR, SINGLE CHANNEL, DC/DC CONVERTER

SIZE	CAGE CODE	
A	**67268**	**5962-15224**

SHEET 1 OF 18

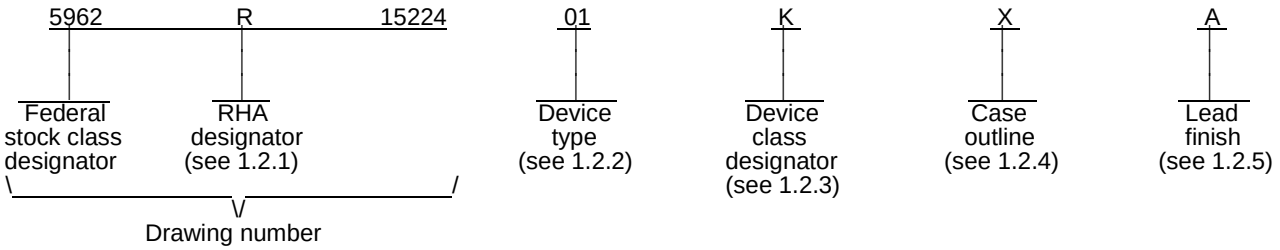
DSCC FORM 2233
APR 97

5962-E530-15

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices meet the MIL-PRF-38534 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	LSO2801R5S	DC-DC Converter, 12 W, +1.5 V Output
02	LSO2801R8S	DC-DC Converter, 14.4 W, +1.8 V Output
03	LSO2802R5S	DC-DC Converter, 20 W, +2.5 V Output
04	LSO2803R3S	DC-DC Converter, 25 W, +3.3 V Output
05	LSO2805S	DC-DC Converter, 20 W, +5 V Output
06	LSO2812S	DC-DC Converter, 30 W, +12 V Output
07	LSO2815S	DC-DC Converter, 30 W, +15 V Output

1.2.3 Device class designator. This device class designator is a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

Device class	Device performance documentation
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C, and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	13	Straight leads with side mounting tabs

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/ 2/

Input Voltage (Continuous)	60 V dc
Case Operating Temperature Range (T_C)	-55°C to +125 °C
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature	-55 °C to +130 °C

1.4 Recommended operating conditions.

Input voltage range	+18 V dc to +40 V dc
Case operating temperature range (T_C)	-55°C to +85°C

1.5 Radiation features. 3/

Maximum total dose available (dose rate = 50 - 300 rads(Si)/s)	100 krad(Si) 4/ 5/
Neutron Irradiation (1 MeV equivalent neutrons)	$1x10^{12}$ n/cm^2 6/
Single event phenomenon (SEP) effective linear energy transfer (LET):	
No SEL, SEB, SEFI, SEGR	$\leq$ 82 MeV-cm^2/mg 7/
SEU	$\leq$ 82 MeV-cm^2/mg 8/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-19500 - Semiconductor Devices, General Specification for.
MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.
MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.
MIL-STD-750 - Test Method Standard for Semiconductor Devices

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Device types 01 through 07 operation between +85°C and +125°C is guaranteed, but no parametric limits are specified in Table IA. For operation above the recommended maximum case temperature of +85°C contact the approved source of supply.
3/ See 4.3.5 for the manufacturer's radiation hardness assurance analysis and testing.
4/ A representative device has been High Dose Rate (HDR) tested using Condition A of Method 1019 of MIL-STD-883 to 150 krad(Si) to ensure Radiation Hardness Assurance designator levels "L" of 50 krad(si) and "R" of 100 krad(si). A representative device will be re-tested after design or process changes that may affect the RHA response of these devices.
5/ The devices on this SMD have not been characterized for Enhanced Low Dose Rate Sensitivity (ELDRS).
6/ Linear bipolar integrated circuit and bipolar semiconductor components are tested per method 1017 of MIL-STD-883 to ($1x10^{12}$ n/cm$^{2)}$.
7/ Single event performance is tested on representative devices. No Gate Ruptures, Latch-up, Burn-out, or Single Event Function Interrupts were exhibited to the limit specified. See table IB.
8/ Single event upsets (transient voltages) observed were within the limit specified in Table IB.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

Copies of these documents are available online at http://www.astm.org/

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DLA Land and Maritime-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DLA Land and Maritime-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime-VA, or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_C as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +85°C$, V_{IN} = +28 V dc ± 5%, Full Load, C_L = 0 unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output voltage	V_{OUT}	V_{IN} = 18 V dc to 40 V dc, I_{OUT} = 8 A	1	01	1.48	1.52	V dc
			2,3		1.47	1.53	
			1	02	1.78	1.82	
			2,3		1.77	1.83	
			1	03	2.48	2.52	
			2,3		2.47	2.53	
		L, R 2/ 3/	1,2,3	01	1.455	1.545	
				02	1.746	1.854	
				03	2.425	2.575	
		V_{IN} = 18 V dc to 40 V dc, I_{OUT} = 7.57 A	1	04	3.28	3.32	
			2,3		3.27	3.33	
		L, R 2/ 3/	1,2,3		3.201	3.399	
		V_{IN} = 18 V dc to 40 V dc, I_{OUT} = 6 A	1	05	4.97	5.03	
			2,3		4.95	5.05	
		L, R 2/ 3/	1,2,3		4.85	5.15	
		V_{IN} = 18 V dc to 40 V dc, I_{OUT} = 2.5 A	1	06	11.94	12.06	
			2,3		11.88	12.12	
		L, R 2/ 3/	1,2,3		11.64	12.36	
		V_{IN} = 18 V dc to 40 V dc, I_{OUT} = 2 A	1	07	14.92	15.08	
			2,3		14.85	15.15	
		L, R 2/ 3/	1,2,3		14.55	15.45	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +85°C$ V_{IN} = +28 V dc ± 5% Full Load, C_L = 0 unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output Current 4/	I_{OUT}	V_{IN} = 18 V dc to 40 V dc 2/		01		8.00	A
				02		8.00	
				03		8.00	
				04		7.57	
				05		6.00	
				06		2.50	
				07		2.00	
V_{OUT} Ripple Voltage	V_{RIP}	BW = 20 kHz to 10 MHz V_{IN} = 18 V, 28 V, 40 V dc 100 % load	1,2,3	01, 02, 03, 04		18	mVp-p
		L, R 2/ 3/				35	
				05, 07		30	
		L, R 2/ 3/				50	
				06		30	
		L, R 2/ 3/				70	
V_{OUT} Line Regulation 5/	VR_{LINE}	V_{IN} = 18 V, 28 V, 40 V dc 0%, 50%, 100 % load 2/	1,2,3	All	-0.5	0.5	%
V_{OUT} Load Regulation 5/	VR_{LOAD}	V_{IN} = 18 V, 28 V, 40 V dc 0%, 50%, 100 % load 2/	1,2,3	All	-1.0	1.0	%
Total Regulation (Line and Load) 5/		V_{IN} = 18 to 40 V dc 0% to 100 % load 2/	1,2,3	All	-1.0	1.0	%
Input Current 6/	I_{IN}	Pin 4 shorted to pin 3 2/	1,2,3	All		8	mA
		I_{OUT} = 0, Inhibit (pin 3) = open 2/		01 to 04		60	
				05 to 07		70	
Input undervoltage lockout (turn off when V_{In} decreasing)	UVLO	0% to 100 % load	1,2,3	All	14.6	15.9	V
		L, R 2/ 3/			14.0	16.5	
Input undervoltage release (turn off when V_{In} rising)	UVR	0% to 100 % load	1,2,3	All	16.6	17.3	V
		L, R 2/ 3/			15.5	17.9	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +85°C$ V_{IN} = +28 V dc ± 5% Full Load, C_L = 0 unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input under voltage hysteresis	UVR-UVLO	0% to 100 % load	1,2,3	All	1.0	3.0	V
Input current telemetry ratio	I_{CT}	100% load	1,2,3	All	1.42	1.56	V/A
		L, R 2/ 3/			1.4	1.6	
Switching Frequency	F_S		1,2,3	All	465	525	kHz
		L, R 2/ 3/			425	575	
Overvoltage protection Output voltage threshold	OVP	0% load to 100% load	1,2,3	All	117	123	mV
		L, R 2/ 3/			115	125	
Enable input (inhibit function) open circuit voltage drive 7/				All	3.0	6.0	V
Enable input (inhibit function) drive current (sink) 7/				All		100	µA
Enable input (inhibit function) voltage range 7/ 8/				All	-0.5	50	V
Efficiency 6/	Eff	I_{OUT} = 100% load 2/	1,2,3	01	60		%
				02	63		
				03	67		
				04	71		
				05, 06,07	77		
Isolation 6/	ISO	100 V dc, T_C = +25°C 2/	1	All	20		MΩ
Capacitive Load 7/ 9/	C_L	No effect on DC performance, T_C = +25°C		01, 02, 03		2500	µF
				04		2200	
				05		1000	
				06		180	
				07		120	
Short Circuit Power Dissipation 6/	P_D	Short Circuit 2/	1,2,3	All		16	W
Overload current limit point 10/	I_{LIM}	V_{OUT} = 90% of nominal 2/	1,2,3	All	105	145	%

See footnotes at end of table.

TABLE IA. Electrical performance characteristic – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +85°C$ V_{IN} = +28 V dc ± 5% Full Load, C_L = 0 unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Overload power dissipation 6/	P_D	V_{OUT} = 90% of nominal 2/	1,2,3	All	10.5	16	W
Line Rejection 7/	REJ	T_C = +25°C 100% load, dc to 50 kHz		All	50		dB
		L, R 2/ 3/		All	40		
V_{OUT} Step Load Transient 11/	V_{TLOAD}	50% load to 100% load V_{IN} = 28 V dc	4,5,6	01,02, 03		600	mV pk
				04		250	
		L, R 2/ 3/			-300	300	
				05		230	
				06		210	
				07		200	
V_{OUT} Step Load Transient Recovery 11/ 12/	TT_{LOAD}	50% Load to 100% Load V_{IN} = 28 V dc	4,5,6	All		150	µs
		L, R 2/ 3/				200	
V_{OUT} Step Line Transient 7/ 13/	V_{TLINE}	V_{IN} = 18 V dc to 40 V dc		All		300	mV pk
V_{OUT} Step Line Transient Recovery 7/ 12/ 13/	TT_{LINE}	V_{IN} = 18 V dc to 40 V dc		All		200	µs
Turn on overshoot	$Vton_{OS}$	10% load, full load	4,5,6	All		50	mV pk
Turn on delay 14/	Ton_D	10% load, full load	4,5,6	All		10	ms
		L, R 2/ 3/				12	

1/ Post irradiation testing shall be in accordance with 4.3.5 and table IA herein.
2/ A representative device has been tested using Condition A (50-300 rad(Si)/s) of Method 1019 to 150 krad(Si) for these parameters to ensure Radiation Hardness Assurance designator levels R and L. A representative device will be re-tested after design or process changes that may affect the RHA response of these devices.
3/ End of Life (EOL) Performance guaranteed to meet stated limits by worst-case analysis, which includes radiation, temperature, and aging effects.
4/ Parameter verified during line and load regulation tests.
5/ Percent of nominal output voltage.
6/ This parameter is not included in the worst-case analysis. The end-of-life tolerances are supported by post-irradiation and life test data.
7/ Parameter shall be tested as part of device characterization and after design and process changes. Thereafter, parameters shall be guaranteed to the limits specified in table IA.
8/ Enable input function is compatible with relay interface or open collector as determined in worst-case analysis.
9/ Capacitive load may be any value from 0 to the maximum limit without compromising DC performance.

TABLE IA. Electrical performance characteristic – Continued.

10/ Current limit point is defined as the output current, relative to full rated load, such that Vout = 90% of the nominal output voltage.
11/ Load step transition time ≥ 10 µs.
12/ Recovery time is measured from the initiation of the transient to where V_{OUT} has returned within ±1 percent of its steady state value.
13/ Line step transition time ≥ 100 µs.
14/ Turn on delay time from either a step application of input power or a logic low to a logic high transition on the inhibit pin (Pin 3) to the point where V_{OUT} = 90% of nominal.

TABLE IB. SEP test limits. 1/

Device types	SEP	Temperature (T_C)	Conditions/Results	Effective linear energy transfer (LET)
All	SEU (SET)	+25°C	The largest transients on all models are 100 mV or 3.3% of the nominal output voltage whichever is the greater. With a duration of less than 200 µs.	≤ 82 MeV-cm^2/mg
All	SEFI Shutdowns	+25°C	None	≤ 82 MeV-cm^2/mg
All	SEL	+25°C	None	≤ 82 MeV-cm^2/mg
All	SEB	+25°C	None	≤ 82 MeV-cm^2/mg
All	SEGR	+25°C	None	≤ 82 MeV-cm^2/mg

1/ For SEP test conditions, see 4.3.5.1.1.3 herein.

Case outline X.

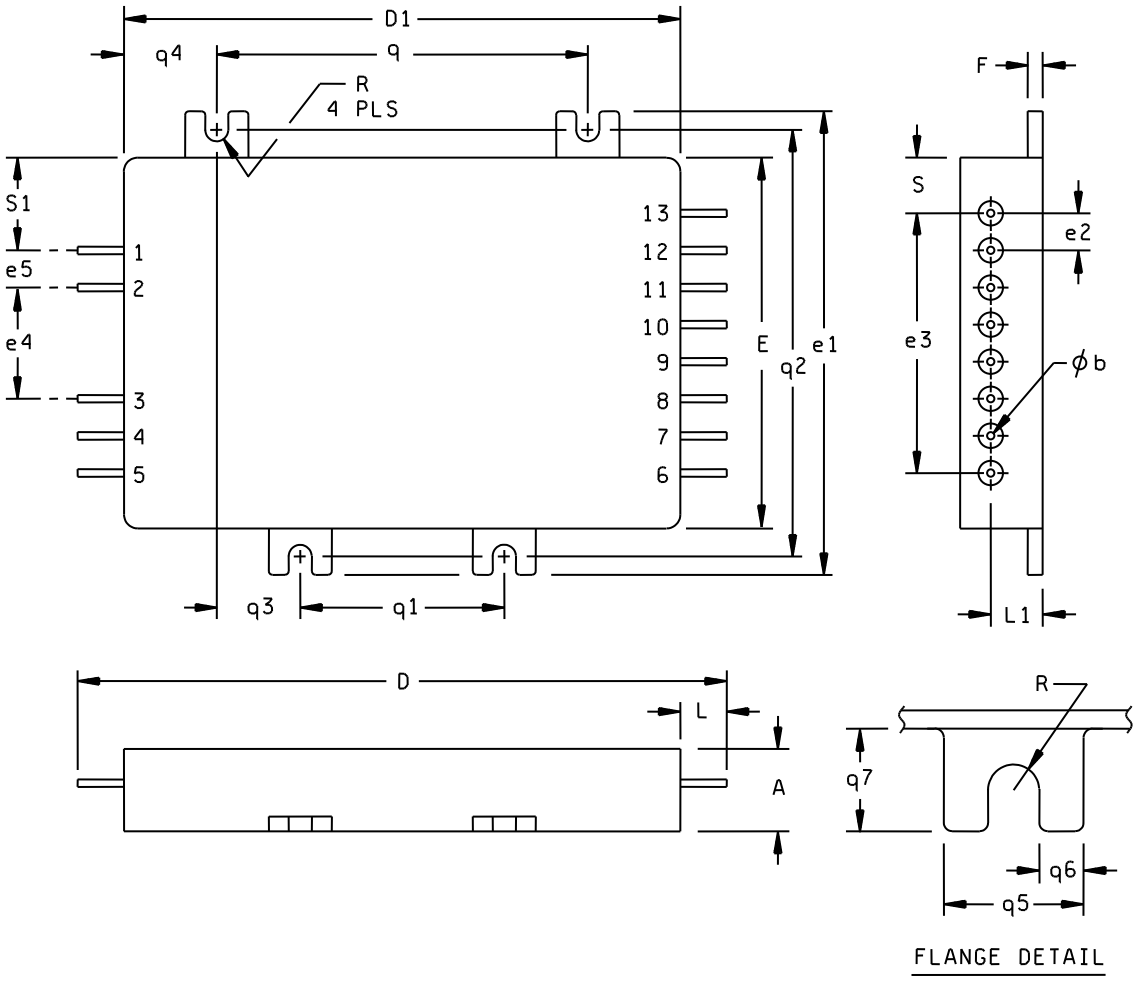


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-15224
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Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		12.07		.475
D	88.90 REF		3.50 REF	
D1		77.85		3.065
E		52.20		2.055
e1	63.37	63.63	2.495	2.505
e2/e5	5.05	5.33	.190	.210
e3	35.56 REF		1.400 REF	
e4	14.99	15.49	.590	.610
F		2.03		.080
L/q7	6.1	6.6	.24	.26
L1	6.48	6.73	.255	.265
q	50.55	55.05	1.99	2.01
q1	27.69	28.19	1.09	1.11
q2	58.17	58.67	2.29	2.31
q3	11.18	11.68	.44	.46
q4	12.57	12.83	.495	.505
q5	9.91	10.41	.39	.41
q6	3.30	3.81	.13	.15
R		1.588		.0625
S	7.37	7.87	.290	.310
S1	12.45	12.95	.49	.51
∅b	0.89	1.14	.035	.045

NOTES:
1. The U.S. government preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Lead identification for reference only.
3. Case outline weight: 125 grams maximum.

FIGURE 1. Case outline - Continued.

Device type	All
Case outline	X
Terminal number	Terminal symbol
1	+V input
2	Input return
3	Inhibit
4	Inhibit return
5	Undervoltage latch
6	Case ground
7	Input current telemetry
8	Output adjust
9	- Sense
10	+ Sense
11	OVP adjust
12	Output return
13	+ Output voltage

FIGURE 2. Terminal connections.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1, 4
Final electrical parameters	1*, 2, 3, 4, 5, 6
Group A test requirements	1, 2, 3, 4, 5, 6
Group C end-point electrical parameters	1, 2, 3, 4, 5, 6
End-point electrical parameters for radiation hardness assurance (RHA) devices	1, 2, 3, 4, 5, 6

* PDA applies to subgroup 1.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8, 9, 10, and 11 shall be omitted.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_C as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5. Radiation hardness assurance (RHA). RHA qualification is required only for those devices with the RHA designator as specified herein. See table IIIA and IIIB.

Table IIIA. Radiation Hardness Assurance Methods Table.

RHA method employed	**Active elements tested only as part of the hybrid device.**	**Tested**		**Worst Case Analysis** Performed using extreme value analysis				**End points after final dose**	
		Element Level	Hybrid Device Level	Includes temperature effects	Combines temperature and radiation effects	Combines total dose and displacement effects	End-of-life	Element Level	Hybrid device level
	No	Tested 1X	Tested at 1.5X the specified TID rating	Yes	No	Yes	1/ Yes	T_C = +25ºC	T_C = -55ºC +25ºC and 85ºC

1/ Worst case analysis performed with case temperature from -55ºC to 85ºC.

Table IIIB. Hybrid level and element level test table..

Radiation Test		Total Dose			Heavy Ion	Proton/Neutron
		Low Dose Rate	High Dose Rate (HDR)	ELDRS Characterization	SEP	Displacement Damage (DD)
Hybrid Level Testing		Not Tested	Tested (150 krad(Si))	Not performed	Tested (82 MeV-cm^2/mg)	Not Tested
Element Level Testing 1/	**CMOS Microcircuits**	Not tested	Tested to 1.5X the level specified	Not performed	Not Tested	Tested ($1x10^{12}$ n/cm^2)
	CMOS discrete (Power MOSFET)	Not tested	Tested to 1.5X the level specified	Not performed	Tested (82 MeV-cm^2/mg)	Not Tested
	Bipolar Discrete Semiconductors	Not tested	Tested to 1X the level specified	Not performed	Tested (hybrid level)	Tested ($1x10^{12}$ n/cm^2)
	Bipolar/BiCMOS Linear or Mixed Signal	Not tested	Tested to 1X the level specified	Not performed	Tested (hybrid level)	Tested ($1x10^{12}$ n/cm^2)

1/ The device manufacturer either performs the element level testing, or purchases QML elements with documentation indicating the manufacturer has already performed the testing. See paragraphs 4.3.5.1.2.2 a. and 4.3.5.2.1 a.

4.3.5.1 Radiation Hardness Assurance (RHA) inspection. RHA qualification is required for those devices with the RHA designator as specified herein. End-point electrical parameters for radiation hardness assurance (RHA) devices shall be specified in table IA. Radiation testing will be in accordance with the qualifying activity (DLA Land and Maritime-VQ) approved plan and with MIL-PRF-38534, Appendix G.

a. The hybrid device manufacturer shall establish procedures controlling element radiation testing, and shall establish radiation test plans used to implement element lot qualification during procurement. Test plans and test reports shall be filed and controlled in accordance with the manufacturer's configuration management system.

b. The hybrid device manufacturer shall designate a RHA program manager to oversee element lot qualification, and to monitor design changes for continued compliance to RHA requirements.

4.3.5.1.1 Hybrid level radiation qualification.

4.3.5.1.1.1 Qualification by similarity. A family is defined by the family model designator e.g. LSO single. All parts with this designator share a common design and use the same active elements with the exception of the output Schottky rectifiers. The LSO single1.5 V (device type 01), 1.8 V (device type 02), 2.5 (device type 03), 3.3 V (device type 04), 5 V (device type 05), 12 V (device type 06) and 15 V (device type 07) per this SMD are considered similar for the purpose of radiation testing. Device type 5962R1522404KXA (3.3 V) was tested for TID and SEP. Device types 5962R1522405KXA (5 V) and 5962R1522407KXA (15 V) were tested for SEP and all other devices on this SMD are RHA qualified by similarity.

4.3.5.1.1.2 Total ionizing dose irradiation testing. A minimum representative device of the hybrid family (family model designator, e.g. LSO single) is characterized and tested initially and after any design or process changes which may affect the RHA response of the device type. Devices are tested at High Dose Rate (HDR) in accordance with condition A of method 1019 of MIL-STD-883 to 150 krads(Si). The minimum sample size is two biased devices. Test results are compared to the limits specified in table IA after anneal at 100°C for 160 hours at nominal input voltage and full load.

4.3.5.1.1.3 Single event phenomena (SEP). Representative devices 04 (3.3 V), 05 (5 V), and 07 (15 V) have been characterized for SEP response at initial qualification in accordance with ASTM F1192 and will be retested after any design or process changes which may affect the RHA response. Test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be normal to the die surface. No shadowing of the ion beam due to fixturing is allowed.

b. The fluence shall be $\geq 1x10^7$ particles/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s.

d. The particle range shall be $\geq$ 50 micron in silicon.

e. The initial characterization is performed at minimum, nominal and maximum input voltage, and with both minimum and maximum load. For future qualification the characterization will be performed only at worst case condition, maximum input voltage and maximum load. The test temperature shall be +25ºC ±10 ºC in air.

f. For SEP test limits, see table IB herein.

4.3.5.1.2 Element level radiation qualification

4.3.5.1.2.1 Technologies not being tested. Testing is not performed on device technologies including: Junction Diodes, Schottky diodes, and zener diodes the manufacturer has determined to be radiation hardened.

4.3.5.1.2.2 Total Ionizing Dose Irradiation. The manufacturer employs two methods of addressing TID.

a. RHA QML die.

1. Active Elements are purchased as level L or R (as required by the device RHA designator) per MIL-PRF-38535 Standard Microcircuit Drawing (SMD) or MIL-PRF-19500 JAN specification sheet with electrical performance characteristics established for the elements at hybrid device design.

b. Non RHA QML die. (including QML not-RHA die or die bought to a lower RLAT level than required by the hybrid device).

1. Bipolar discrete devices - Ten biased samples from each initial wafer lot of active elements, except as noted in 4.3.5.1.2.1 will be characterized and tested at HDR in accordance with condition A of method 1019 of MIL-STD-750 to 100 krads(Si). Element parametric degradation test results are analyzed using 0.9900/90% statistics and compared to limits established for the elements at hybrid device design.

2. Bipolar/BiCMOS linear – Ten biased samples from each initial wafer lot of microcircuit elements, except as noted in 4.3.5.1.2.1, will be characterized and tested at HDR in accordance with condition A of method 1019 of MIL-STD-883 to 100 krads(Si). Bipolar microcircuits are evaluated for ELDRS and tested accordingly. All MOS elements are subjected to 168 hours of accelerated anneal at 100ºC. Element parametric degradation test results are analyzed using 0.9900/90% statistics and compared to limits established for the elements at hybrid device design.

4.3.5.1.3 Neutron Irradiation. The manufacturer employs two methods of addressing displacement damage due to neutron irradiation

a. All samples of CMOS, bipolar discrete, bipolar, BiCMOS, and linear or mixed signal integrated circuits described in 4.3.5.1.2.2 shall be tested to a minimum average integrated neutron fluence (1 MeV equivalent of $1x10^{12}$ n/cm^2) in accordance with method 1017 of MIL-STD-883 prior to TID testing. 0.9900/90% statistics are applied to the element parameter degradations which are compared to limits established for the element at hybrid device design

4.3.5.2 Radiation lot Acceptance. Each wafer lot of non-RHA QML active elements shall be evaluated for acceptance in accordance with MIL-PRF-38534 and herein except as noted in 4.3.5.1.2.1.

4.3.5.2.1 Total Ionizing Dose Irradiation. The manufacturer employs two methods of addressing TID.

a. RHA QML die.

1. Active Elements are purchased at the RLAT level (L or R) required by the hybrid device to a MIL-PRF-38535 (SMD) Standard Microcircuit Drawing or MIL-PRF-19500 JAN specification sheet with electrical performance characteristics established for the element at hybrid device design.

b. Non RHA QML die.

2 . Non RHA QML die (including QML not-RHA die or die bought to a lower RLAT level than required by the hybrid device). shall be tested as follows: Ten biased and two control samples from each wafer lot of active elements, except as noted in 4.3.5.1.2.1, will be characterized and tested at HDR in accordance with condition A of method 1019 of MIL-STD-883. The samples will be tested to 1X the rated value of the device (1.5X for MOS technology devices) for which it is purchased (R or L). 0.9900/90% statistics are applied to the element parametric degradations which are compared against limits established for the element at hybrid device design.

4.3.5.2.2 Neutron Irradiation. Every wafer lot of bipolar linear or mixed signal integrated circuit and semiconductor elements, except those purchased as RHA QML die will be tested to a minimum average integrated neutron fluence (1 MeV Si equivalent) of 1×10^{12} n/cm^2, in accordance with method 1017 of MIL-STD-883 using a minimum sample size of 10 samples. 0.9900/90% statistics are applied to the element parameter degradations which are compared to limits established for the elements at hybrid device design.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Post Office Box 3990, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Occurrence of latchup (SEL).

d Occurrence of Burn-out (SEB).

e. Occurrence of Gate Rupture (SEGR).

f. Occurrence of Single Event Functional Interrupt (SEFI).

g Occurrence of Single Event Upset (SEU).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-11-02

Approved sources of supply for SMD 5962-15224 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-1522401KXA	52467	LSO2801R5S
5962-1522401KXC	52467	LSO2801R5S
5962L1522401KXA	52467	LSO2801R5S
5962L1522401KXC	52467	LSO2801R5S
5962R1522401KXA	52467	LSO2801R5S
5962R1522401KXC	52467	LSO2801R5S
5962-1522402KXA	52467	LSO2801R8S
5962-1522402KXC	52467	LSO2801R8S
5962L1522402KXA	52467	LSO2801R8S
5962L1522402KXC	52467	LSO2801R8S
5962R1522402KXA	52467	LSO2801R8S
5962R1522402KXC	52467	LSO2801R8S
5962-1522403KXA	52467	LSO2802R5S
5962-1522403KXC	52467	LSO2802R5S
5962L1522403KXA	52467	LSO2802R5S
5962L1522403KXC	52467	LSO2802R5S
5962R1522403KXA	52467	LSO2802R5S
5962R1522403KXC	52467	LSO2802R5S
5962-1522404KXA	52467	LSO2803R3S
5962-1522404KXC	52467	LSO2803R3S
5962L1522404KXA	52467	LSO2803R3S
5962L1522404KXC	52467	LSO2803R3S
5962R1522404KXA	52467	LSO2803R3S
5962R1522404KXC	52467	LSO2803R3S
5962-1522405KXA	52467	LSO2805S
5962-1522405KXC	52467	LSO2805S
5962L1522405KXA	52467	LSO2805S
5962L1522405KXC	52467	LSO2805S
5962R1522405KXA	52467	LSO2805S
5962R1522405KXC	52467	LSO2805S
5962-1522406KXA	52467	LSO2812S
5962-1522406KXC	52467	LSO2812S
5962L1522406KXA	52467	LSO2812S
5962L1522406KXC	52467	LSO2812S
5962R1522406KXA	52467	LSO2812S
5962R1522406KXC	52467	LSO2812S

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-1522407KXA	52467	LSO2815S
5962-1522407KXC	52467	LSO2815S
5962L1522407KXA	52467	LSO2815S
5962L1522407KXC	52467	LSO2815S
5962R1522407KXA	52467	LSO2815S
5962R1522407KXC	52467	LSO2815S

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
52467	International Rectifier 2520 Junction Ave. San Jose, CA 95134

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.