



# STS1DN45K3

Dual N-channel 450 V, 3.2  $\Omega$ , 0.5 A SuperMESH3™  
Power MOSFET in SO-8

Preliminary data

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>	P <sub>w</sub>
STS1DN45K3	450 V	< 3.8 $\Omega$	0.5 A	1.7 W

- 100% avalanche tested
- Low input capacitances and gate charge
- Low gate input resistance

## Application

- Switching applications

## Description

SuperMESH3™ is a new Power MOSFET technology that is obtained via improvements applied to STMicroelectronics' SuperMESH™ technology combined with a new optimized vertical structure. The resulting product has an extremely low on resistance, superior dynamic performance and high avalanche capability, making it especially suitable for the most demanding applications.

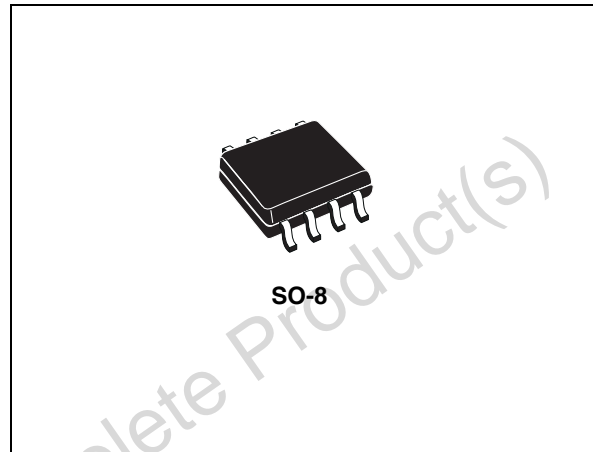


Figure 1. Internal schematic diagram

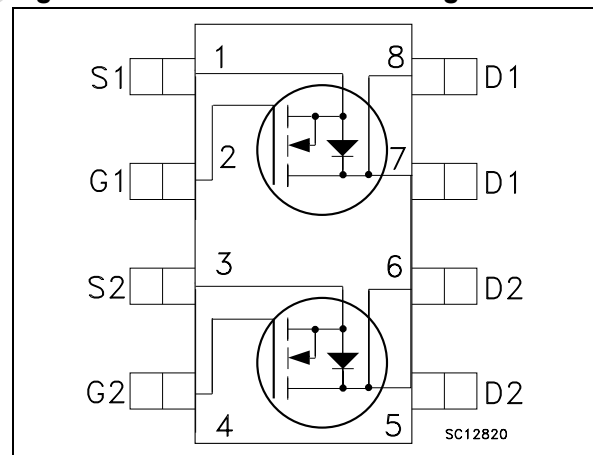


Table 1. Device summary

Order codes	Marking	Packages	Packaging
STS1DN45K3	11145	SO-8	Tape and reel

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Obsolete Product(s) - Obsolete Product(s)



# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	450	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	0.5	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	0.32	A
$I_{DM}^{(1)}$	Drain current (pulsed)	2	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ (dual operation)	1.7	W
	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ (single operation)	1.3	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	0.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	TBD	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	TBD	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 0.5\text{ A}$ ,  $di/dt \leq \text{TBD A}/\mu\text{s}$ ,  $V_{Peak} < V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb max (single operation)	62.5	$^\circ\text{C}/\text{W}$
	Thermal resistance junction-amb max (dual operation)	78	$^\circ\text{C}/\text{W}$

1. When mounted on FR4 board (steady state)

## 2 Electrical characteristics

( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	450			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125\text{ }^\circ\text{C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 0.5\text{ A}$		3.2	3.8	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	150	-	pF
$C_{oss}$	Output capacitance			30		pF
$C_{rss}$	Reverse transfer capacitance			6		pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }360\text{ V}$ , $V_{GS} = 0$	-	TBD	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			TBD		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	TBD	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 360\text{ V}$ , $I_D = 0.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 3</a> )	-	6	-	nC
$Q_{gs}$	Gate-source charge			TBD		nC
$Q_{gd}$	Gate-drain charge			TBD		nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 225\text{ V}$ , $I_D = 0.5\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <i>Figure 4</i> )	-	TBD	-	ns
$t_r$	Rise time			TBD		ns
$t_{d(off)}$	Turn-off-delay time			TBD		ns
$t_f$	Fall time			TBD		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		0.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 0.5\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 0.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see <i>Figure 7</i> )	-	TBD		ns
$Q_{rr}$	Reverse recovery charge			TBD		nC
$I_{RRM}$	Reverse recovery current			TBD		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 0.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <i>Figure 7</i> )	-	TBD		ns
$Q_{rr}$	Reverse recovery charge			TBD		nC
$I_{RRM}$	Reverse recovery current			TBD		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

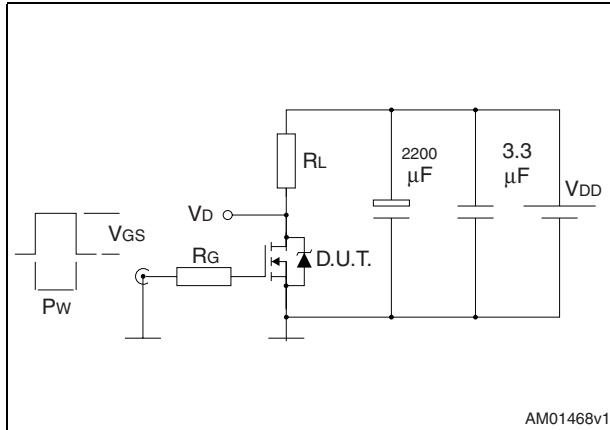
**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{gs} = \pm 1\text{ mA}$ (open drain)	30			V

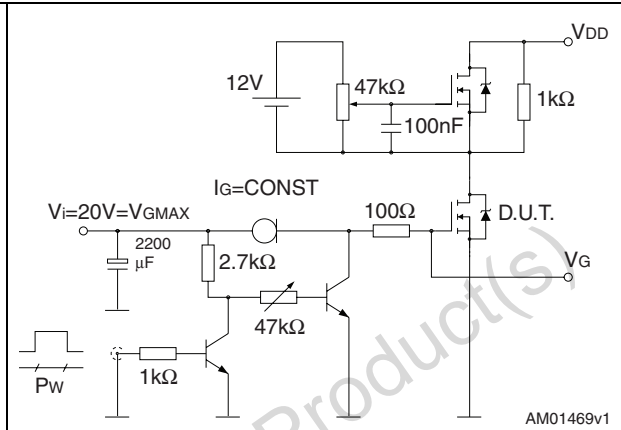
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

### 3 Test circuits

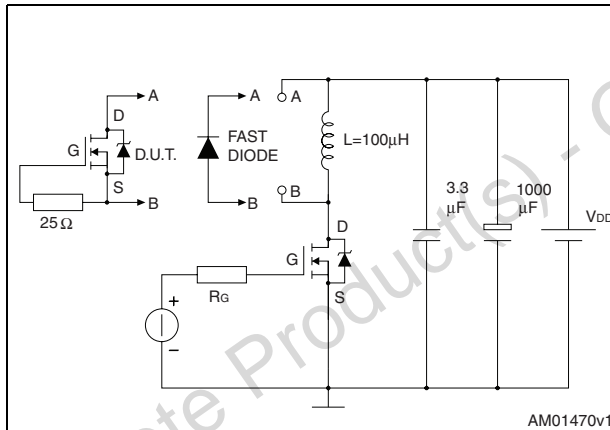
**Figure 2. Switching times test circuit for resistive load**



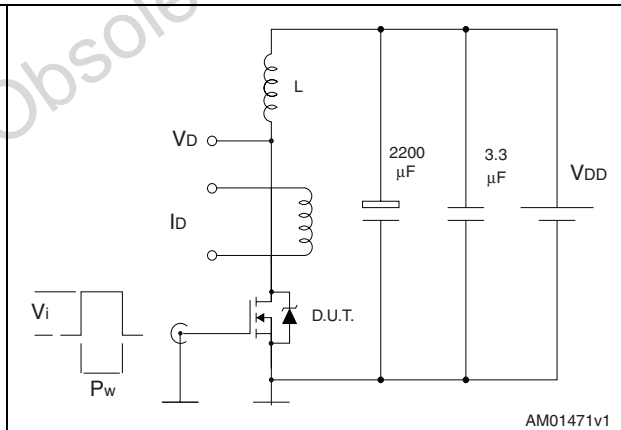
**Figure 3. Gate charge test circuit**



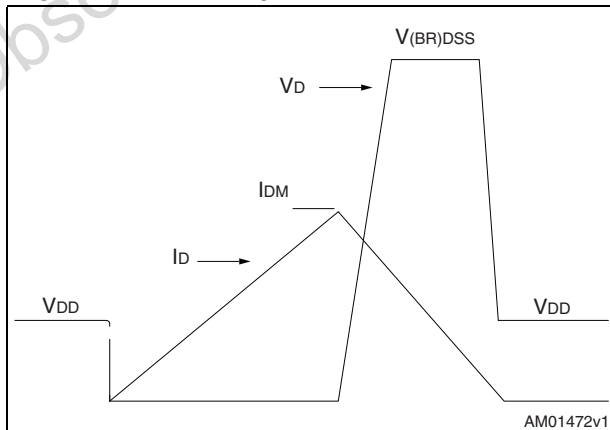
**Figure 4. Test circuit for inductive load switching and diode recovery times**



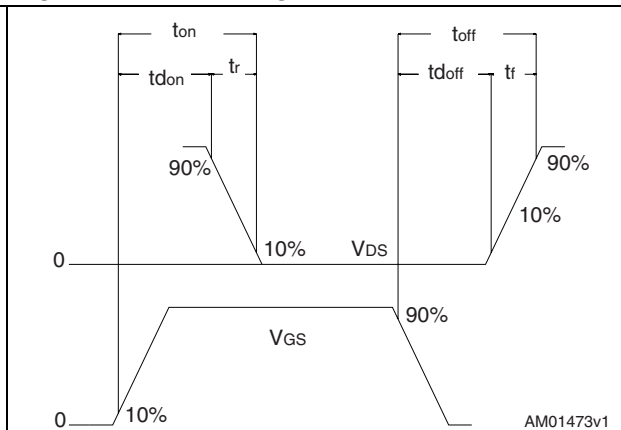
**Figure 5. Unclamped inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**



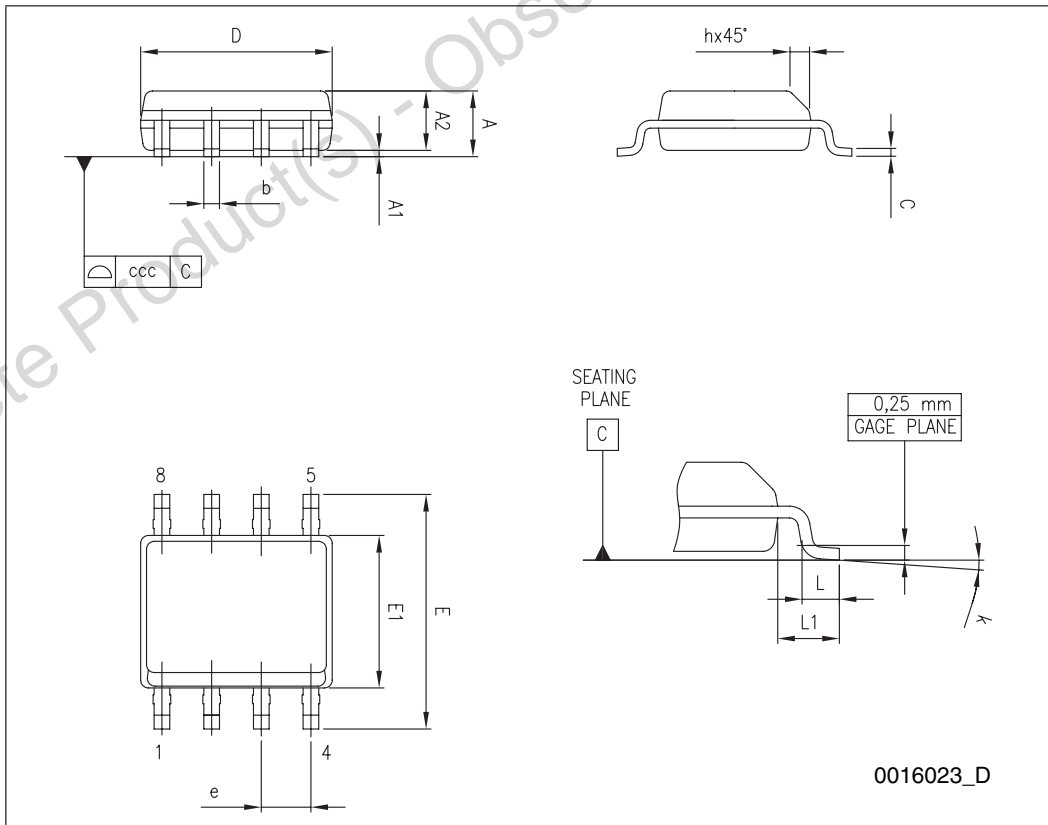
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Obsolete Product(s) - Obsolete Product(s)

**SO-8 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10





## 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
07-Apr-2010	1	First release

Obsolete Product(s) - Obsolete Product(s)

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