# Product Preview

# IGBT with Monolithic Free Wheeling Diode

This Insulated Gate Bipolar Transistor (IGBT) features a robust and cost effective ultra Field Stop (FS) Trench construction and provides superior performance. It is especially designed for low on–state and is well suited for resonant or soft switching topologies, such as those used in inductive heating applications. The device contains a reverse conducting diode integrated on the same die, which makes the device construction very cost effective.

#### **Features**

- Extremely Efficient Trench with ultra Fieldstop Technology
- 1400 V Breakdown Voltage
- Optimized for Low Losses in IH Cooker Application
- Reliable and Cost Effective Single Die Solution
- These are Pb–Free Devices

### **Typical Applications**

- Inductive Heating
- Consumer Appliances
- Soft Switching

### **ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector–emitter voltage @ T <sub>J</sub> = 25°C	V <sub>CES</sub>	1400	V
Collector current @ Tc = 25°C @ Tc = 100°C	lc	60 30	А
Pulsed collector current, $T_{pulse}$ limited by $T_{Jmax}$ 10 $\mu s$ pulse, $V_{GE}$ = 15 $V$	ІСМ	120	A
Diode forward current @ Tc = 25°C @ Tc = 100°C	I <sub>F</sub>	60 30	Α
Diode pulsed current, $T_{pulse}$ limited by $T_{Jmax}$ 10 $\mu s$ pulse, $V_{GE}$ = 0 $V$	I <sub>FM</sub>	120	Α
Gate-emitter voltage Transient Gate-emitter Voltage ( $T_{pulse} = 5 \mu s$ , D < 0.10)	V <sub>GE</sub>	±20 ±25	V
Power Dissipation @ Tc = 25°C @ Tc = 100°C	P <sub>D</sub>	357 178	W
Operating junction temperature range	$T_J$	-40 to +175	°C
Storage temperature range	T <sub>stg</sub>	-55 to +175	°C
Lead temperature for soldering, 1/8" from case for 5 seconds	T <sub>SLD</sub>	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

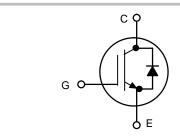
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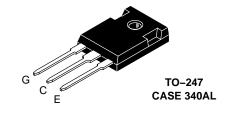


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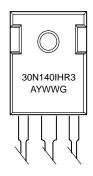
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30 A, 1400 V V<sub>CEsat</sub> = 1.8 V E<sub>off</sub> = 1.05 mJ





### **MARKING DIAGRAM**



A = Assembly Location

Y = Year WW = Work Week G = Pb-Free Package

#### **ORDERING INFORMATION**

Device	Package	Shipping
NGTB30N140IHR3WG	TO-247 (Pb-Free)	30 Units / Rail

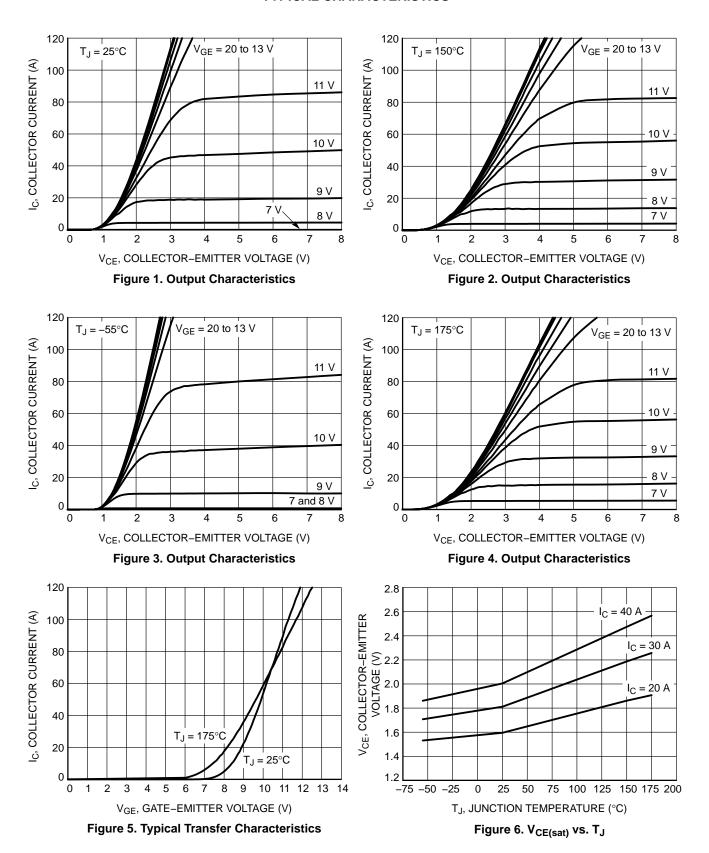
### THERMAL CHARACTERISTICS

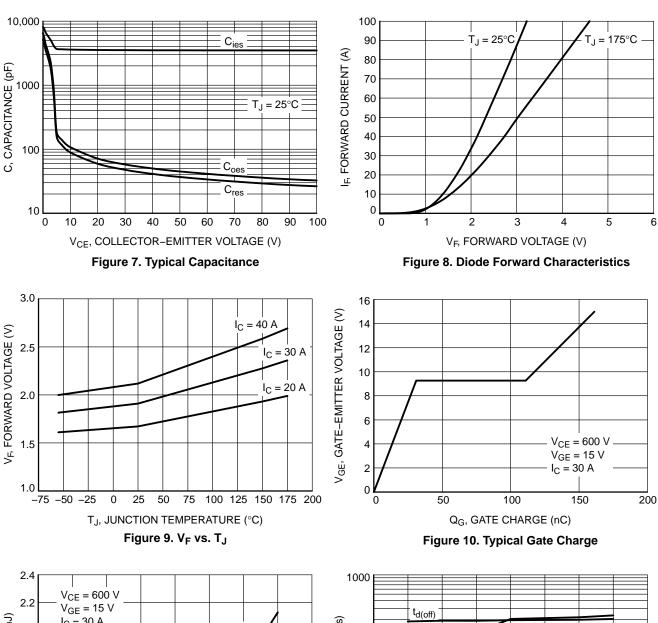
Rating	Symbol	Value	Unit
Thermal resistance junction-to-case	$R_{ heta JC}$	0.42	°C/W
Thermal resistance junction-to-ambient	$R_{ heta JA}$	40	°C/W

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Тур	Max	Unit
STATIC CHARACTERISTIC						
Collector–emitter breakdown voltage, gate–emitter short–circuited	$V_{GE} = 0 \text{ V}, I_{C} = 1 \text{ mA}$	V <sub>(BR)CES</sub>	1400	_	-	V
Collector-emitter saturation voltage	V <sub>GE</sub> = 15 V, I <sub>C</sub> = 30 A V <sub>GE</sub> = 15 V, I <sub>C</sub> = 30 A, T <sub>J</sub> = 175°C	V <sub>CEsat</sub>	- -	1.80 2.20	1.95 -	V
Gate-emitter threshold voltage	$V_{GE} = V_{CE}, I_{C} = 175 \mu A$	V <sub>GE(th)</sub>	4.5	5.7	6.5	V
Collector–emitter cut–off current, gate– emitter short–circuited	V <sub>GE</sub> = 0 V, V <sub>CE</sub> = 1400 V V <sub>GE</sub> = 0 V, V <sub>CE</sub> = 1400 V, T <sub>J =</sub> 175°C	I <sub>CES</sub>	- -	_ 210	20 -	μΑ
Gate leakage current, collector–emitter short–circuited	V <sub>GE</sub> = 20 V, V <sub>CE</sub> = 0 V	I <sub>GES</sub>	-	-	120	nA
DYNAMIC CHARACTERISTIC						
Input capacitance	V <sub>CE</sub> = 20 V, V <sub>GE</sub> = 0 V, f = 1 MHz	C <sub>ies</sub>	-	3505	-	pF
Output capacitance		C <sub>oes</sub>	-	70	-	
Reverse transfer capacitance		C <sub>res</sub>	-	58	-	
Gate charge total		$Q_g$	-	163	-	nC
Gate to emitter charge	$V_{CE} = 600 \text{ V}, I_{C} = 30 \text{ A}, V_{GE} = 15 \text{ V}$	Q <sub>ge</sub>	-	30	-	
Gate to collector charge		$Q_{gc}$	_	81	_	
SWITCHING CHARACTERISTIC, INDUCT	IVE LOAD					
Turn-off delay time	$T_J = 25^{\circ}C$ , $V_{CC} = 600 \text{ V}$ , $I_C = 30 \text{ A}$ , $R_g = 10 \Omega$ $V_{GE} = 15 \text{ V}$	t <sub>d(off)</sub>	-	197	-	ns
Fall time		t <sub>f</sub>	-	122	-	
Turn-off switching loss		E <sub>off</sub>	_	1.05	_	mJ
Turn-off delay time	$T_J = 150^{\circ}\text{C}, V_{CC} = 600 \text{ V},$ $I_C = 30 \text{ A}, R_g = 10 \Omega$ $V_{GE} = 15 \text{ V}$	t <sub>d(off)</sub>	_	209	_	ns
Fall time		t <sub>f</sub>	-	214	-	
Turn-off switching loss	V <sub>GE</sub> = 15 V	E <sub>off</sub>	-	1.75	-	mJ
DIODE CHARACTERISTIC						
Forward voltage	$V_{GE} = 0 \text{ V}, I_F = 30 \text{ A}$ $V_{GE} = 0 \text{ V}, I_F = 30 \text{ A}, T_J = 175^{\circ}\text{C}$	V <sub>F</sub>	_ _	1.90 2.48	2.10 -	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.





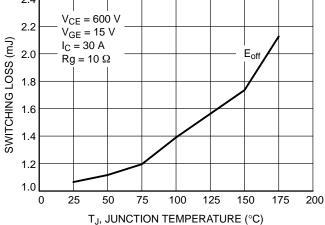


Figure 11. Switching Loss vs. Temperature

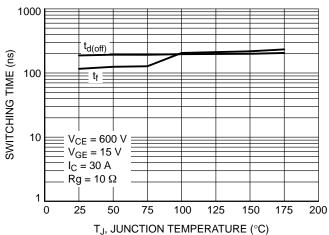


Figure 12. Switching Loss vs. Temperature

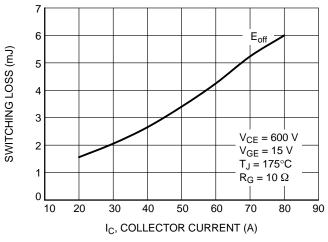


Figure 13. Switching Loss vs. I<sub>C</sub>

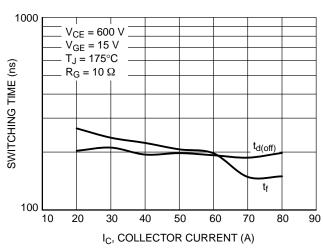


Figure 14. Switching Time vs. I<sub>C</sub>

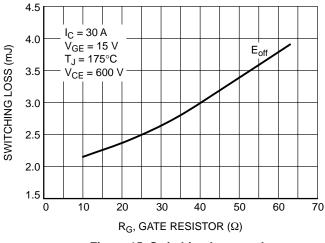


Figure 15. Switching Loss vs. I<sub>C</sub>

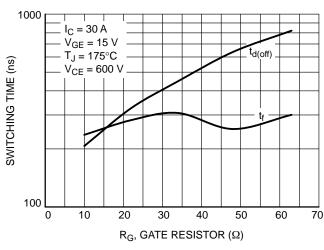


Figure 16. Switching Time vs. I<sub>C</sub>

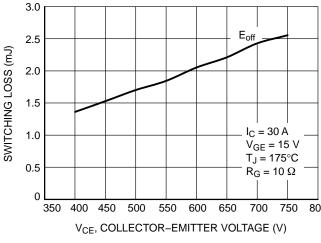


Figure 17. Switching Loss vs. I<sub>C</sub>

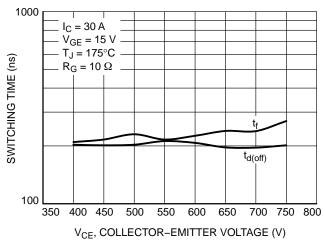


Figure 18. Switching Time vs. I<sub>C</sub>

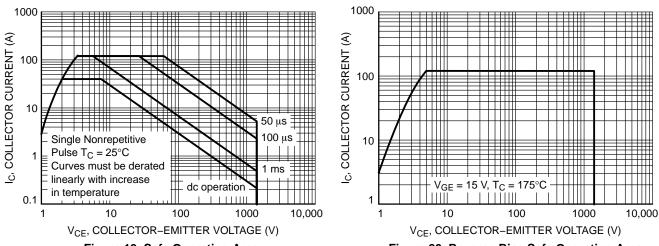


Figure 19. Safe Operating Area Figure 20. Reverse Bias Safe Operating Area

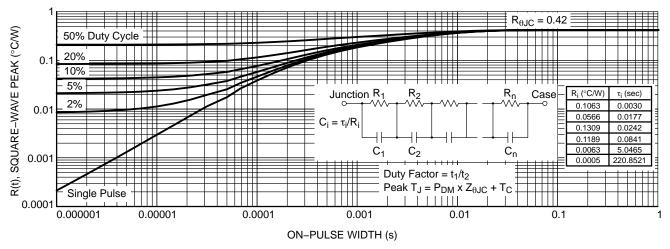


Figure 21. IGBT Transient Thermal Impedance

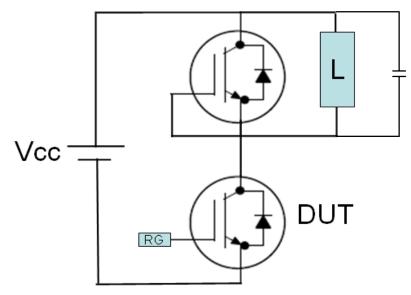


Figure 22. Test Circuit for Switching Characteristics

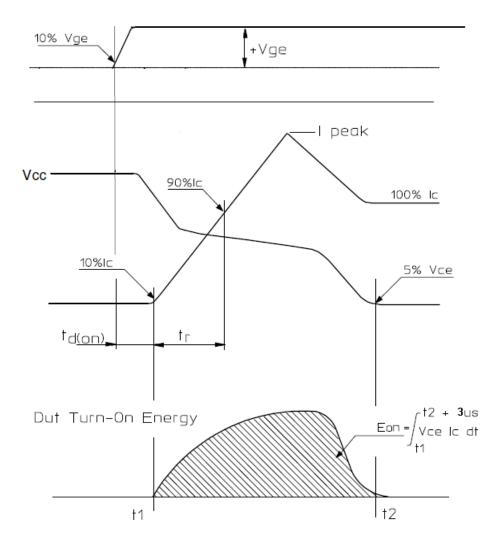


Figure 23. Definition of Turn On Waveform

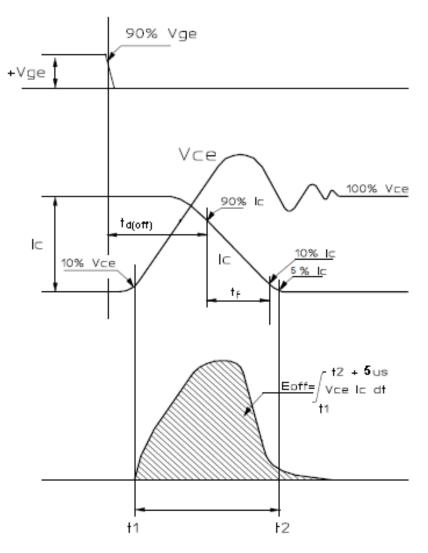
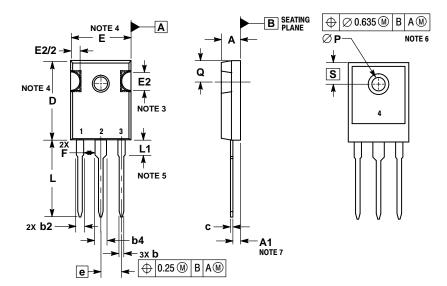


Figure 24. Definition of Turn Off Waveform

#### PACKAGE DIMENSIONS

TO-247 CASE 340AL ISSUE D



- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

- DIMENSIONING AND TOLEHANCING PEH ASME Y14.5M, 18 CONTROLLING DIMENSION: MILLIMETERS. SLOT REQUIRED, NOTCH MAY BE ROUNDED. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
- LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY
- ØP SHALL HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM DIAMETER OF 3.91. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED

	MILLIMETERS		
DIM	MIN	MAX	
Α	4.70	5.30	
A1	2.20	2.60	
b	1.07	1.33	
b2	1.65	2.35	
b4	2.60	3.40	
С	0.45	0.68	
D	20.80	21.34	
E	15.50	16.25	
E2	4.32	5.49	
е	5.45 BSC		
F	2.655		
L	19.80	20.80	
L1	3.81	4.32	
P	3.55	3.65	
Q	5.40	6.20	
S	6.15 BSC		

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