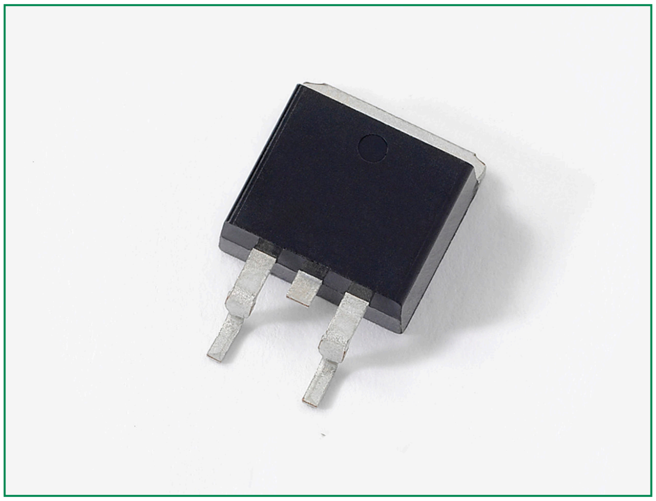
NGD8201AN - 20 A, 400 V, N-Channel Ignition IGBT, DPAK



20 Amps, 400 Volts
V_{CE}(on) ≤ 1.3 V @
I_C = 10 A, V_{GE} ≥ 4.5 V

Maximum Ratings (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	440	V
Gate–Gate Voltage	V_{CES}	440	V
Gate–Emitter Voltage	V_{GE}	± 15	V
Collector Current–Continuous @ T_C = 25°C – Pulsed	I_C	20 50	A_{DC} A_{AC}
Continous Gate Current	I_G	1.0	mA
Transient Gate Current (t ≤ 2 ms, f ≤ 100 Hz)	I_G	20	mA
ESD (Charged–Device Model)	ESD	2.0	kV
ESD (Human Body Model) R = 1500 Ω, C = 100 pF	ESD	2.0	kV
ESD (Machine Model) R = 0 Ω, C = 200 pF	ESD	500	V
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.83	W W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to +175	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

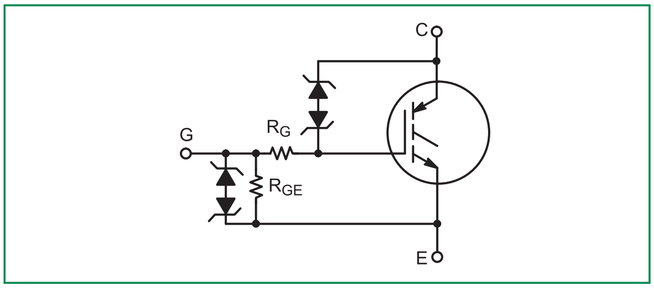
Description

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over–Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

Features

- Ideal for Coil–on–Plug and Driver–on–Coil Applications
- DPAK Package Offers Smaller Footprint for Increased Board Space
- Gate–Emitter ESD Protection
- Temperature Compensated Gate–Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- New Design Increases Unclamped Inductive Switching (UIS) Energy Per Area
- Low Threshold Voltage for Interfacing Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Emitter Ballasting for Short–Circuit Capability
- These are Pb–Free Devices

Functional Diagram



Additional Information

Datasheet | Resources | Samples

Unclamped Collector–To–Emitter Avalanche Characteristics

	Symbol	Value	Unit
Single Pulse Collector–to–Emitter Avalanche Energy			
V_{CC} = 50 V, V_{GE} = 5.0 V, P_k I_L = 16.7 A, R_G = 1000 Ω , L = 1.8 mH, Starting T_J = 25°C	E_{AS}	250	mJ
V_{CC} = 50 V, V_{GE} = 5.0 V, P_k I_L = 14.9 A, R_G = 1000 Ω , L = 3.0 mH, Starting T_J = 150°C		200	
V_{CC} = 50 V, V_{GE} = 5.0 V, P_k I_L = 14.1 A, R_G = 1000 Ω , L = 1.8 mH, Starting T_J = 175°C		180	
Reverse Avalanche Energy			
V_{CC} = 100 V, V_{GE} = 20 V, P_k I_L = 25.8 A, L = 6.0 mH, Starting T_J = 25°C	$E_{AS(R)}$	2000	mJ

Thermal Characteristics

	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.3	°C/W
Thermal Resistance, Junction to Ambient DPAK (Note 1)	$R_{\theta JA}$	95	
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 5 seconds	T_L	275	°C

1. When surface mounted to an FR4 board using the minimum recommended pad size.

Electrical Characteristics - OFF

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Collector–Emitter Clamp Voltage	B_{VCES}	I_C = 2.0 mA	T_J = –40°C to 175°C	370	395	420	V
		I_C = 10 mA	T_J = –40°C to 175°C	390	415	440	
Zero Gate Voltage Collector Current	I_{CES}	V_{CE} = 15 V, V_{GE} = 0 V	T_J = 25°C	–	0.1	1.0	μA
		V_{CE} = 200 V, V_{GE} = 0 V	T_J = 25°C	0.5	1.5	10	
			T_J = 175°C	1.0	25	100*	
			T_J = –40°C	0.4	0.8	5.0	
Reverse Collector–Emitter Clamp Voltage	$B_{VCES(R)}$	I_C = -75 mA	T_J = 25°C	30	35	39	V
			T_J = 175°C	35	39	45*	
			T_J = –40°C	30	33	37	
Reverse Collector–Emitter Leakage Current	$I_{CES(R)}$	V_{CE} = –24 V	T_J = 25°C	0.05	0.2	1.0	mA
			T_J = 175°C	1.0	8.5	25	
			T_J = –40°C	0.005	0.025	0.2	
Gate–Emitter Clamp Voltage	BV_{GES}	I_G = ± 5.0 mA	T_J = –40°C to 175°C	12	12.5	14	V
Gate–Emitter Leakage Current	I_{GES}	V_{GE} = ± 5.0 V	T_J = –40°C to 175°C	200	300	350*	μA
Gate Resistor	R_G	–	T_J = –40°C to 175°C	–	70	–	Ω
Gate–Emitter Resistor	R_{GE}	–	T_J = –40°C to 175°C	14.25	16	25	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Maximum Value of Characteristic across Temperature Range.

Electrical Characteristics - ON (Note 3)

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Gate Threshold Voltage	$V_{GE\ (th)}$	I_C = 1.0 mA, $V_{GE} = V_{CE}$	T_J = 25°C	1.5	1.8	2.1	V
			T_J = 175°C	0.7	1.0	1.3	
			T_J = −40°C	1.7	2.0	2.3*	
Threshold Temperature Coefficient (Negative)	–	–	–	4.0	4.6	5.2	mV/°C
Collector–to–Emitter On–Voltage	$V_{CE\ (on)}$	I_C = 6.5 A, V_{GE} = 3.7 V	T_J = 25°C	0.85	1.03	1.35	V
			T_J = 175°C	0.7	0.9	1.15	
			T_J = −40°C	0.09	1.11	1.4	
		I_C =9.0 A, V_{GE} = 3.9 V	T_J = 25°C	0.9	1.11	1.45	
			T_J = 175°C	0.8	1.01	1.25	
			T_J = −40°C	1.0	1.18	1.5	
		I_C = 7.5 A, V_{GE} = 4.5 V	T_J = 25°C	0.85	1.15	1.4	
			T_J = 175°C	0.7	0.95	1.2	
			T_J = −40°C	1.0	1.3	1.6*	
		I_C = 10 A, V_{GE} = 4.5 V	T_J = 25°C	1.0	1.3	1.6	
			T_J = 175°C	0.8	1.05	1.4	
			T_J = −40°C	1.1	1.4	1.7*	
		I_C = 15 A, V_{GE} = 4.5 V	T_J = 25°C	1.15	1.45	1.7	
			T_J = 175°C	1.0	1.3	1.55	
			T_J = −40°C	1.25	1.55	1.8*	
		I_C = 20 A, V_{GE} = 4.5 V	T_J = 25°C	1.1	1.4	1.9	
			T_J = 175°C	1.2	1.5	1.8	
			T_J = −40°C	1.3	1.42	2.0	
Forward Transconductance	gfs	I_C = 6.0 A, V_{CE} = 5.0 V	T_J = 25°C	10	18	25	Mhos

*Maximum Value of Characteristic across Temperature Range.
3. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

Dynamic Characteristics

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Input Capacitance	C_{ISS}	f = 10 kHz V_{CC} = 25 V	T_J = -40°C to 175°C	1100	1300	1500	pF
Output Capacitance	C_{OSS}			70	80	90	
Transfer Capacitance	C_{RSS}			18	20	22	

Switching Characteristics

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Turn–Off Delay Time (Resistive)	$t_{d\ (off)}$	V_{CC} = 300 V I_C = 9.0 A R_G = 1.0 kΩ R_L = 33 Ω V_{GE} = 5.0 V	T_J = 25°C	6.0	8.0	10	µSec
			T_J = 175°C	6.0	8.0	10	
Fall Time (Resistive)	t_f		T_J = 25°C	4.0	6.0	8.0	
			T_J = 175°C	8.0	10.5	14	
Turn–Off Delay Time (Inductive)	$t_{d\ (off)}$	V_{CC} = 300 V I_C = 9.0 A R_G = 1.0 kΩ L = 300 µH V_{GE} = 5.0 V	T_J = 25°C	3.0	5.0	7.0	
			T_J = 175°C	5.0	7.0	9.0	
Fall Time (Inductive)	t_f		T_J = 25°C	1.5	3.0	4.5	
			T_J = 175°C	5.0	7.0	10	
Turn–On Delay Time	$t_{d\ (on)}$	V_{CC} = 14 V I_C = 9.0 A R_G = 1.0 kΩ R_L = 1.5 Ω V_{GE} = 5.0 V	T_J = 25°C	1.0	1.5	2.0	
			T_J = 175°C	1.0	1.5	2.0	
Rise Time	t_r		T_J = 25°C	4.0	6.0	8.0	
			T_J = 175°C	3.0	5.0	7.0	

Typical Electrical Characteristics

Figure 1. Self Clamped Inductive Switching

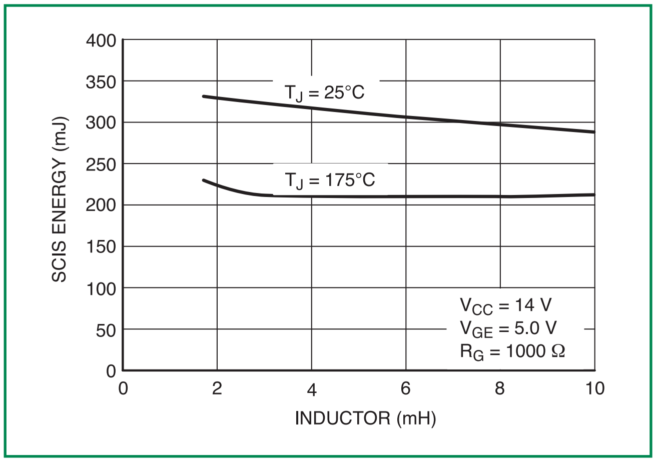


Figure 2. Open Secondary Avalanche Current vs. Temperature

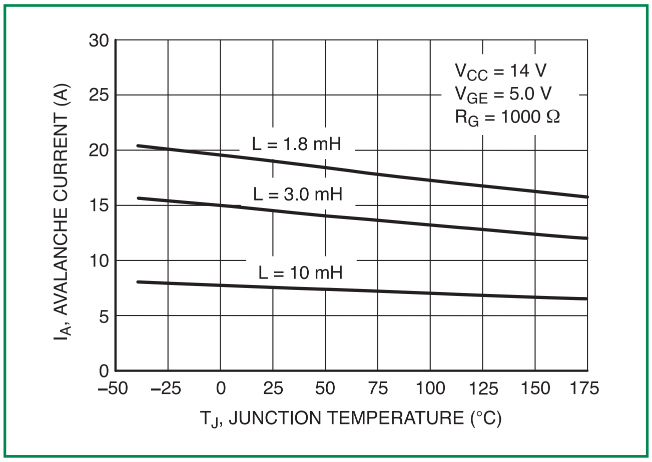


Figure 3. Collector–to–Emitter Voltage vs. Junction Temperature

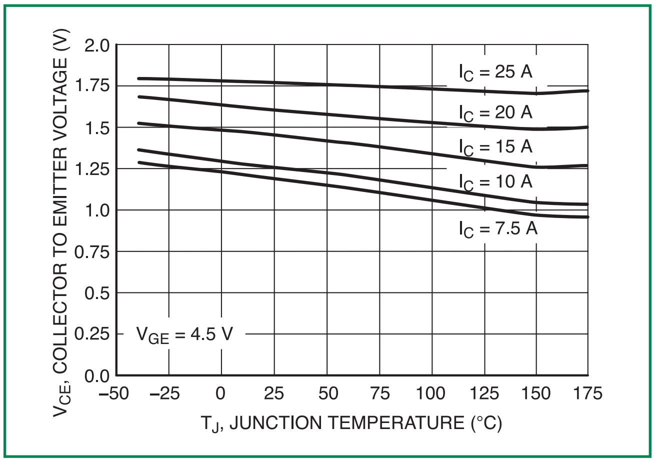


Figure 4. Collector Current vs. Collector–to–Emitter Voltage

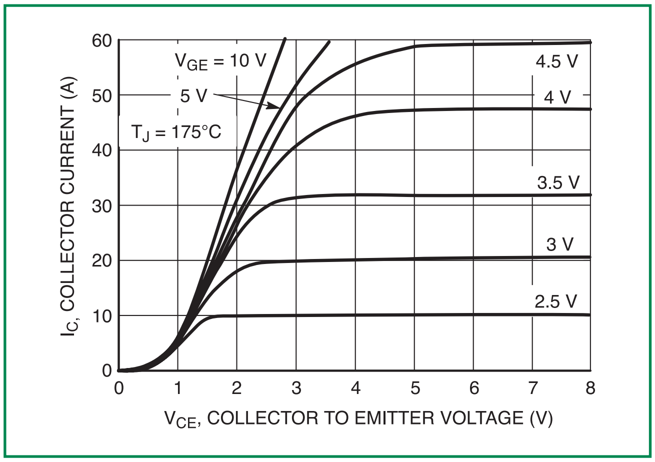


Figure 5. Collector Current vs. Collector–to–Emitter Voltage

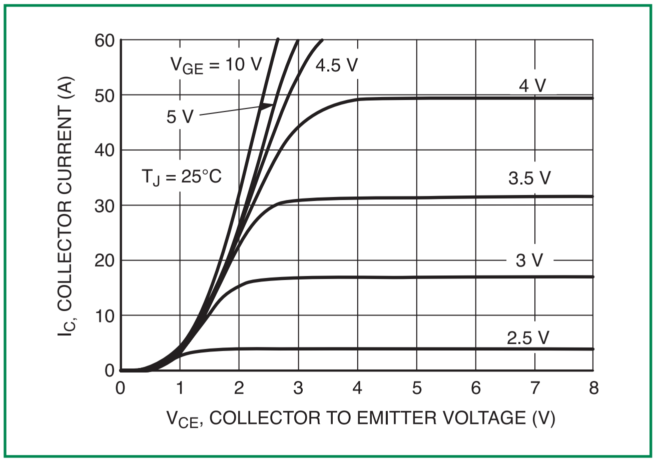


Figure 6. Collector Current vs. Collector–to–Emitter Voltage

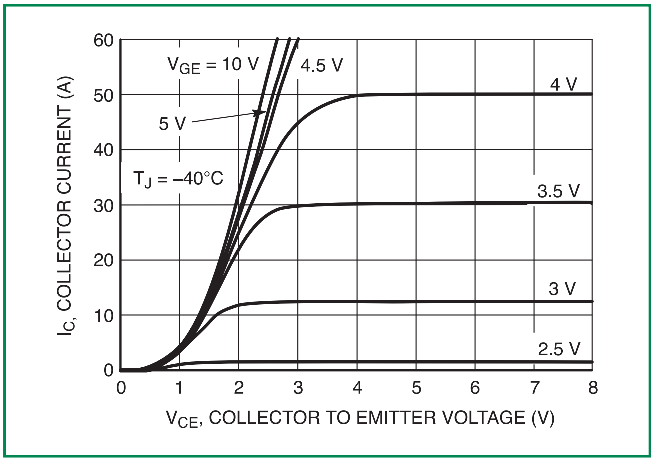


Figure 7. Transfer Characteristics

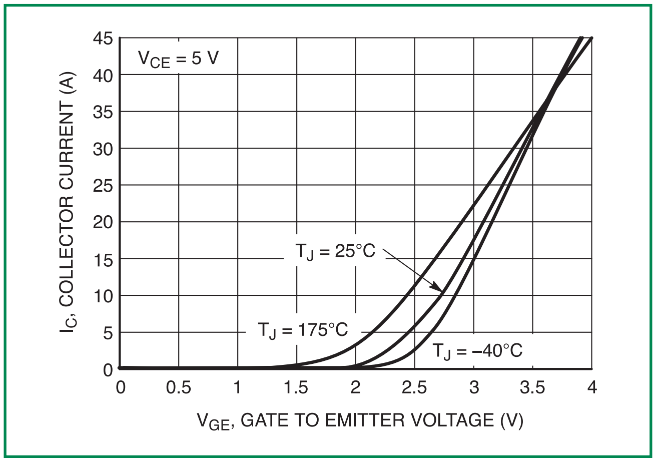


Figure 8. Collector–to–Emitter Leakage Current vs. Temp

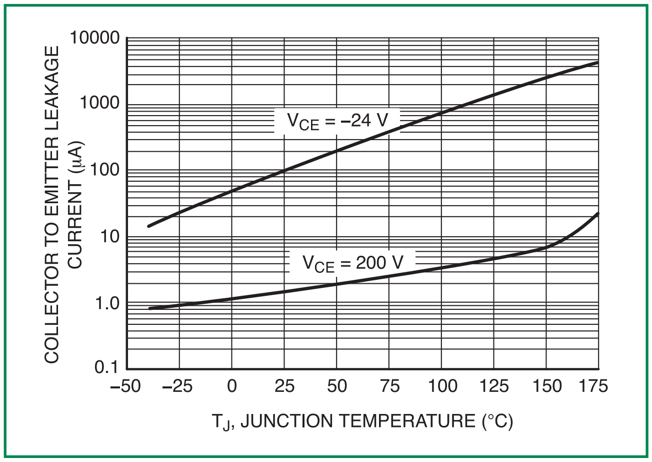


Figure 9. Gate Threshold Voltage vs. Temperature

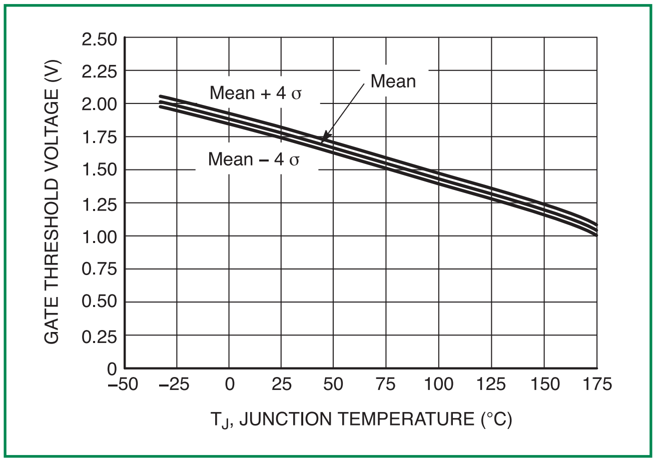


Figure 10. Capacitance vs. Collector–to–Emitter Voltage

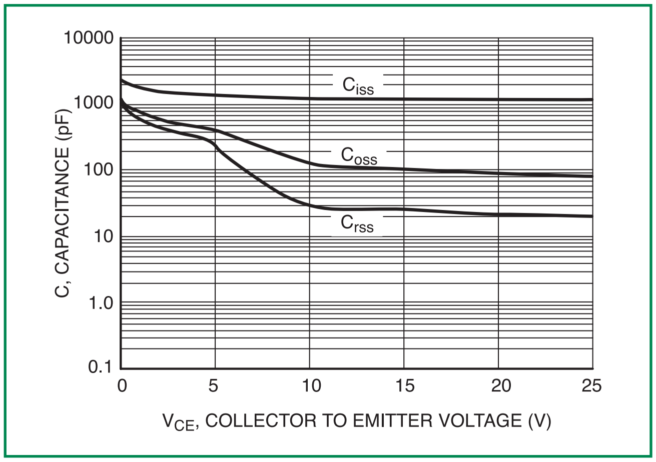


Figure 11. Resistive Switching Fall Time vs. Temperature

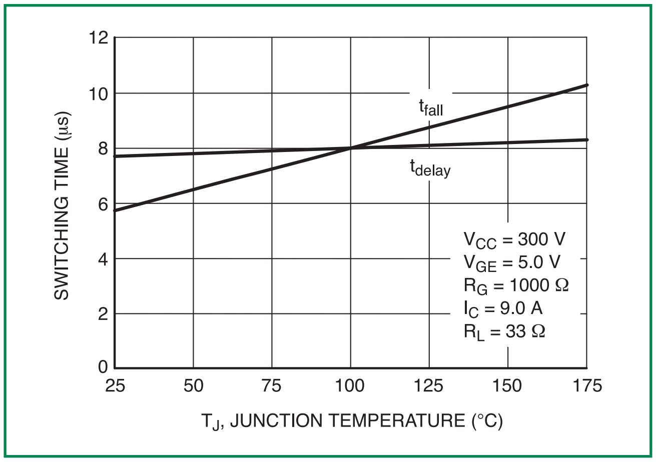


Figure 12. Inductive Switching Fall Time vs. Temperature

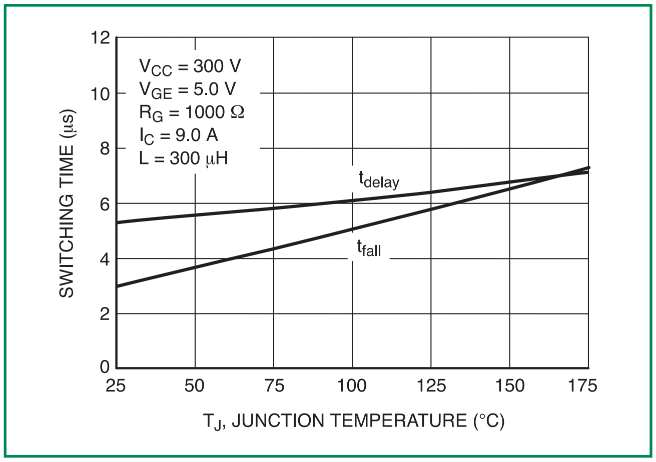


Figure 13. Minimum Pad Transient Thermal Resistance (Non–normalized Junction–to–Ambient)

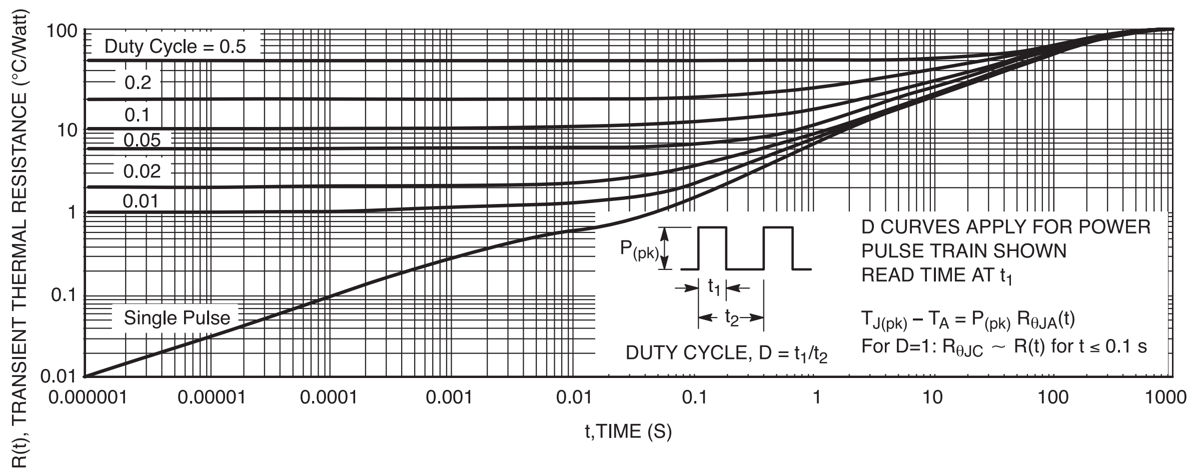
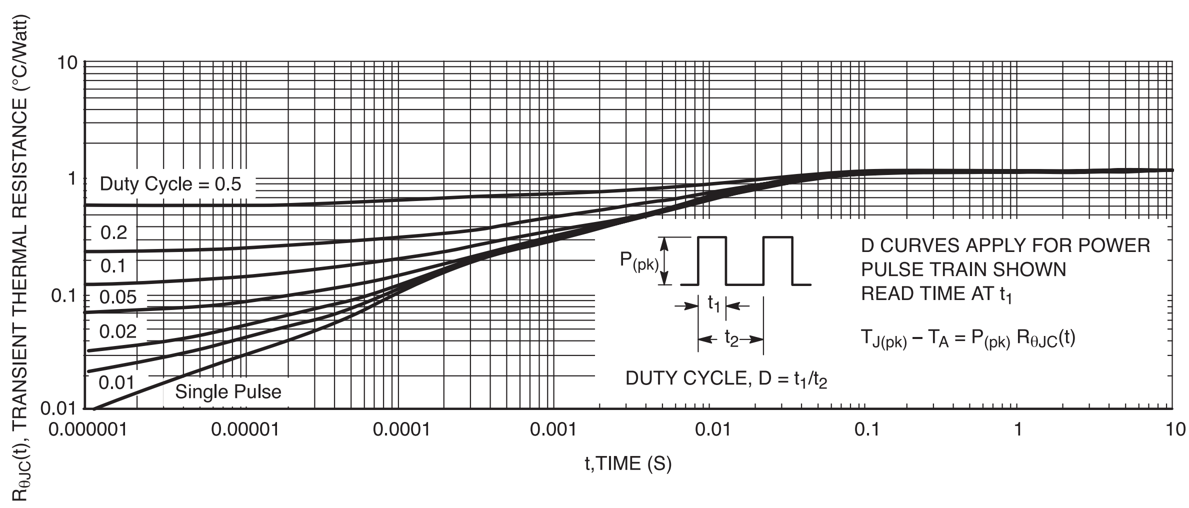
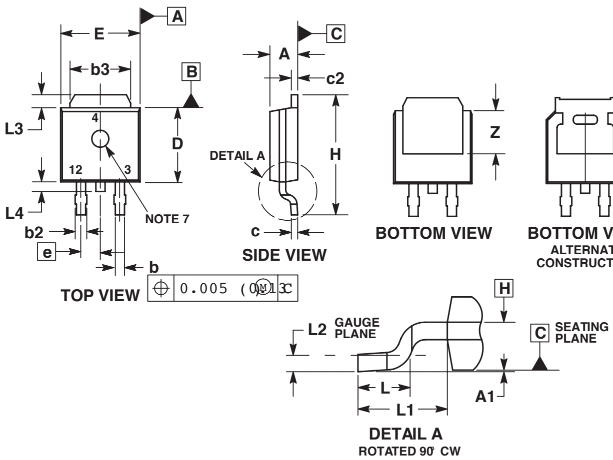


Figure 14. Best Case Transient Thermal Resistance (Non–normalized Junction–to–Case Mounted on Cold Plate)



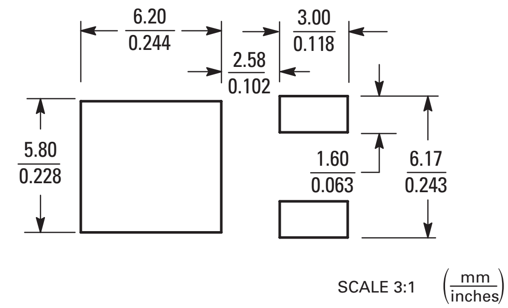
Dimensions



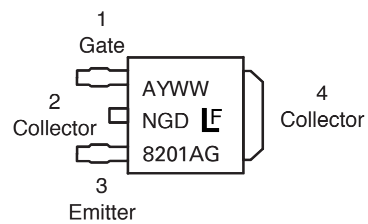
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

Soldering Footrpint



Part Marking System



NGD8201A = Device Code
A= Assembly Location
Y= Year
WW = Work Week
G = Pb–Free Device

ORDERING INFORMATION

Device	Package	Shipping†
NGD8201ANT4G	DPAK (Pb–Free)	2,500 / Tape & Reel