# NPN - 2N6515, 2N6517; PNP - 2N6520

# High Voltage Transistors
## NPN and PNP

**ON Semiconductor®**

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### Features

- Voltage and Current are Negative for PNP Transistors
- These are Pb–Free Devices*



COLLECTOR 3
2 BASE
**NPN**
1 EMITTER

COLLECTOR 3
2 BASE
**PNP**
1 EMITTER

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector – Emitter Voltage<br>2N6515<br>2N6517, 2N6520 | $V_{CEO}$ | <br>250<br>350 | Vdc |
| Collector – Base Voltage<br>2N6515<br>2N6517, 2N6520 | $V_{CBO}$ | <br>250<br>350 | Vdc |
| Emitter – Base Voltage<br>2N6515, 2N6517<br>2N6520 | $V_{EBO}$ | <br>6.0<br>5.0 | Vdc |
| Base Current | $I_B$ | 250 | mAdc |
| Collector Current – Continuous | $I_C$ | 500 | mAdc |
| Total Device Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 625<br>5.0 | mW<br>mW/°C |
| Total Device Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 1.5<br>12 | W<br>mW/°C |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |

### THERMAL CHARACTERISTICS

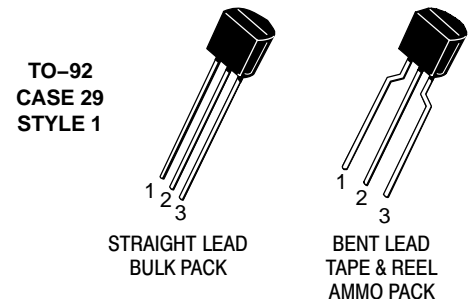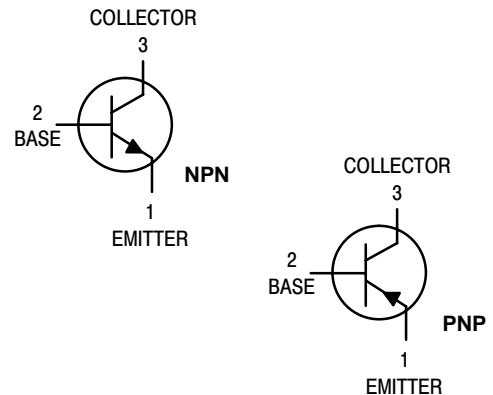| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction–to–Ambient | $R_{\theta JA}$ | 200 | °C/W |
| Thermal Resistance, Junction–to–Case | $R_{\theta JC}$ | 83.3 | °C/W |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**TO–92**
**CASE 29**
**STYLE 1**



1 2 3
STRAIGHT LEAD
BULK PACK

1 2 3
BENT LEAD
TAPE & REEL
AMMO PACK

### MARKING DIAGRAM



2N
65xx
AYWW ▪

xx = 15, 17, or 20
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
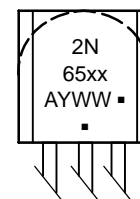
# NPN – 2N6515, 2N6517; PNP – 2N6520

**ELECTRICAL CHARACTERISTICS** ($T_A = 25°C$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | |
| Collector–Emitter Breakdown Voltage (Note 1)<br>($I_C = 1.0$ mAdc, $I_B = 0$)      2N6515<br>2N6517, 2N6520 | $V_{(BR)CEO}$ | 250<br>350 | –<br>– | Vdc |
| Collector–Base Breakdown Voltage<br>($I_C = 100$ μAdc, $I_E = 0$ )      2N6515<br>2N6517, 2N6520 | $V_{(BR)CBO}$ | 250<br>350 | –<br>– | Vdc |
| Emitter–Base Breakdown Voltage<br>($I_E = 10$ μAdc, $I_C = 0$)      2N6515, 2N6517<br>2N6520 | $V_{(BR)EBO}$ | 6.0<br>5.0 | –<br>– | Vdc |
| Collector Cutoff Current<br>($V_{CB} = 150$ Vdc, $I_E = 0$)      2N6515<br>($V_{CB} = 250$ Vdc, $I_E = 0$)      2N6517, 2N6520 | $I_{CBO}$ | –<br>– | 50<br>50 | nAdc |
| Emitter Cutoff Current<br>($V_{EB} = 5.0$ Vdc, $I_C = 0$)      2N6515, 2N6517<br>($V_{EB} = 4.0$ Vdc, $I_C = 0$)      2N6520 | $I_{EBO}$ | –<br>– | 50<br>50 | nAdc |
| **ON CHARACTERISTICS** (Note 1) | | | | |
| DC Current Gain<br>($I_C = 1.0$ mAdc, $V_{CE} = 10$ Vdc)      2N6515<br>2N6517, 2N6520<br><br>($I_C = 10$ mAdc, $V_{CE} = 10$ Vdc)      2N6515<br>2N6517, 2N6520<br><br>($I_C = 30$ mAdc, $V_{CE} = 10$ Vdc)      2N6515<br>2N6517, 2N6520<br><br>($I_C = 50$ mAdc, $V_{CE} = 10$ Vdc)      2N6515<br>2N6517, 2N6520<br><br>($I_C = 100$ mAdc, $V_{CE} = 10$ Vdc)      2N6515<br>2N6517, 2N6520 | $h_{FE}$ | 35<br>20<br><br>50<br>30<br><br>50<br>30<br><br>45<br>20<br><br>25<br>15 | –<br>–<br><br>–<br>–<br><br>300<br>200<br><br>220<br>200<br><br>–<br>– | – |
| Collector–Emitter Saturation Voltage<br>($I_C = 10$ mAdc, $I_B = 1.0$ mAdc)<br>($I_C = 20$ mAdc, $I_B = 2.0$ mAdc)<br>($I_C = 30$ mAdc, $I_B = 3.0$ mAdc)<br>($I_C = 50$ mAdc, $I_B = 5.0$ mAdc) | $V_{CE(sat)}$ | –<br>–<br>–<br>– | 0.30<br>0.35<br>0.50<br>1.0 | Vdc |
| Base–Emitter Saturation Voltage<br>($I_C = 10$ mAdc, $I_B = 1.0$ mAdc)<br>($I_C = 20$ mAdc, $I_B = 2.0$ mAdc)<br>($I_C = 30$ mAdc, $I_B = 3.0$ mAdc) | $V_{BE(sat)}$ | –<br>–<br>– | 0.75<br>0.85<br>0.90 | Vdc |
| Base–Emitter On Voltage<br>($I_C = 100$ mAdc, $V_{CE} = 10$ Vdc) | $V_{BE(on)}$ | – | 2.0 | Vdc |
| **SMALL–SIGNAL CHARACTERISTICS** | | | | |
| Current–Gain – Bandwidth Product (Note 1)<br>($I_C = 10$ mAdc, $V_{CE} = 20$ Vdc, $f = 20$ MHz) | $f_T$ | 40 | 200 | MHz |
| Collector–Base Capacitance<br>($V_{CB} = 20$ Vdc, $I_E = 0$, $f = 1.0$ MHz) | $C_{cb}$ | – | 6.0 | pF |
| Emitter–Base Capacitance<br>($V_{EB} = 0.5$ Vdc, $I_C = 0$, $f = 1.0$ MHz)      2N6515, 2N6517<br>2N6520 | $C_{eb}$ | –<br>– | 80<br>100 | pF |
| **SWITCHING CHARACTERISTICS** | | | | |
| Turn–On Time<br>($V_{CC} = 100$ Vdc, $V_{BE(off)} = 2.0$ Vdc, $I_C = 50$ mAdc, $I_{B1} = 10$ mAdc) | $t_{on}$ | – | 200 | μs |
| Turn–Off Time<br>($V_{CC} = 100$ Vdc, $I_C = 50$ mAdc, $I_{B1} = I_{B2} = 10$ mAdc) | $t_{off}$ | – | 3.5 | μs |

1. Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2.0%.

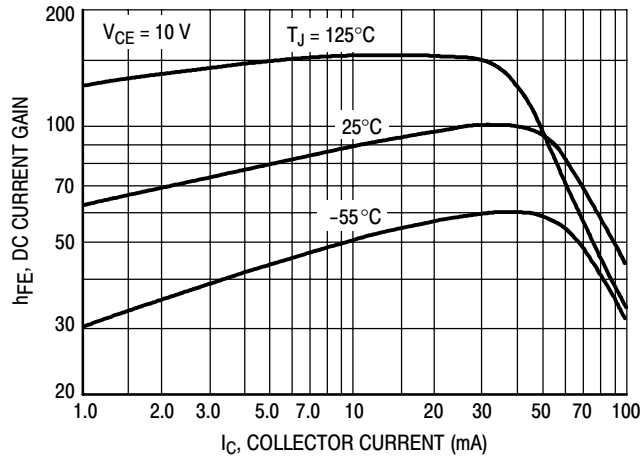## NPN – 2N6515, 2N6517; PNP – 2N6520



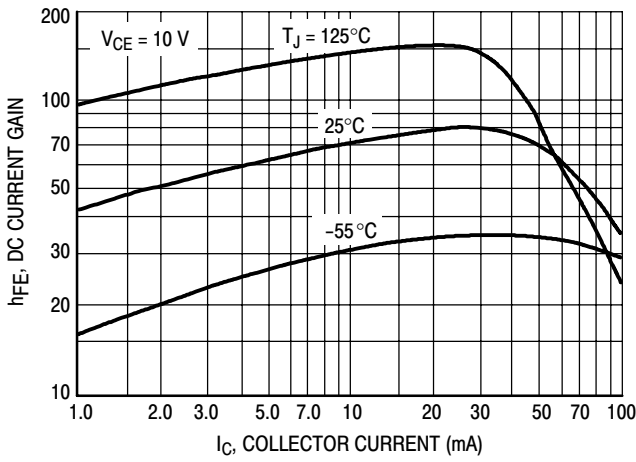**Figure 1. DC Current Gain
NPN 2N6515**
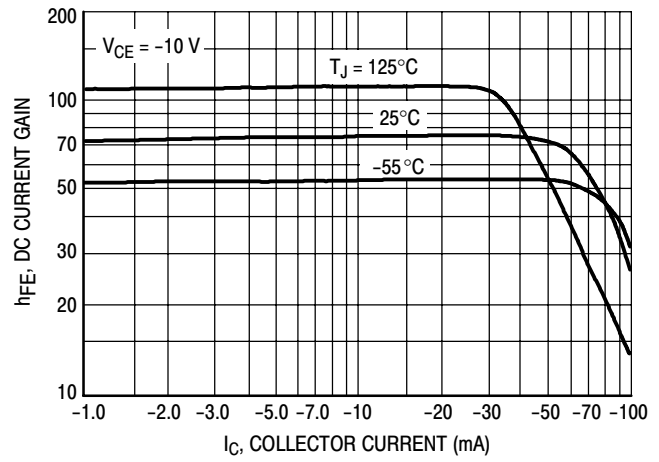


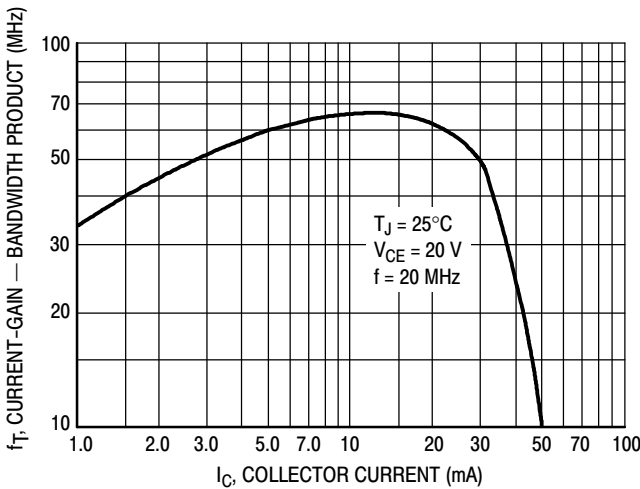**Figure 2. DC Current Gain
NPN 2N6517**



**Figure 3. DC Current Gain
PNP 2N6520**



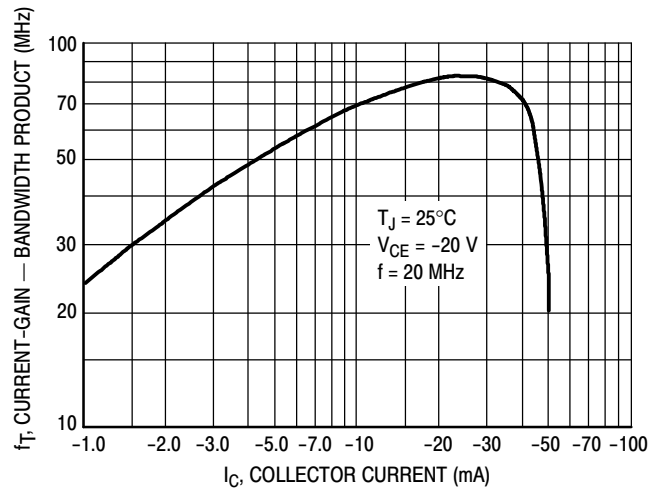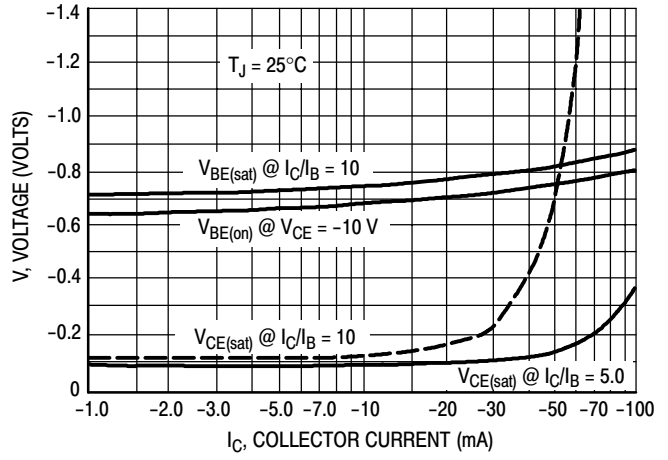**Figure 4. Current–Gain – Bandwidth Product
NPN 2N6515, 2N6517**
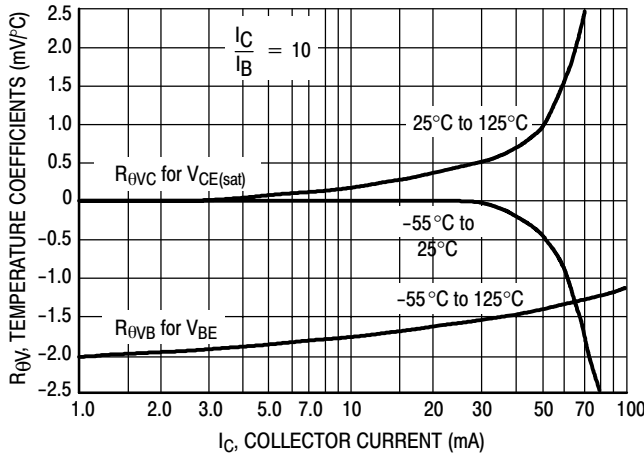


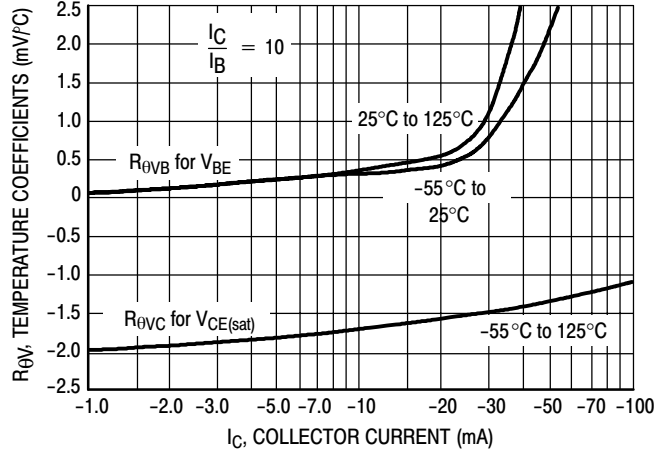**Figure 5. Current–Gain – Bandwidth Product
PNP 2N6520**
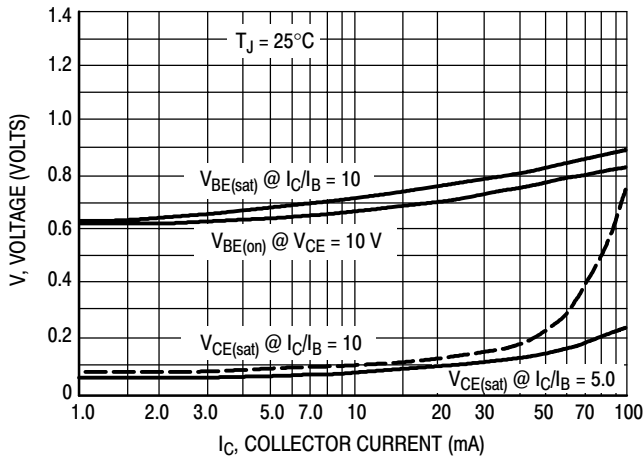
**Figure 6. "On" Voltages**
**NPN 2N6515, 2N6517**



**Figure 7. "On" Voltages**
**PNP 2N6520**



**Figure 8. Temperature Coefficients**
**NPN 2N6515, 2N6517**



**Figure 9. Temperature Coefficients**
**PNP 2N6520**
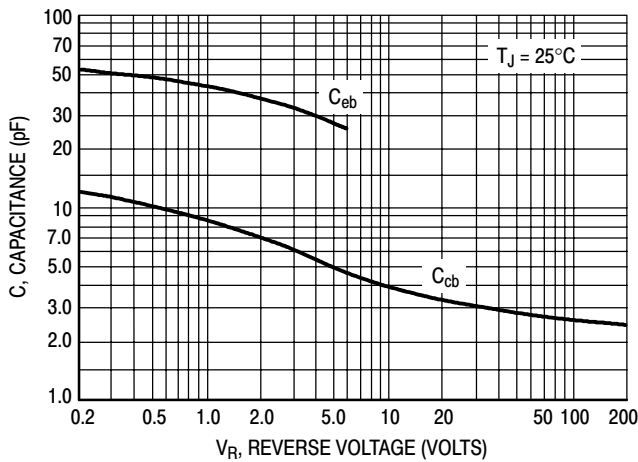


**Figure 10. Capacitance**
**NPN 2N6515, 2N6517**
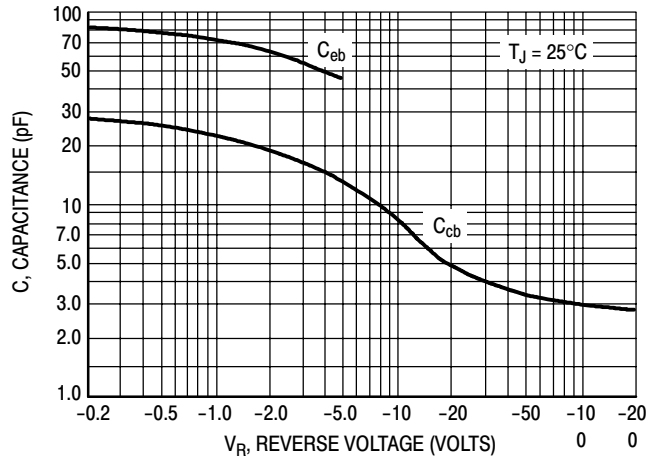


**Figure 11. Capacitance**
**PNP 2N6520**
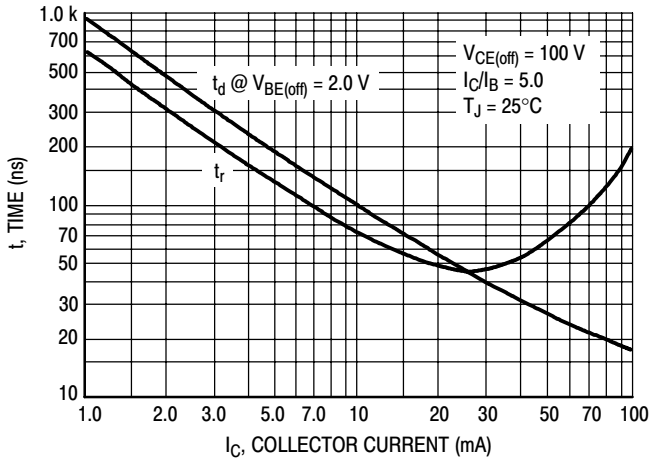
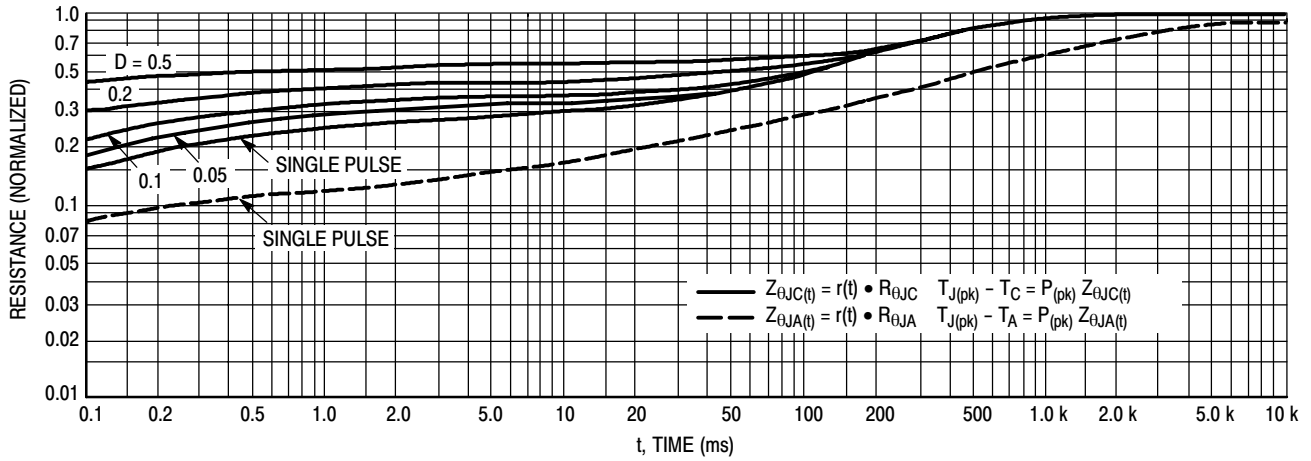Figure 12. Turn–On Time
NPN 2N6515, 2N6517
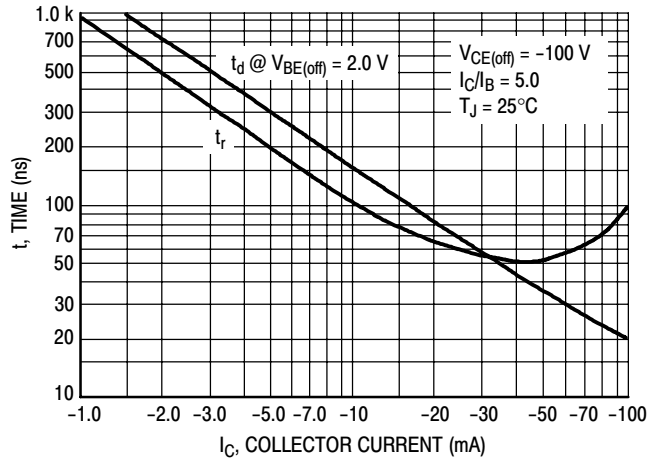


Figure 13. Turn–On Time
PNP 2N6520
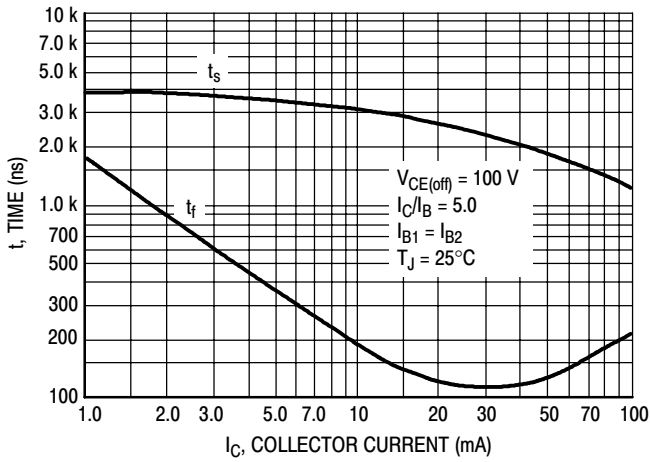


Figure 14. Turn–Off Time
NPN 2N6515, 2N6517
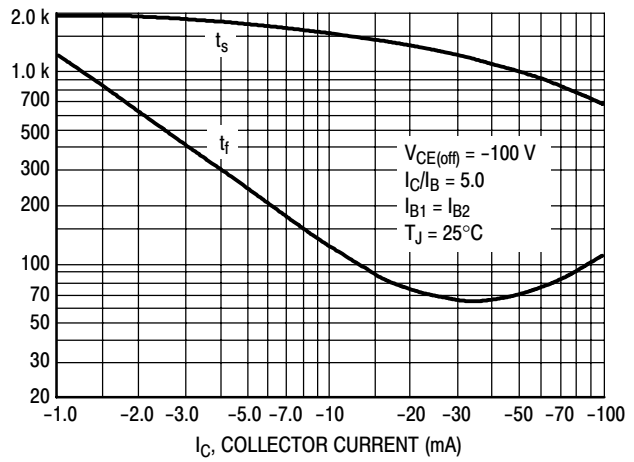


Figure 15. Turn–Off Time
PNP 2N6520



PULSE WIDTH ≈ 100 μs
$t_r$, $t_f$ ≤ 5.0 ns
DUTY CYCLE ≤ 1.0%
FOR PNP TEST CIRCUIT,
REVERSE ALL VOLTAGE POLARITIES
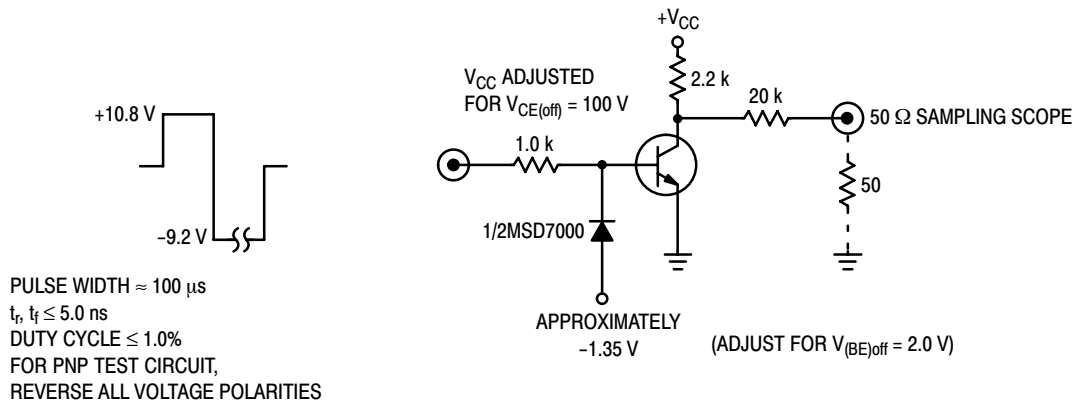
Figure 16. Switching Time Test Circuit

## NPN – 2N6515, 2N6517; PNP – 2N6520



**Figure 17. Thermal Response**



**Figure 18. Active Region Safe Operating Area**



$$\text{DUTY CYCLE} = t_1 \, f = \frac{t_1}{t_P}$$

PEAK PULSE POWER $= P_P$

**Design Note: Use of Transient Thermal Resistance Data**
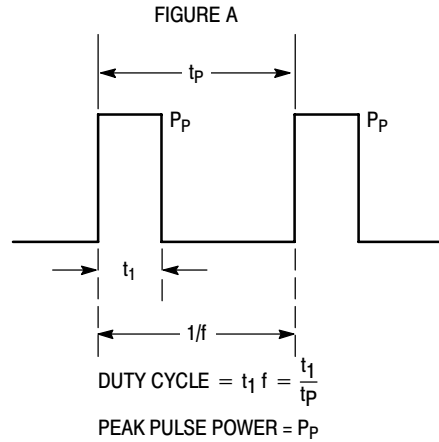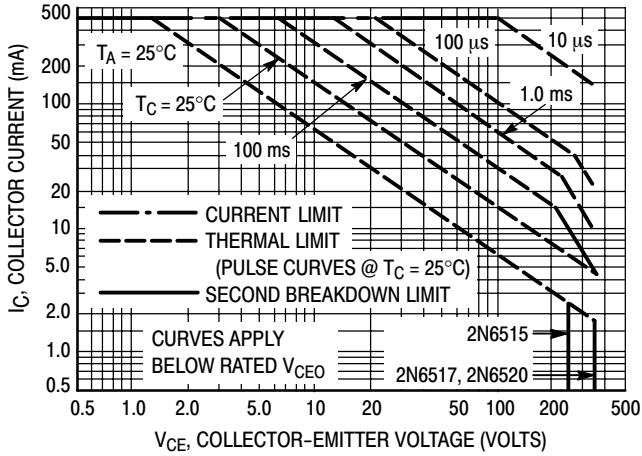
### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| 2N6515RLRMG | TO–92 (Pb–Free) | 2000 Ammo Pack |
| 2N6517G | TO–92 (Pb–Free) | 5000 Unit / Bulk |
| 2N6517RLRPG | TO–92 (Pb–Free) | 2000 Ammo Pack |
| 2N6520RLRAG | TO–92 (Pb–Free) | 2000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**ON Semiconductor**®
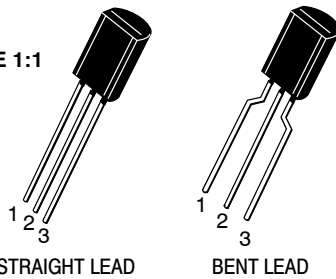
### TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE A

DATE 08 MAY 2012

**SCALE 1:1**

STRAIGHT LEAD     BENT LEAD
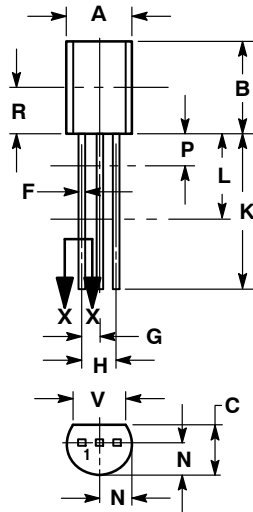
STRAIGHT LEAD
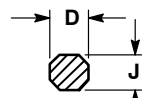
**SECTION X−X**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----|-----|-----|-----|
|  | MIN | MAX | MIN | MAX |
| A | 0.175 | 0.205 | 4.44 | 5.21 |
| B | 0.290 | 0.310 | 7.37 | 7.87 |
| C | 0.125 | 0.165 | 3.18 | 4.19 |
| D | 0.018 | 0.021 | 0.46 | 0.53 |
| F | 0.016 | 0.019 | 0.41 | 0.48 |
| G | 0.045 | 0.055 | 1.15 | 1.39 |
| H | 0.095 | 0.105 | 2.42 | 2.66 |
| J | 0.018 | 0.024 | 0.46 | 0.61 |
| K | 0.500 | --- | 12.70 | --- |
| L | 0.250 | --- | 6.35 | --- |
| N | 0.080 | 0.105 | 2.04 | 2.66 |
| P | --- | 0.100 | --- | 2.54 |
| R | 0.135 | --- | 3.43 | --- |
| V | 0.135 | --- | 3.43 | --- |

BENT LEAD

SEATING PLANE
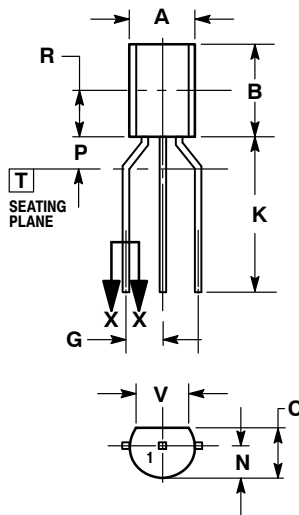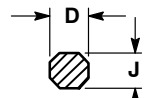
**SECTION X−X**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----|-----|-----|-----|
|  | MIN | MAX | MIN | MAX |
| A | 0.175 | 0.205 | 4.44 | 5.21 |
| B | 0.290 | 0.310 | 7.37 | 7.87 |
| C | 0.125 | 0.165 | 3.18 | 4.19 |
| D | 0.018 | 0.021 | 0.46 | 0.53 |
| G | 0.094 | 0.102 | 2.40 | 2.80 |
| J | 0.018 | 0.024 | 0.46 | 0.61 |
| K | 0.500 | --- | 12.70 | --- |
| N | 0.080 | 0.105 | 2.04 | 2.66 |
| P | --- | 0.100 | --- | 2.54 |
| R | 0.135 | --- | 3.43 | --- |
| V | 0.135 | --- | 3.43 | --- |

## STYLES ON PAGE 2

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STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. $V_{CC}$
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

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| DESCRIPTION: | TO−92 (TO−226) 1 WATT | | PAGE 2 OF 2 |

**PUBLICATION ORDERING INFORMATION**

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