

NPN - 2N6515, 2N6517; PNP - 2N6520

High Voltage Transistors NPN and PNP

Features

- Voltage and Current are Negative for PNP Transistors
- These are Pb-Free Devices*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage 2N6515 2N6517, 2N6520	V_{CEO}	250 350	Vdc
Collector – Base Voltage 2N6515 2N6517, 2N6520	V_{CBO}	250 350	Vdc
Emitter – Base Voltage 2N6515, 2N6517 2N6520	V_{EBO}	6.0 5.0	Vdc
Base Current	I_B	250	mAdc
Collector Current – Continuous	I_C	500	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	625 5.0	mW mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	1.5 12	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	200	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	83.3	$^\circ\text{C}/\text{W}$

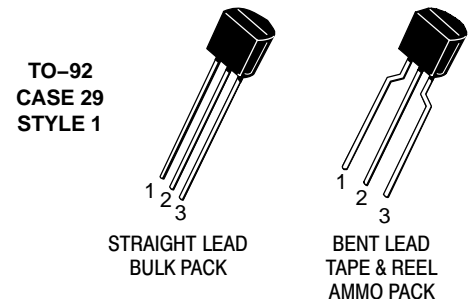
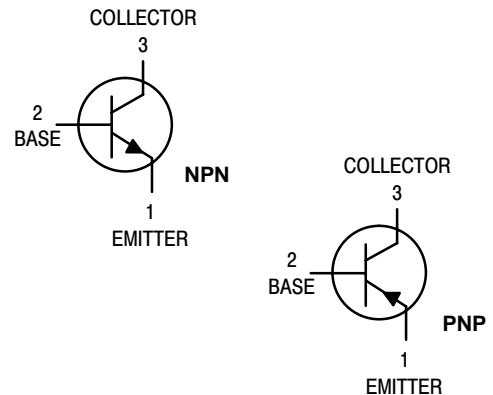
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

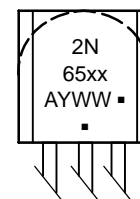


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MARKING DIAGRAM



xx = 15, 17, or 20
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NPN – 2N6515, 2N6517; PNP – 2N6520

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (Note 1) (I _C = 1.0 mA _{dc} , I _B = 0)	2N6515 2N6517, 2N6520	V _{(BR)CEO}	250 350	– –	V _{dc}
Collector–Base Breakdown Voltage (I _C = 100 μA _{dc} , I _E = 0)	2N6515 2N6517, 2N6520	V _{(BR)CBO}	250 350	– –	V _{dc}
Emitter–Base Breakdown Voltage (I _E = 10 μA _{dc} , I _C = 0)	2N6515, 2N6517 2N6520	V _{(BR)EBO}	6.0 5.0	– –	V _{dc}
Collector Cutoff Current (V _{CB} = 150 V _{dc} , I _E = 0) (V _{CB} = 250 V _{dc} , I _E = 0)	2N6515 2N6517, 2N6520	I _{CBO}	– –	50 50	nA _{dc}
Emitter Cutoff Current (V _{EB} = 5.0 V _{dc} , I _C = 0) (V _{EB} = 4.0 V _{dc} , I _C = 0)	2N6515, 2N6517 2N6520	I _{EBO}	– –	50 50	nA _{dc}

ON CHARACTERISTICS (Note 1)

DC Current Gain (I _C = 1.0 mA _{dc} , V _{CE} = 10 V _{dc})	2N6515 2N6517, 2N6520	h _{FE}	35 20	– –	–
(I _C = 10 mA _{dc} , V _{CE} = 10 V _{dc})	2N6515 2N6517, 2N6520		50 30	– –	
(I _C = 30 mA _{dc} , V _{CE} = 10 V _{dc})	2N6515 2N6517, 2N6520		50 30	300 200	
(I _C = 50 mA _{dc} , V _{CE} = 10 V _{dc})	2N6515 2N6517, 2N6520		45 20	220 200	
(I _C = 100 mA _{dc} , V _{CE} = 10 V _{dc})	2N6515 2N6517, 2N6520		25 15	– –	
Collector–Emitter Saturation Voltage (I _C = 10 mA _{dc} , I _B = 1.0 mA _{dc}) (I _C = 20 mA _{dc} , I _B = 2.0 mA _{dc}) (I _C = 30 mA _{dc} , I _B = 3.0 mA _{dc}) (I _C = 50 mA _{dc} , I _B = 5.0 mA _{dc})		V _{CE(sat)}	– – – –	0.30 0.35 0.50 1.0	V _{dc}
Base–Emitter Saturation Voltage (I _C = 10 mA _{dc} , I _B = 1.0 mA _{dc}) (I _C = 20 mA _{dc} , I _B = 2.0 mA _{dc}) (I _C = 30 mA _{dc} , I _B = 3.0 mA _{dc})		V _{BE(sat)}	– – –	0.75 0.85 0.90	V _{dc}
Base–Emitter On Voltage (I _C = 100 mA _{dc} , V _{CE} = 10 V _{dc})		V _{BE(on)}	–	2.0	V _{dc}

SMALL-SIGNAL CHARACTERISTICS

Current–Gain – Bandwidth Product (Note 1) (I _C = 10 mA _{dc} , V _{CE} = 20 V _{dc} , f = 20 MHz)		f _T	40	200	MHz
Collector–Base Capacitance (V _{CB} = 20 V _{dc} , I _E = 0, f = 1.0 MHz)		C _{cb}	–	6.0	pF
Emitter–Base Capacitance (V _{EB} = 0.5 V _{dc} , I _C = 0, f = 1.0 MHz)	2N6515, 2N6517 2N6520	C _{eb}	– –	80 100	pF

SWITCHING CHARACTERISTICS

Turn–On Time (V _{CC} = 100 V _{dc} , V _{BE(off)} = 2.0 V _{dc} , I _C = 50 mA _{dc} , I _{B1} = 10 mA _{dc})		t _{on}	–	200	μs
Turn–Off Time (V _{CC} = 100 V _{dc} , I _C = 50 mA _{dc} , I _{B1} = I _{B2} = 10 mA _{dc})		t _{off}	–	3.5	μs

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

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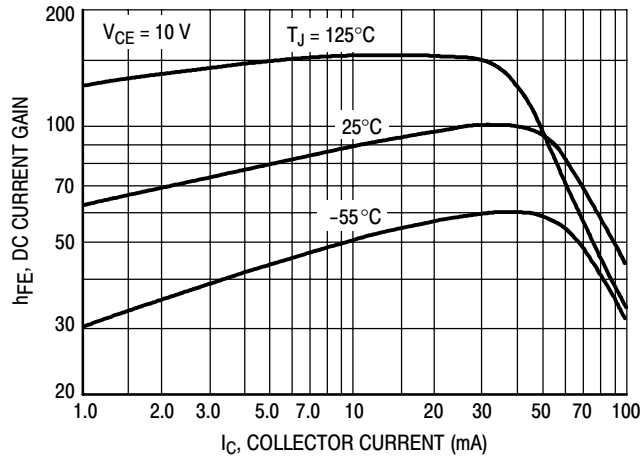


Figure 1. DC Current Gain
NPN 2N6515

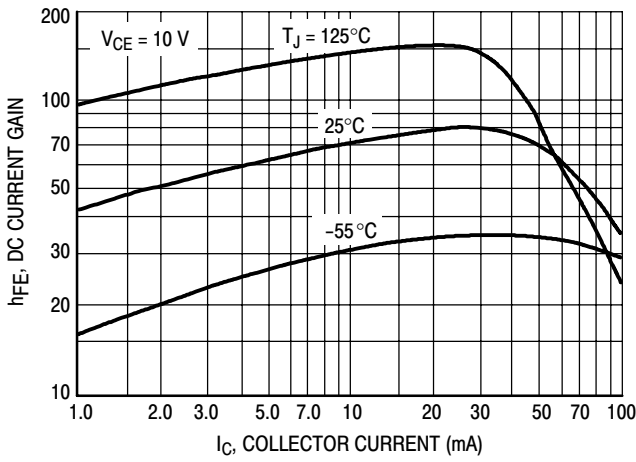


Figure 2. DC Current Gain
NPN 2N6517

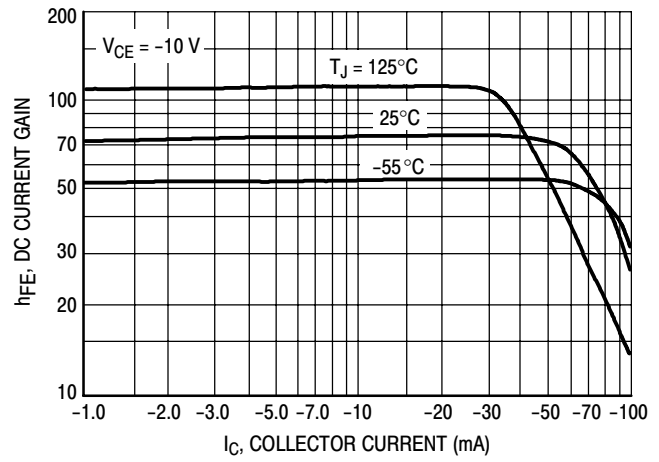


Figure 3. DC Current Gain
PNP 2N6520

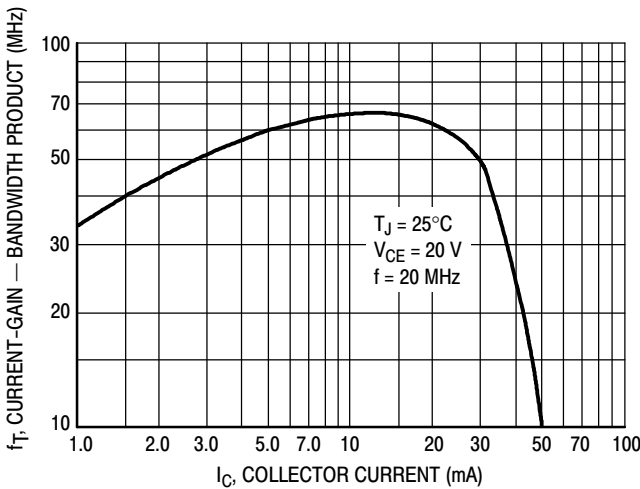


Figure 4. Current-Gain – Bandwidth Product
NPN 2N6515, 2N6517

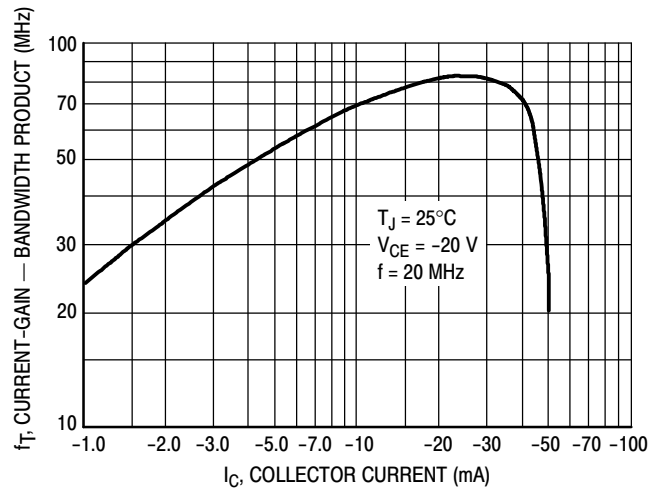
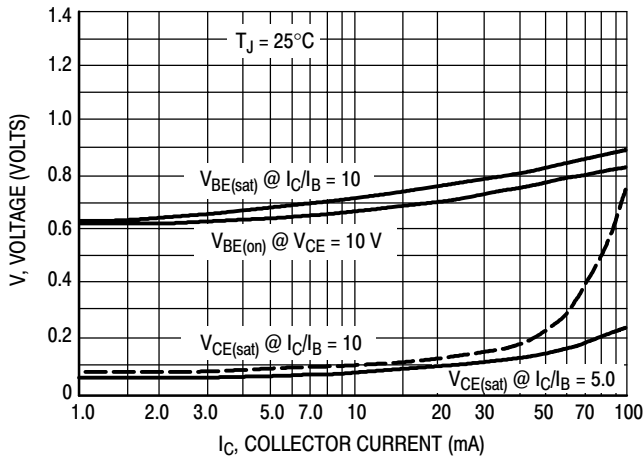
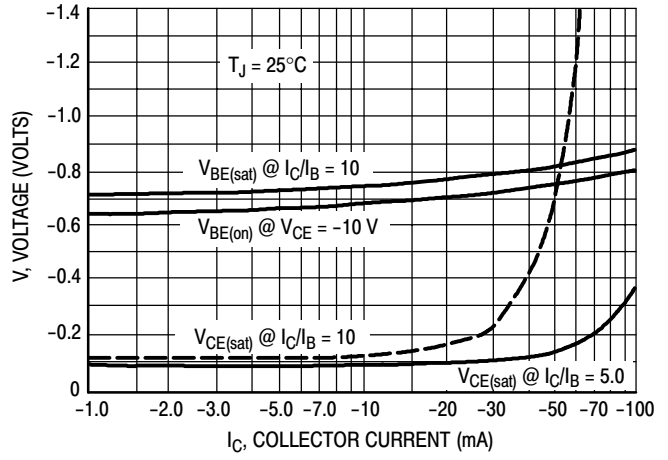


Figure 5. Current-Gain – Bandwidth Product
PNP 2N6520

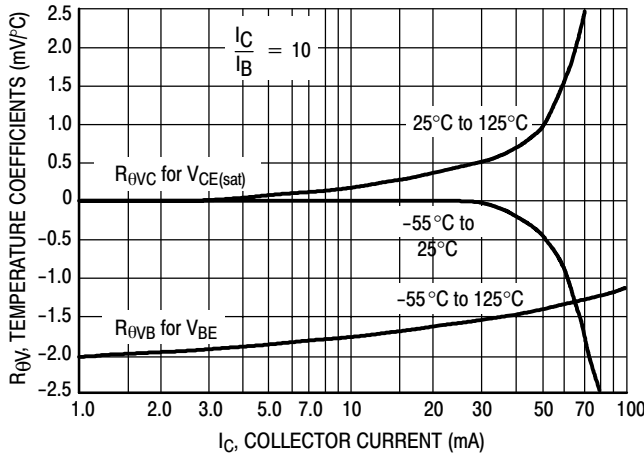
NPN – 2N6515, 2N6517; PNP – 2N6520



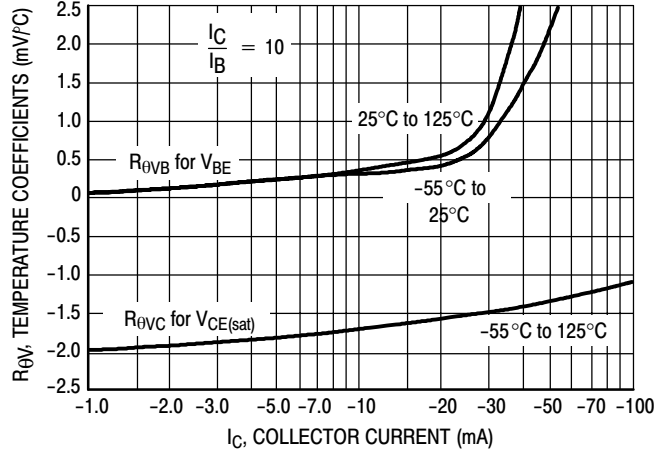
**Figure 6. "On" Voltages
NPN 2N6515, 2N6517**



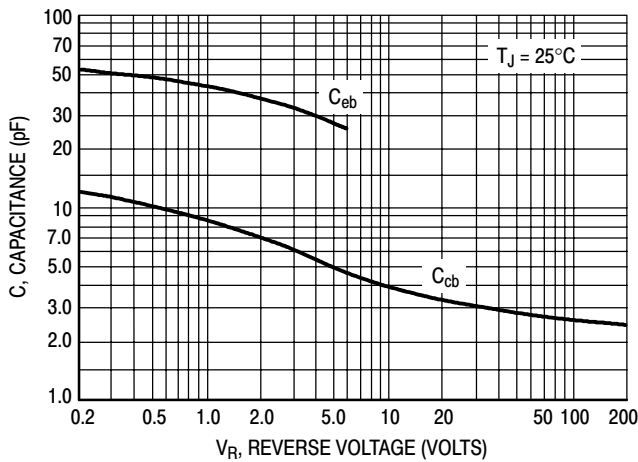
**Figure 7. "On" Voltages
PNP 2N6520**



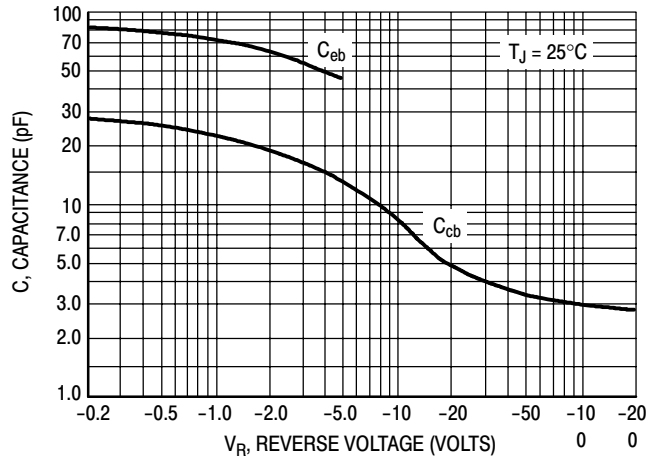
**Figure 8. Temperature Coefficients
NPN 2N6515, 2N6517**



**Figure 9. Temperature Coefficients
PNP 2N6520**

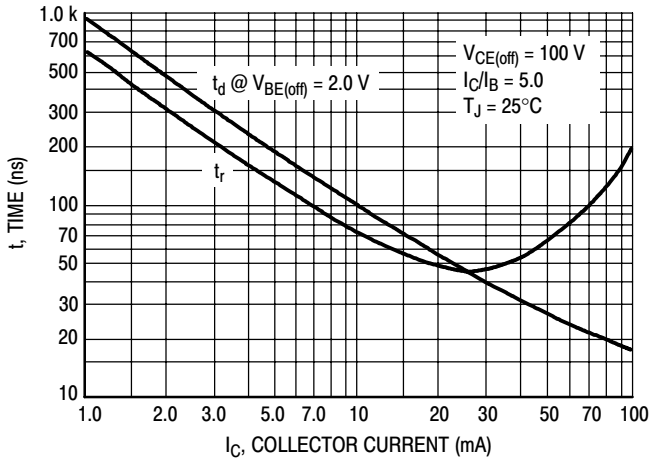


**Figure 10. Capacitance
NPN 2N6515, 2N6517**

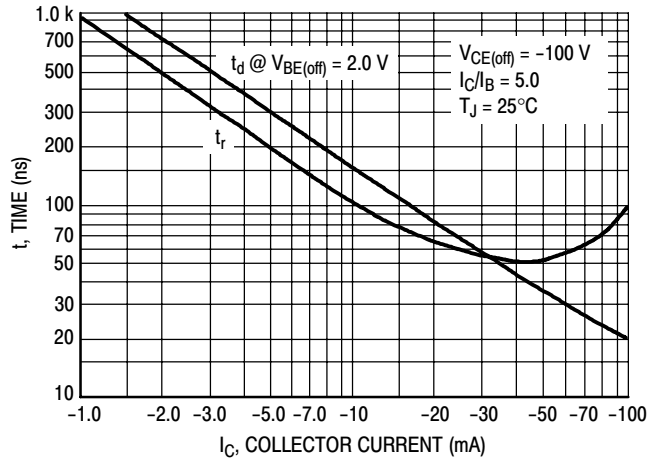


**Figure 11. Capacitance
PNP 2N6520**

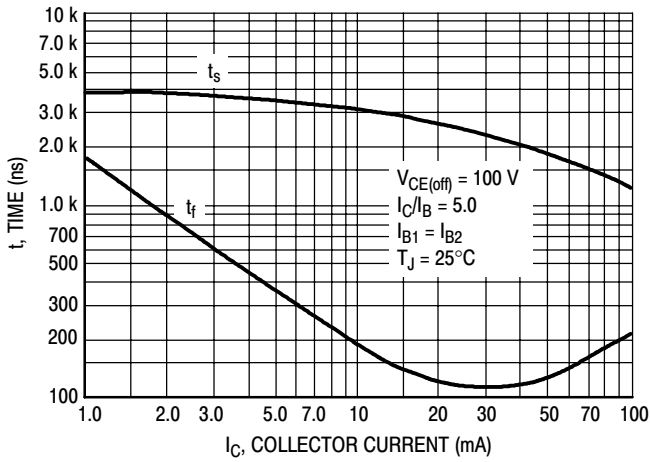
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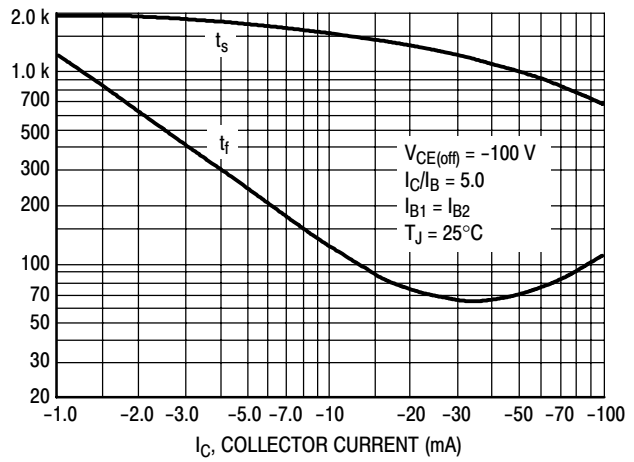
**Figure 12. Turn-On Time
NPN 2N6515, 2N6517**



**Figure 13. Turn-On Time
PNP 2N6520**



**Figure 14. Turn-Off Time
NPN 2N6515, 2N6517**



**Figure 15. Turn-Off Time
PNP 2N6520**

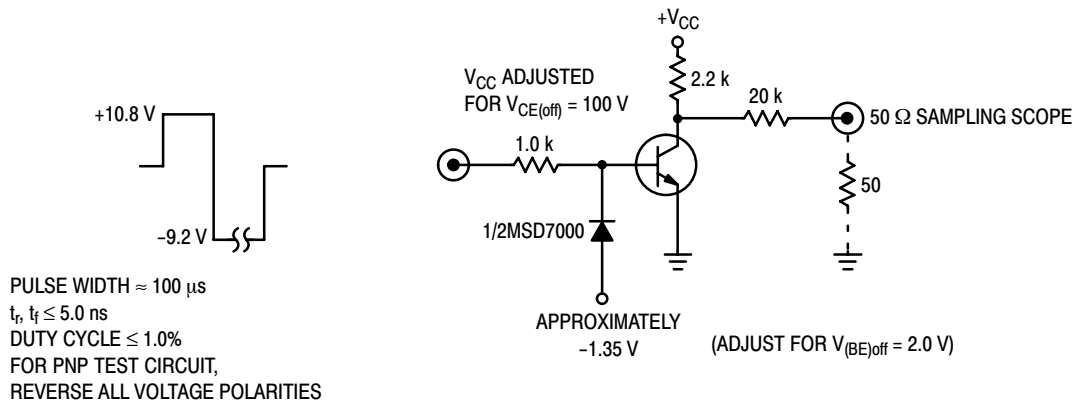
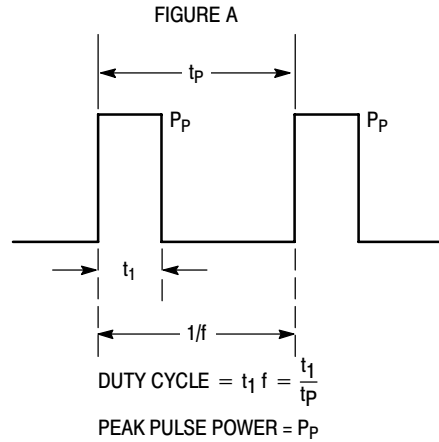
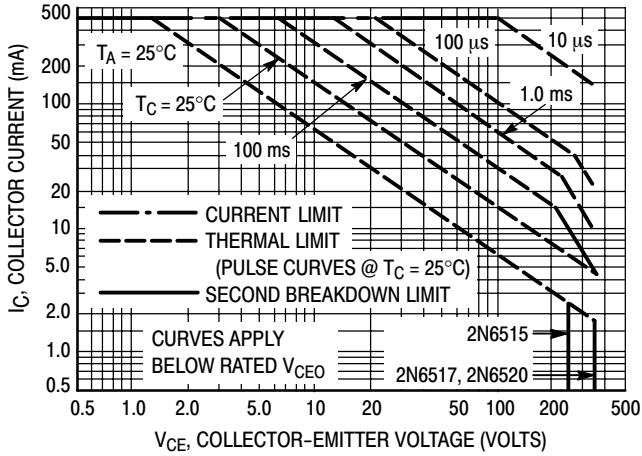
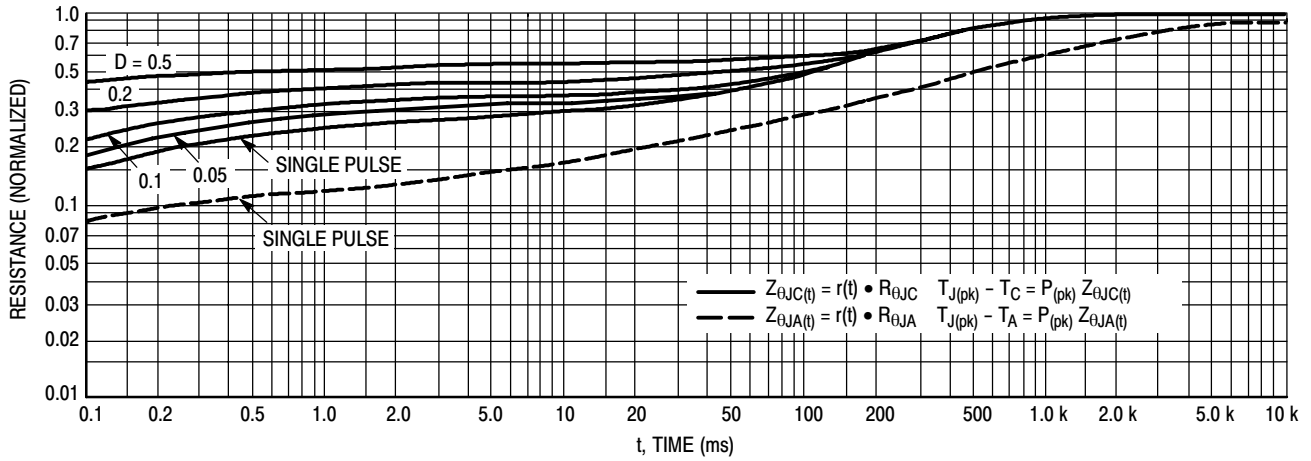


Figure 16. Switching Time Test Circuit

NPN – 2N6515, 2N6517; PNP – 2N6520



ORDERING INFORMATION

Device	Package	Shipping†
2N6515RLRMG	TO-92 (Pb-Free)	2000 Ammo Pack
2N6517G	TO-92 (Pb-Free)	5000 Unit / Bulk
2N6517RLRPG	TO-92 (Pb-Free)	2000 Ammo Pack
2N6520RLRAG	TO-92 (Pb-Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

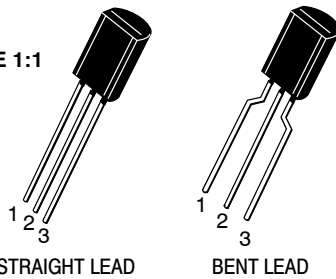
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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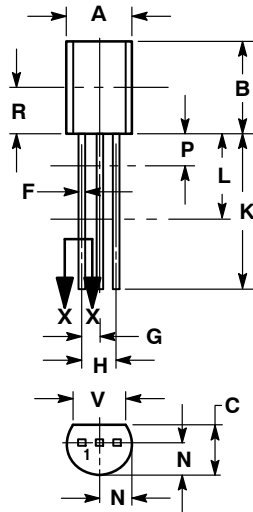


SCALE 1:1

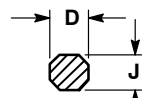


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ISSUE A

DATE 08 MAY 2012



STRAIGHT LEAD

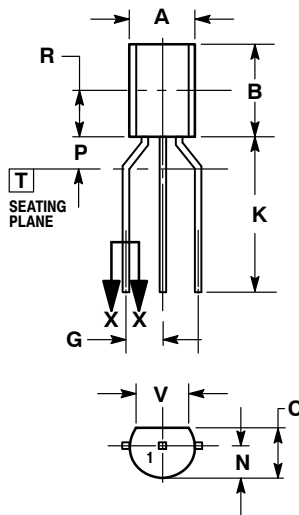


SECTION X-X

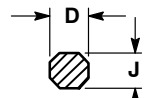
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---



BENT LEAD



SECTION X-X

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

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C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
G	0.094	0.102	2.40	2.80
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---

STYLES ON PAGE 2

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CASE 29-10
ISSUE A**

DATE 08 MAY 2012

- | | | | | |
|---|--|--|---|---|
| <p>STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR</p> | <p>STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR</p> | <p>STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE</p> | <p>STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE</p> |
| <p>STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN</p> | <p>STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE</p> | <p>STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE</p> | <p>STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2</p> | <p>STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE</p> |
| <p>STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE</p> | <p>STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2</p> | <p>STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2</p> | <p>STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE</p> | <p>STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2</p> |
| <p>STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE</p> | <p>STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER</p> | <p>STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED</p> | <p>STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE</p> | <p>STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE</p> |
| <p>STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE</p> | <p>STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN</p> | <p>STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN</p> | <p>STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE</p> | <p>STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2</p> |
| <p>STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT</p> | <p>STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT</p> | <p>STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE</p> | <p>STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE</p> | <p>STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE</p> |
| <p>STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE</p> | <p>STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER</p> | <p>STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT</p> | <p>STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC</p> | <p>STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER</p> |

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