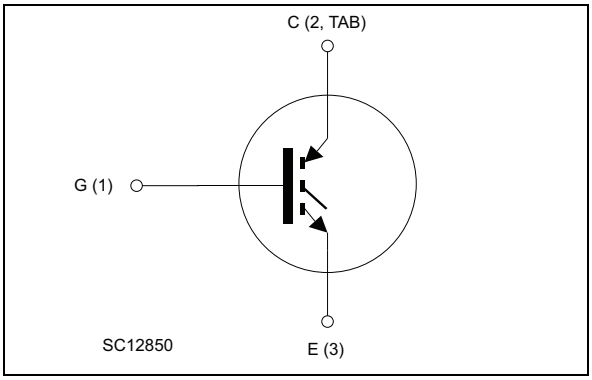
STG40H120F2D7

1200 V, 40 A trench gate field-stop H series IGBT die in D7 packing

Datasheet - preliminary data



Description

This die is an IGBT developed using an advanced propriety trench gate and field-stop structure. This device is part of the improved H series IGBTs.

Features

- Medium speed switching series
- Low $V_{CE(sat)}$= 2 V (typ) at I_C= 40 A
- Positive $V_{CE(sat)}$ temperature coefficient
- Tight parameter distribution
- Low switching-off losses
- Short tail current
- Short-circuit rated

Applications

- Welding
- UPS
- PFC
- Photovoltaic inverter
- High frequency converter

Table 1. Device summary

Order code	V_{DS}	I_{CN}	Die size	Packing
STG40H120F2D7	1200 V	40 A	6.05 x 6.83 mm²	D7

Contents

1 Mechanical parameters

Table 2. Mechanical parameters

Parameter		Value	Unit
Die size with scribe line		6.05 x 6.83	mm²
Wafer size		200	mm
Die thickness		110	µm
Maximum possible dice per wafer		623	dice
Front side passivation		Silicone nitride	
Emitter pad size including gate pad (x4)		5.02 x 1.25	mm²
Gate pad size		1.36 x 1.00	mm²
Front side metallization	composition	AlSiCu	
	thickness	4.5	µm
Back side metallization	composition	Al/Ti/NiV/Ag	
	thickness	0.65	µm
Die bond		Electrically conductive glue or soft solder	
Recommended wire bonding		≤ 500	µm

2 Electrical ratings

Table 3. Absolute maximum ratings (T_J = 25 °C, unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage	1200	V
V_{GE}	Gate-emitter voltage	±20	V
I_C	Continuous collector current limited by T_{Jmax}	40(1)	A
I_{CP}(1)(2)	Pulsed collector current, T_p limited by T_{Jmax}	120(1)	A
T_{SC}(3)	Short circuit with stand time VCC= 600 V,V_{GE}= 15 V,V_P≤ 1200V,T_{Jstart} ≤ 150°C	5	µs
T_j	Operating junction temperature	- 55 to 175	°C

1. Depending on thermal properties of assembly
2. Pulse width limited by maximum junction temperature
3. Not tested at chip level, verified by design/characterization

Table 4. Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	I_C = 1 mA, V_{GE} = 0	1200			V
$V_{CE(sat)}$	Collector-emitter saturation voltage (V_{GS} = 0)	V_{GE} = 15 V, I_C= 15 A			2.3	V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 1 mA	5	6	7	V
I_{GES}	Gate-emitter leakage current (V_{CE} = 0)	V_{GE} = ± 20V, V_{CE} = 0			250	nA
I_{CES}	Collector cut-off current (V_{GE}= 0)	V_{CE} = 1200 V			25	µA

Table 5. Electrical characteristics (1)
(not tested at chip level, verified by design/characterization)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15V, I_C = 40A	-	2	2.6	V
		V_{GE} = 15V, I_C = 40A T_J = 175°C	-	2.59		V
C_{ies}	Input capacitance	V_{CE}= 25 V, f = 1Mhz V_{GE}= 0	-	3190		pF
C_{oes}	Output capacitance		-	223		pF
C_{res}	Reverse transfer capacitive		-	77.4		pF
Q_g	Total gate charge	V_{CC} = 960 V, I_C = 40A, V_{GE} = 15V	-	17.2		nC
Q_{ge}	Gate emitter charge		-	84.8		nC
Q_{gc}	Gate collector charge		-	158		nC

1. Value are referred to packaged device STGW40H120F2 with specific test circuit.

Table 6. Switching characteristics(1) on inductive load
(not tested at chip level, verified by design/characterization)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{cc} = 600 V, I_c = 40A, V_{GE} = 15 V, R_G= 10 Ω T_J = 25 °C	-	37	-	ns
t_r	Current rise time		-	18	-	ns
$t_{d(off)}$	Turn-off delay time		-	152	-	ns
t_f	Fall time		-	82.7	-	ns
E_{off}	Switching off energy		-	1325	-	µJ
$t_{d(on)}$	Turn-on delay time	V_{cc} = 600 V, I_c = 40 A, V_{GE} = 15 V, R_G= 10 Ω T_J = 175 °C	-	36	-	ns
t_f	Current rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	161	-	ns
t_f	Fall time		-	190	-	ns
E_{off}	Switching off energy		-	2465	-	µJ

1. Values are strongly dependent on package/module design and mounting technology. These value are referred to the characterization for the device STGW40H120F2 with specific test circuit. Refer to STGW40H120F2 datasheet for more information

3 Chip layout

Figure 1. Die drawing and dimensions[a]

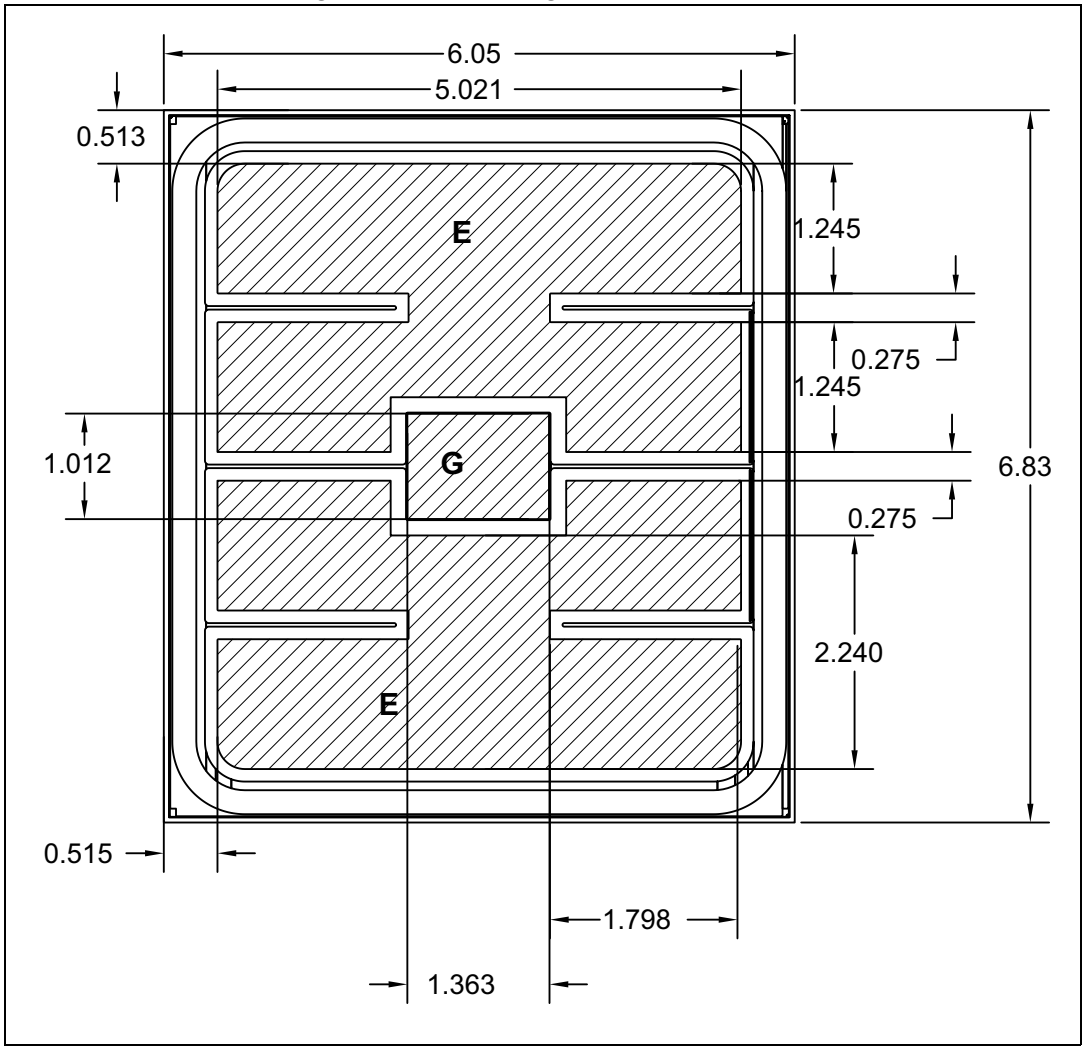
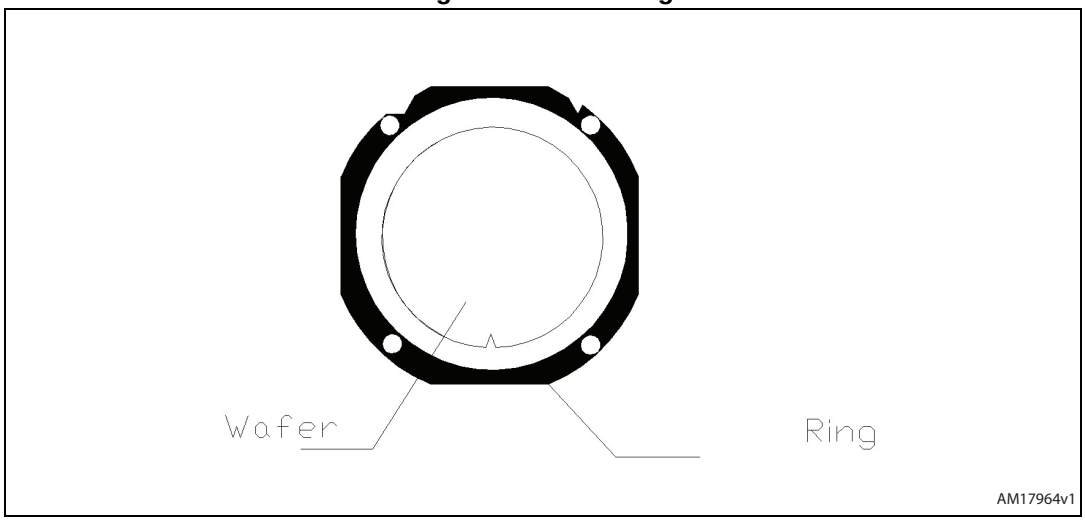


Table 7. Die delivery

Package option	Description	Details
D7	Wafer (8 inches) tested, inked, cut on sticky foil on 10.8" (276 mm) ring (see *Figure 2*)	Wafer (8 inches) is held by ring protected by two carton shells, inside a plastic envelope sealed under vacuum. Maximum number of wafers for each package is 5, weight is about 3.7 Kg.

a. Dimensions are in mm.

Figure 2. D7 drawing



4 Additional information

4.1 Additional testing and screening

For customers requiring product supplied as known good die (KGD) or requiring specific die level testing, please contact the local ST sales office.

4.2 Shipping

Several shipping options are offered, consult the local ST sales office for availability:

- Die in waffle pack - suffix D2 on sales type
- Die on film sticky foil - suffix on sales type D7
- Carrier tape - suffix on sales type D8+KGD

4.3 Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singular dice are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

4.4 Wafer/die storage

Once opened, the wafer must be stored in a dry, inert atmosphere, such as nitrogen. Optimum temperature for storage is 18 °C ± 2 °C with as few variations as possible to avoid parasitic polymerization of the adhesive. Sawn wafers must be processed within 12 weeks after receipt by customer.

After the customer opens the package, the customer is responsible for the products.

5 Revision history

Table 8. Document revision history

Date	Revision	Changes
27-Jan-2015	1	Initial release.