ON Semiconductor

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NGTD17T65F2

IGBT Die

Trench Field Stop II IGBT Die for motor drive and inverter applications.

Features

- Extremely Efficient Trench with Field Stop Technology
- Low V_{CE(sat)} Loss Reduces System Power Dissipation

Typical Applications

- Industrial Motor Drives
- Solar Inverters
- UPS Systems
- Welding

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Collector–Emitter Voltage, T _J = 25°C	V_{CE}	650	V
DC Collector Current, limited by T _{J(max)}	I _C	(Note 1)	Α
Pulsed Collector Current (Note 2)	I _{C, pulse}	160	Α
Gate-Emitter Voltage	V_{GE}	±20	V
Maximum Junction Temperature	T_J	-55 to +175	°C
Short Circuit Withstand Time, $V_{GE} = 15 \text{ V}, V_{CE} = 500 \text{V}, T_J \le 150^{\circ}\text{C}$	T _{SC}	5.0	μS

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Depending on thermal properties of assembly.
- 2. T_{pulse} limited by T_{jmax} , 10 μs pulse, V_{GE} = 15 V.

MECHANICAL DATA

Parameter	Value	Unit	
Die Size	3915 x 4115	μm ²	
Emitter Pad Size	See die layout	μm ²	
Gate Pad Size	585 x 600	μm ²	
Die Thickness	3	mils	
Wafer Size	150	mm	
Top Metal	4 μm AISI		
Back Metal	2 μm TiNiAg		
Max possible chips per wafer	778		
Passivation frontside	Oxide-Nitride		
Reject ink dot size	25 mils		
Recommended storage environment: In original container, in dry nitrogen, or temperature of 18–28°C, 30–65%RH		pe in ring-pack e: < 3 months	

ORDERING INFORMATION

Device	Inking?	Shipping		
NGTD17T65F2WP	Yes	Bare Wafer on Tape		
NGTD17T65F2SWK	Yes	Sawn Wafer on Tape		

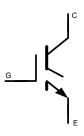


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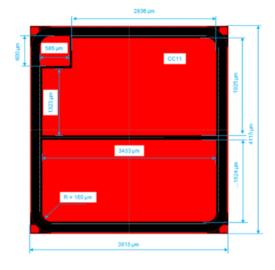
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 $V_{RCE} = 650 \text{ V}$ $I_C = \text{Limited by } T_{J(max)}$

IGBT DIE



DIE OUTLINE



NGTD17T65F2

ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified)

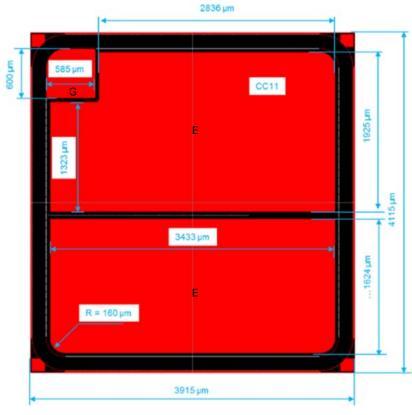
Parameter	Test Conditions	Symbol	Min	Тур	Max	Units
STATIC CHARACTERISTICS						
Collector-Emitter Breakdown Voltage	$V_{GE} = 0 \text{ V}, I_{C} = 500 \mu A$	V _{(BR)CES}	650			V
Collector–Emitter Saturation Voltage	V _{GE} = 15 V, I _C = 40 A	V _{CE(sat)}		1.7	2.0	V
Gate-Emitter Threshold Voltage	$V_{GE} = V_{CE}, I_{C} = 350 \mu A$	V _{GE(TH)}	4.5	5.5	6.5	V
Collector-Emitter Cutoff Current	V _{GE} = 0 V, V _{CE} = 650 V	I _{CES}			0.5	mA
Gate Leakage Current	V _{GE} = 20 V, V _{CE} = 0 V	I _{GES}			200	nA

DYNAMIC CHARACTERISTICS

Input Capacitance		C _{ies}	4060	pF
Output Capacitance	$V_{CE} = 20 \text{ V}, V_{GE} = 0 \text{ V}, f = 1$ MHz	C _{oes}	179	pF
Reverse Transfer Capacitance		C _{res}	115	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DIE LAYOUT



 $E = Emitter pad \\ G = Gate pad \\ All dimensions in <math>\mu m$

Further Electrical Characteristic

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

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