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# MJB41C, NJVMJB41CT4G (NPN), MJB42C, NJVMJB42CT4G (PNP)



ON Semiconductor®

http://onsemi.com

## Complementary Silicon Plastic Power Transistors

### D<sup>2</sup>PAK for Surface Mount

#### Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Electrically the Same as TIP41 and T1P42 Series
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- Pb-Free Packages are Available

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	100	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current – Continuous – Peak	$I_C$	6.0 10	Adc
Base Current	$I_B$	2.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	65 0.52	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016	W W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (Note 1)	E	62.5	mJ
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

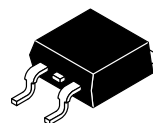
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.92	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1.  $I_C = 2.5\text{ A}$ ,  $L = 20\text{ mH}$ , P.R.F. = 10 Hz,  $V_{CC} = 10\text{ V}$ ,  $R_{BE} = 100\ \Omega$
2. When surface mounted to an FR-4 board using the minimum recommended pad size.

### COMPLEMENTARY SILICON POWER TRANSISTORS 6 AMPERES, 100 VOLTS, 65 WATTS

#### MARKING DIAGRAM



D<sup>2</sup>PAK  
CASE 418B  
STYLE 1



J4xC = Specific Device Code  
x = 1 or 2  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MJB41CG	D <sup>2</sup> PAK (Pb-Free)	50 Units / Rail
MJB41CT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel
NJVMJB41CT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel
MJB42CG	D <sup>2</sup> PAK (Pb-Free)	50 Units / Rail
MJB42CT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel
NJVMJB42CT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MJB41C, NJVMJB41CT4G (NPN), MJB42C, NJVMJB42CT4G (PNP)

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (Note 3) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	100	–	Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	0.7	mAdc
Collector Cutoff Current ( $V_{CE} = 100\text{ Vdc}$ , $V_{EB} = 0$ )	$I_{CES}$	–	100	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	50	$\mu\text{Adc}$
<b>ON CHARACTERISTICS (Note 3)</b>				
DC Current Gain ( $I_C = 0.3\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	30 15	– 75	–
Collector–Emitter Saturation Voltage ( $I_C = 6.0\text{ Adc}$ , $I_B = 600\text{ mAdc}$ )	$V_{CE(sat)}$	–	1.5	Vdc
Base–Emitter On Voltage ( $I_C = 6.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	–	2.0	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain – Bandwidth Product ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	3.0	–	MHz
Small–Signal Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	20	–	–

3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

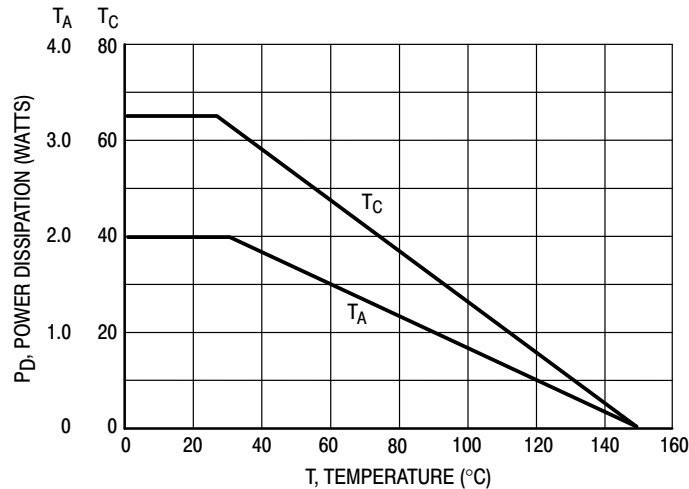


Figure 1. Power Derating

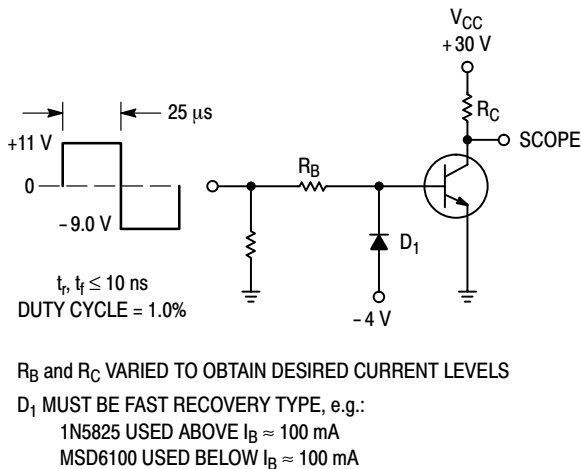


Figure 2. Switching Time Test Circuit

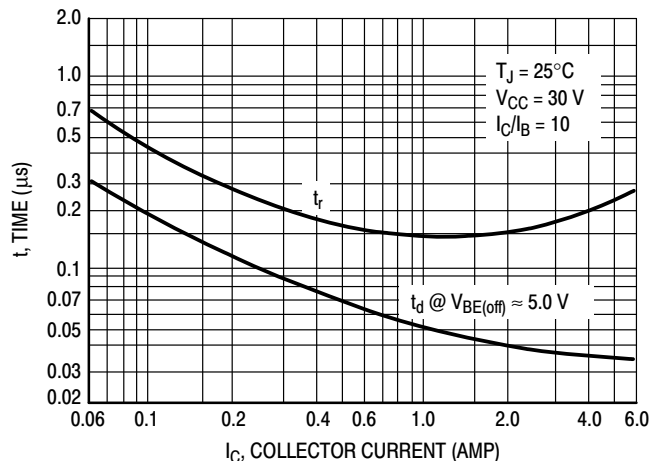


Figure 3. Turn–On Time

# MJB41C, NJVMJB41CT4G (NPN), MJB42C, NJVMJB42CT4G (PNP)

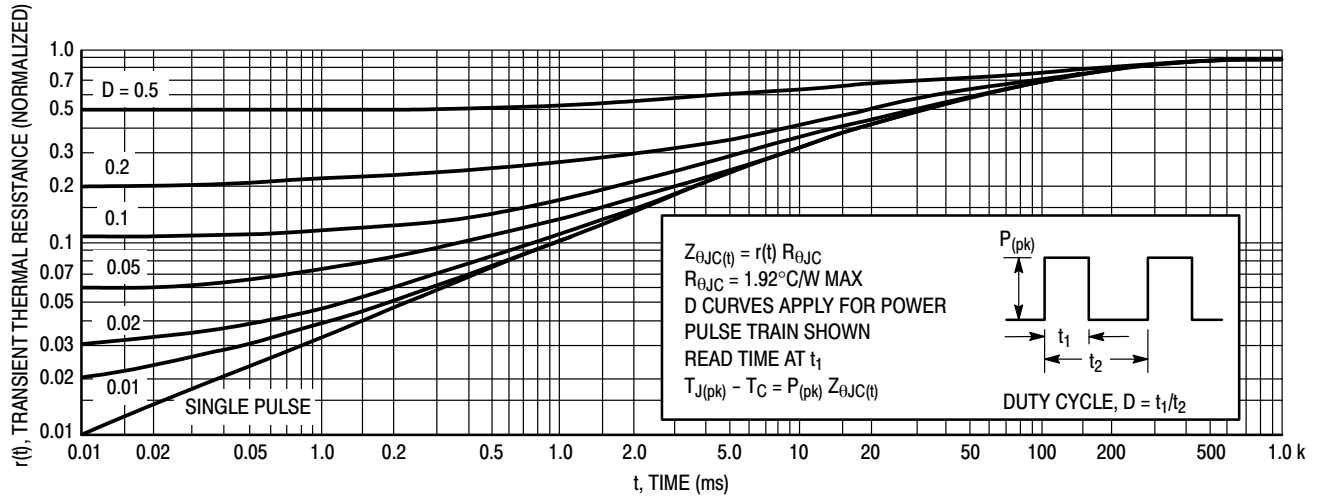


Figure 4. Thermal Response

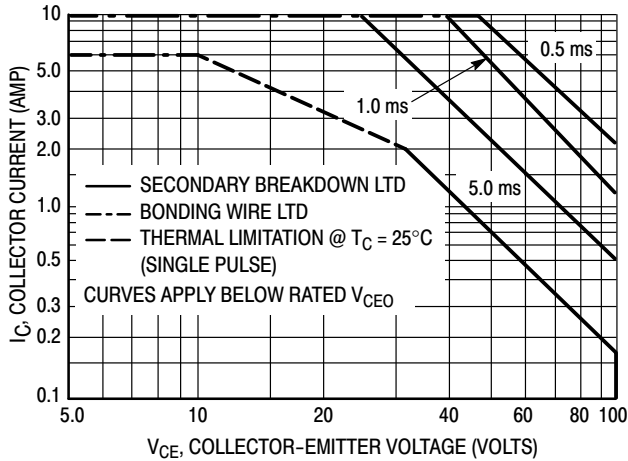


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

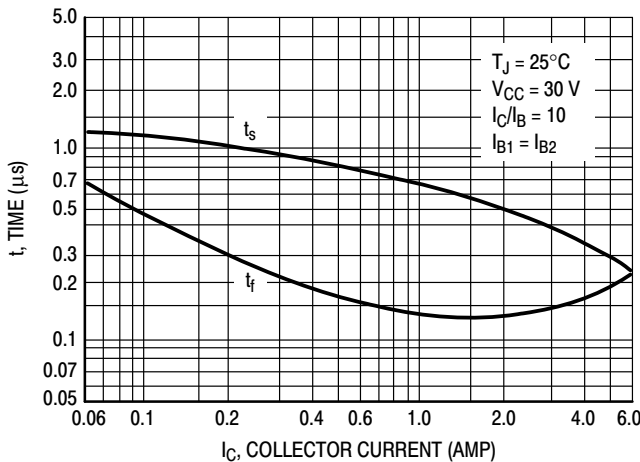


Figure 6. Turn-Off Time

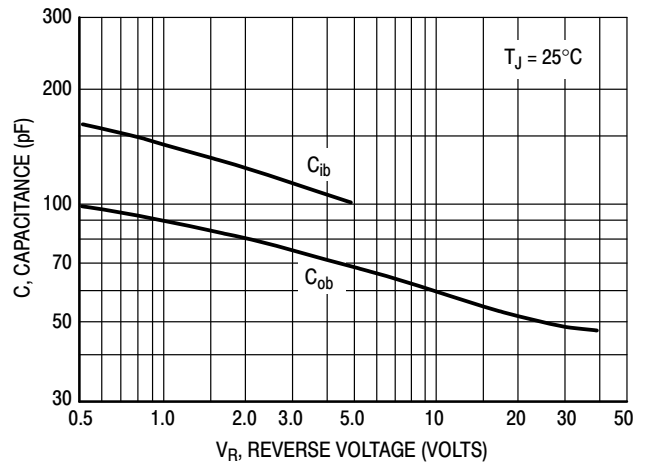


Figure 7. Capacitance

# MJB41C, NJVMJB41CT4G (NPN), MJB42C, NJVMJB42CT4G (PNP)

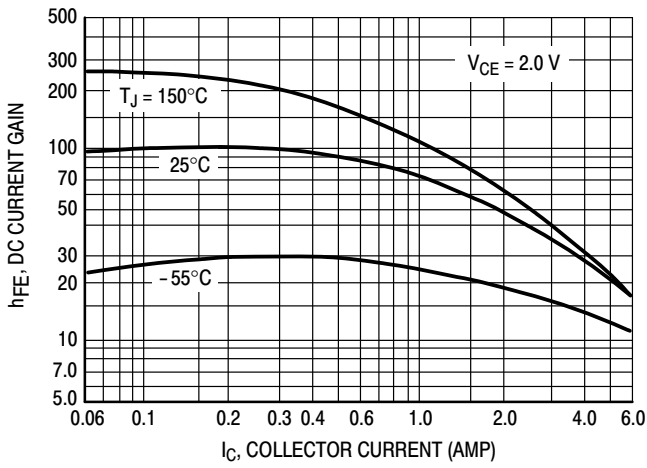


Figure 8. DC Current Gain

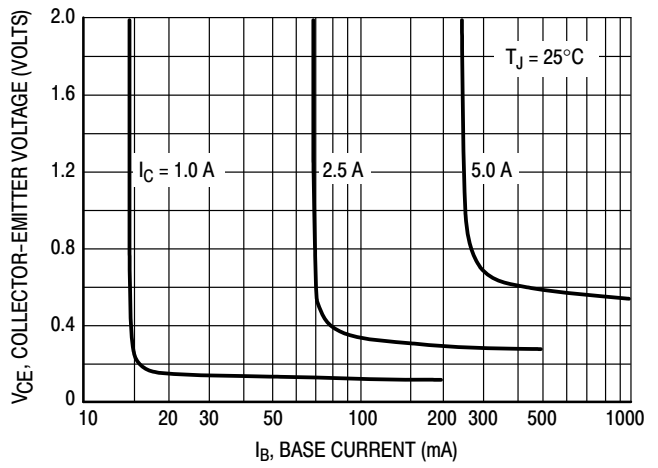


Figure 9. Collector Saturation Region

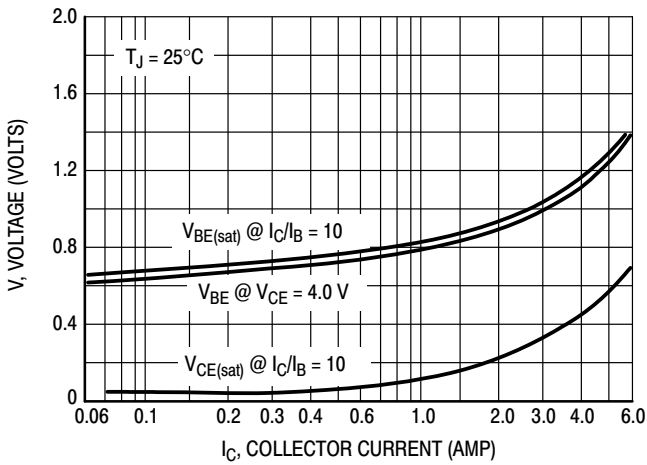


Figure 10. "On" Voltages

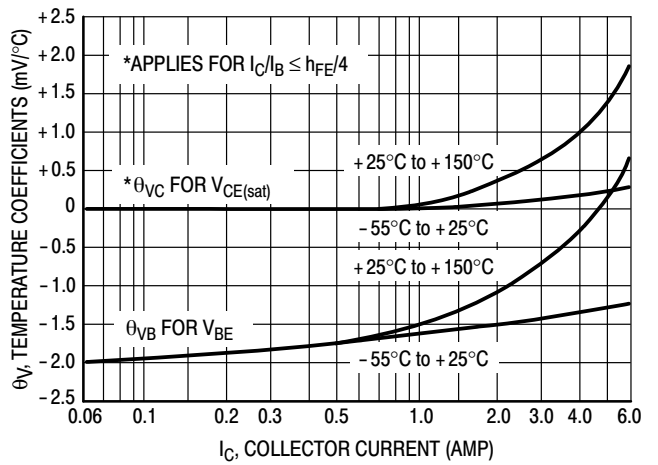


Figure 11. Temperature Coefficients

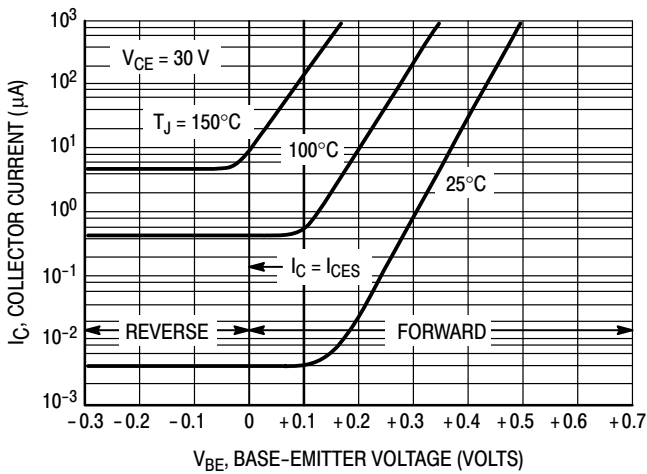


Figure 12. Collector Cut-Off Region

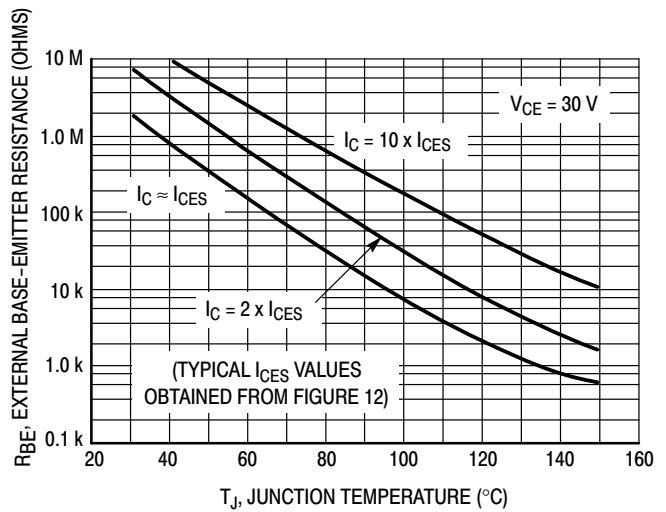


Figure 13. Effects of Base-Emitter Resistance

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

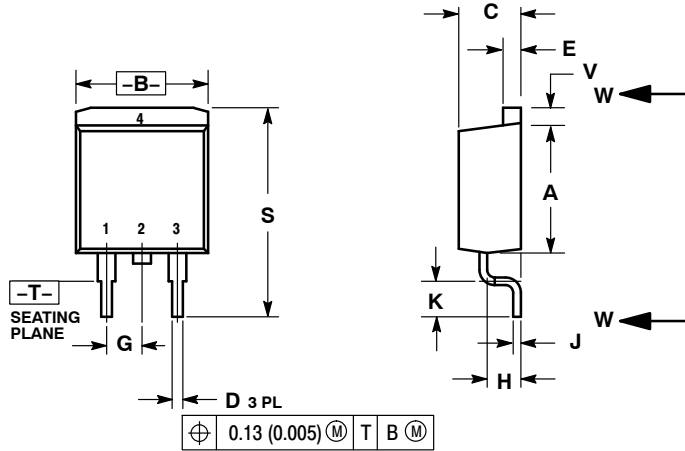
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**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

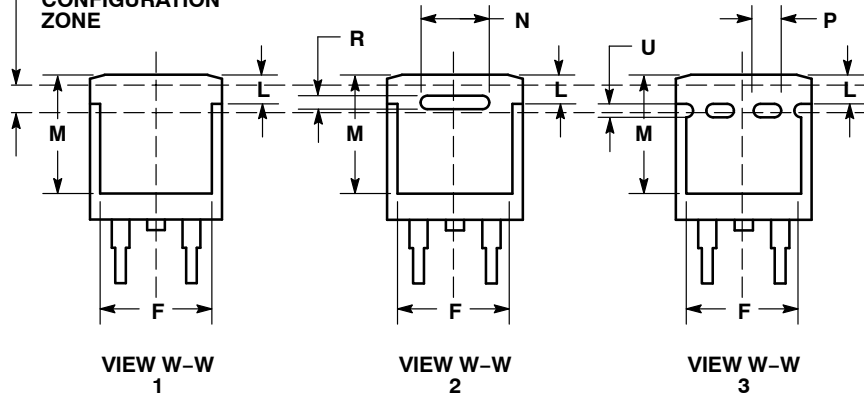
SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

VARIABLE CONFIGURATION ZONE



- |                                                                       |                                                              |                                                                  |                                                                       |                                                                  |                                                                       |
|-----------------------------------------------------------------------|--------------------------------------------------------------|------------------------------------------------------------------|-----------------------------------------------------------------------|------------------------------------------------------------------|-----------------------------------------------------------------------|
| STYLE 1:<br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | STYLE 2:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN | STYLE 3:<br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | STYLE 4:<br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | STYLE 5:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE | STYLE 6:<br>PIN 1. NO CONNECT<br>2. CATHODE<br>3. ANODE<br>4. CATHODE |
|-----------------------------------------------------------------------|--------------------------------------------------------------|------------------------------------------------------------------|-----------------------------------------------------------------------|------------------------------------------------------------------|-----------------------------------------------------------------------|

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**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

**GENERIC  
MARKING DIAGRAM\***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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