# STD130N6F7

## N-channel 60 V, 4.2 mΩ typ., 80 A STripFET™ F7 Power MOSFET in a DPAK package

Datasheet - production data

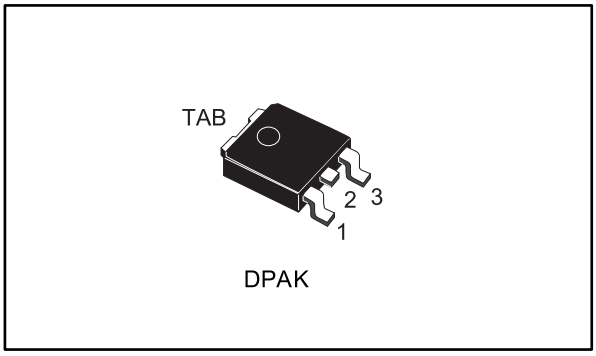
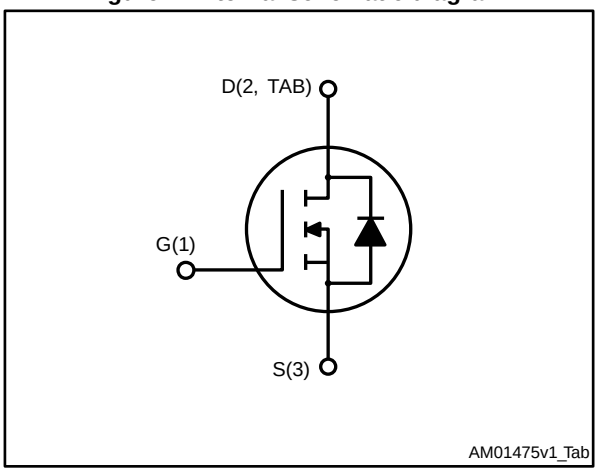



**Figure 1: Internal schematic diagram**




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ | $P_{TOT}$ |
|---|---|---|---|---|
| STD130N6F7 | 60 V | 5.0 mΩ | 80 A | 134 W |

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low $C_{rss}/C_{iss}$ ratio for EMI immunity
- High avalanche ruggedness

## Applications

- Switching applications

## Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

**Table 1: Device summary**

| Order code | Marking | Package | Packing |
|---|---|---|---|
| STD130N6F7 | 130N6F7 | DPAK | Tape and reel |



This is information on a product in full production.

# Contents

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 60 | V |
| $V_{GS}$ | Gate-source voltage | ±20 | V |
| $I_D$(1) | Drain current (continuous) at $T_{case}$ = 25 °C | 80 | A |
| | Drain current (continuous) at $T_{case}$ = 100 °C | 80 | |
| $I_{DM}$(2) | Drain current (pulsed) | 320 | A |
| $P_{TOT}$ | Total dissipation at $T_{case}$ = 25 °C | 134 | W |
| $E_{AS}$(3) | Single pulse avalanche energy | 200 | mJ |
| dV/dt(4) | Drain-body diode dynamic dV/dt ruggedness | 5.0 | V/ns |
| $T_{stg}$ | Storage temperature range | -55 to 175 | °C |
| $T_j$ | Operating junction temperature range | | |

**Notes:**

(1) Current is limited by package.

(2) Pulse width is limited by safe operating area.

(3) starting $T_j$ = 25 °C, $I_D$ = 20 A, $V_{DD}$ = 30 V.

(4)$I_{SD}$= 80 A; di/dt = 600 A/µs; $V_{DD}$ = 48 V; $T_j < T_{jmax}$

**Table 3: Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}pcb}$(1) | Thermal resistance junction-pcb | 50 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient | 1.12 | |

**Notes:**

(1)When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 sec

# 2 Electrical characteristics

($T_{case}$ = 25 °C unless otherwise specified)

**Table 4: Static**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 60 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 60 V | | | 1 | µA |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = 20 V | | | 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 40 A | | 4.2 | 5.0 | mΩ |

**Table 5: Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 30 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 2600 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 1200 | - | |
| $C_{rss}$ | Reverse transfer capacitance | | - | 115 | - | |
| $Q_g$ | Total gate charge | $V_{DD}$ = 30 V, $I_D$ = 80 A, $V_{GS}$ = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*) | - | 42 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 13.6 | - | |
| $Q_{gd}$ | Gate-drain charge | | - | 13 | - | |

**Table 6: Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 30 V, $I_D$ = 40 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*) | - | 24 | - | ns |
| $t_r$ | Rise time | | - | 44 | - | |
| $t_{d(off)}$ | Turn-off delay time | | - | 62 | - | |
| $t_f$ | Fall time | | - | 24 | - | |

**Table 7: Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SD}$ (1) | Forward on voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 80 A | - | | 1.2 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 80 A, di/dt = 100 A/µs, $V_{DD}$ = 48 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*) | - | 50 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 56 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 2.2 | | A |

**Notes:**

(1) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

**Figure 2: Safe operating area**

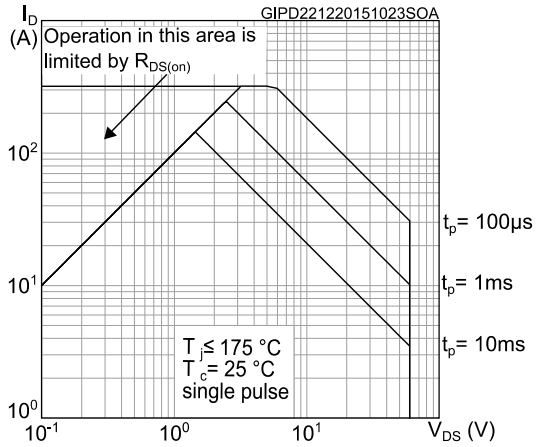



**Figure 3: Thermal impedance**

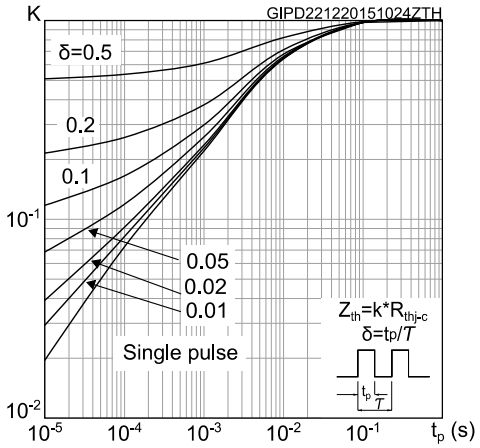



**Figure 4: Output characteristics**

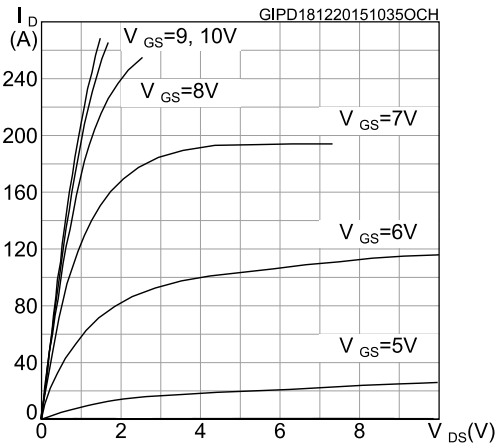



**Figure 5: Transfer characteristics**

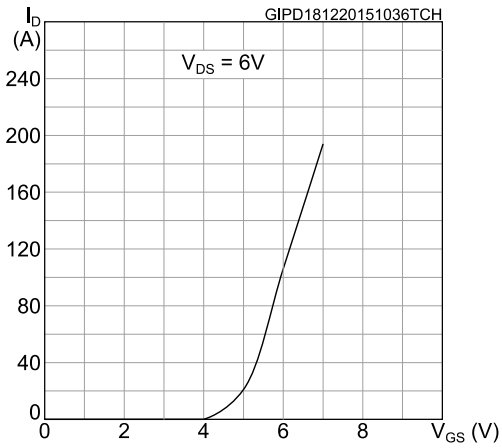



**Figure 6: Gate charge vs gate-source voltage**

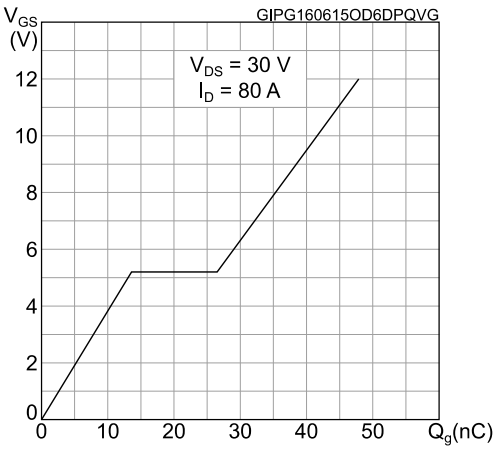



**Figure 7: Static drain-source on-resistance**

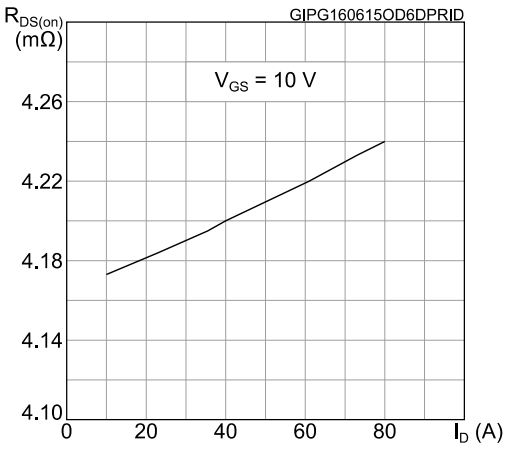


**Figure 8: Capacitance variations**

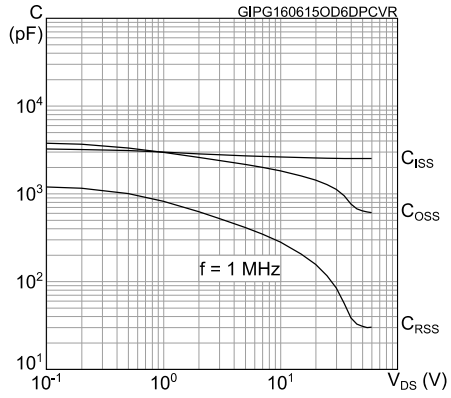



**Figure 9: Normalized gate threshold voltage vs temperature**

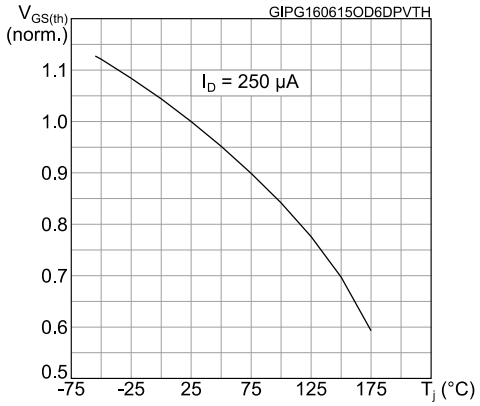



**Figure 10: Normalized on-resistance vs temperature**

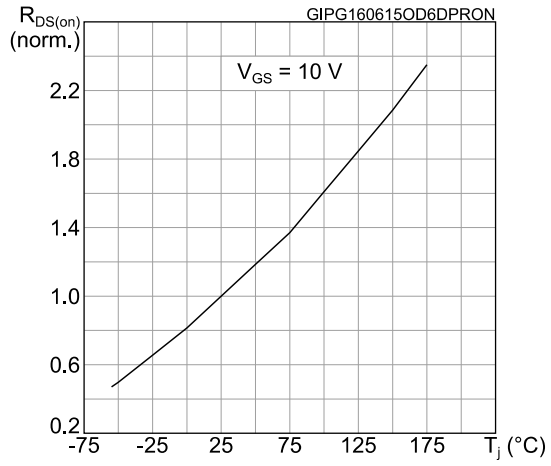



**Figure 11: Normalized V(BR)DSS vs temperature**

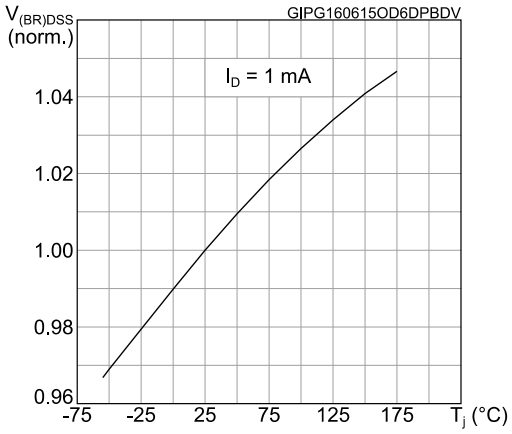
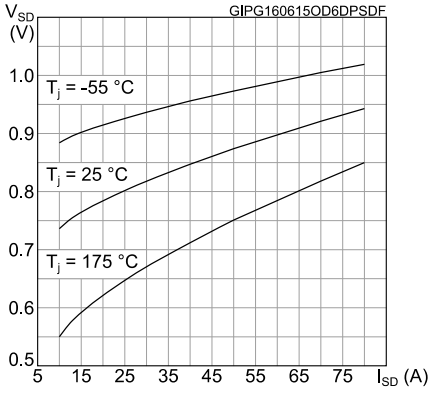



**Figure 12: Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**

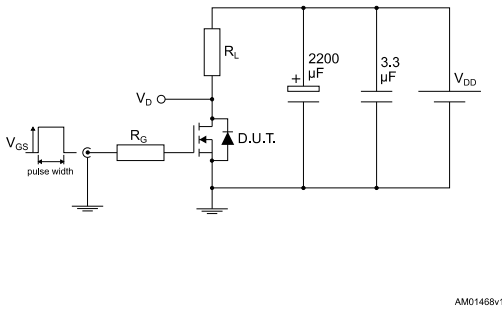



**Figure 14: Test circuit for gate charge behavior**

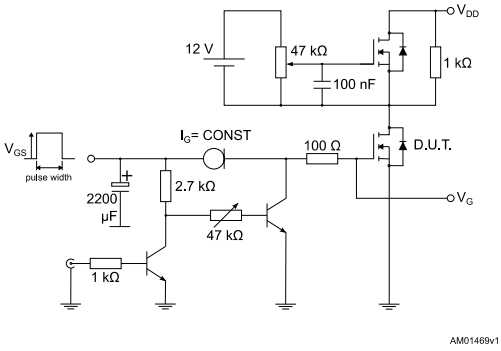



**Figure 15: Test circuit for inductive load switching and diode recovery times**

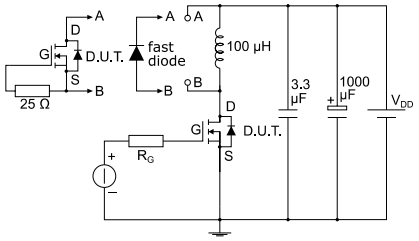



**Figure 16: Unclamped inductive load test circuit**

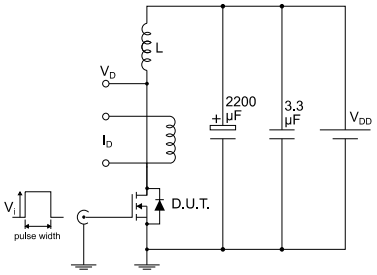



**Figure 17: Unclamped inductive waveform**

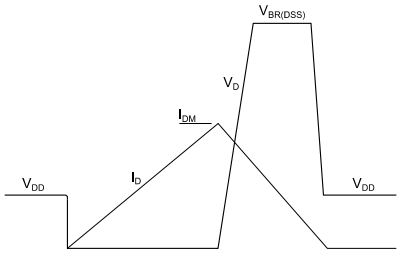
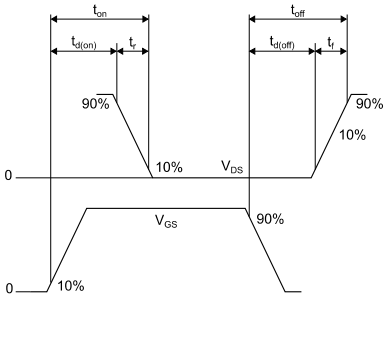



**Figure 18: Switching time waveform**



# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 4.1 DPAK package information

Figure 19: DPAK (TO-252) type A2 package outline

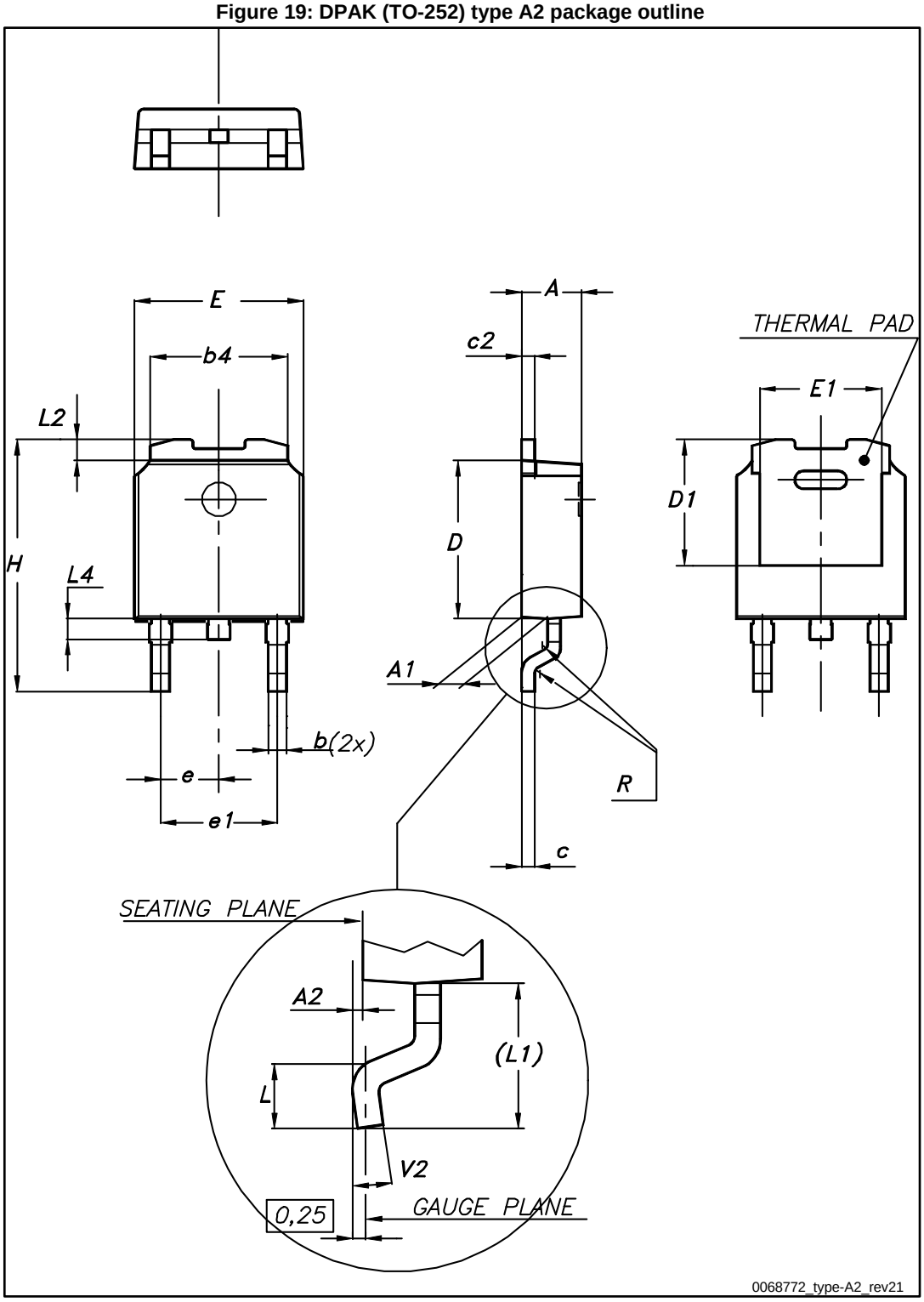
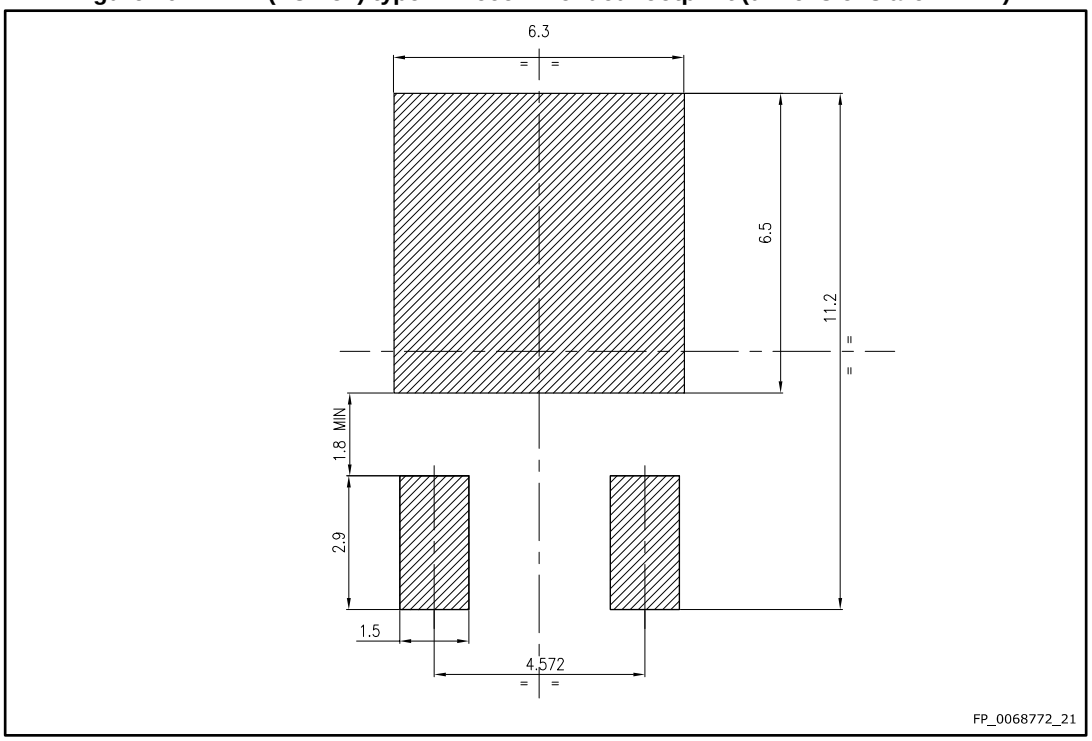


Table 8: DPAK (TO-252) type A2 mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.20 | | 2.40 |
| A1 | 0.90 | | 1.10 |
| A2 | 0.03 | | 0.23 |
| b | 0.64 | | 0.90 |
| b4 | 5.20 | | 5.40 |
| c | 0.45 | | 0.60 |
| c2 | 0.48 | | 0.60 |
| D | 6.00 | | 6.20 |
| D1 | 4.95 | 5.10 | 5.25 |
| E | 6.40 | | 6.60 |
| E1 | 5.10 | 5.20 | 5.30 |
| e | 2.16 | 2.28 | 2.40 |
| e1 | 4.40 | | 4.60 |
| H | 9.35 | | 10.10 |
| L | 1.00 | | 1.50 |
| L1 | 2.60 | 2.80 | 3.00 |
| L2 | 0.65 | 0.80 | 0.95 |
| L4 | 0.60 | | 1.00 |
| R | | 0.20 | |
| V2 | 0° | | 8° |

**Figure 20: DPAK (TO-252) type A2 recommended footprint (dimensions are in mm)**



# 5 Revision history

Table 9: Document revision history

| Date | Revision | Changes |
|---|---|---|
| 17-Dec-2015 | 1 | First release. |
| 10-Oct-2016 | 2 | Document status changed from preliminary to production data.<br>Minor text changes. |

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