



# STW54NM65ND

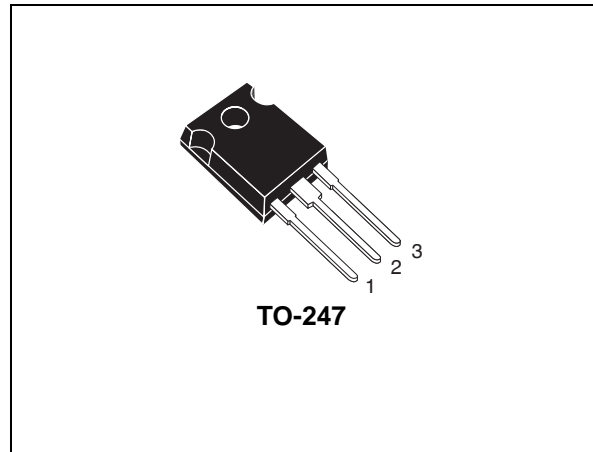
N-channel 650 V, 0.055  $\Omega$  typ., 49 A FDmesh™ II  
Power MOSFET (with fast diode) in a TO-247 package

Datasheet — production data

## Features

Order code	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STW54NM65ND	710 V	< 0.065 $\Omega$	49 A

- The worldwide best R<sub>DS(on)</sub> \* area amongst the fast recovery diode devices
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Extremely high dv/dt and avalanche capabilities



## Application

Switching applications

## Description

The device is an N-channel FDmesh™ II Power MOSFET that belongs to the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout and associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode. It is therefore strongly recommended for bridge topologies, in particular ZVS phase-shift converters.

Figure 1. Internal schematic diagram

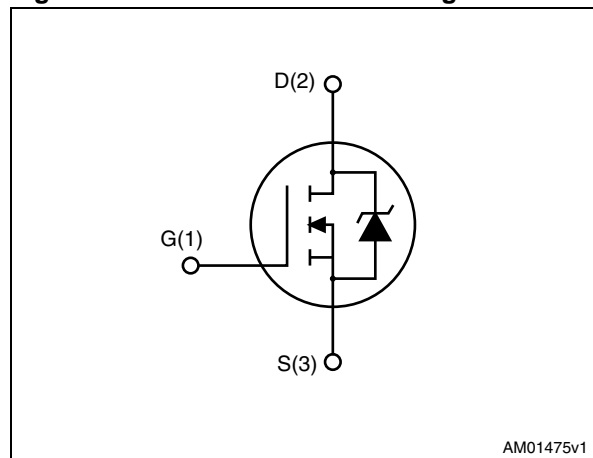


Table 1. Device summary

Order code	Marking	Package	Packaging
STW54NM65ND	54NM65ND	TO-247	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate- source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	49	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	31	A
$I_{DM}^{(1)}$	Drain current (pulsed)	196	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	350	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	40	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 49\text{ A}$ ,  $di/dt \leq 600\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.36	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	15	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	850	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	650			V
$dv/dt^{(1)}$	Drain source voltage slope	$V_{DD} = 480\text{ V}, I_D = 49\text{ A}, V_{GS} = 10\text{ V}$		30		V/ns
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			10 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 24.5\text{ A}$		0.055	0.065	$\Omega$

1. Characteristic value at turn off on inductive load.

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{ISS}$	Input capacitance			6200		pF
$C_{OSS}$	Output capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	218	-	pF
$C_{RSS}$	Reverse transfer capacitance			10		pF
$C_{OSS\text{ eq.}}^{(1)}$	Output equivalent capacitance	$V_{DS}=0\text{ to }200\text{ V } V_{GS}=0$	-	850	-	pF
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 49\text{ A}, V_{GS} = 10\text{ V},$ (see <a href="#">Figure 14</a> )	-	188	-	nC
$Q_{gs}$	Gate-source charge			32		nC
$Q_{gd}$	Gate-drain charge			100		nC
$t_c$	Crossing time	$V_{DD} = 520\text{ V}, I_D = 49\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$		33		ns
$t_r$	Rise time			59		ns
$t_{d(off)}$	Turn-off delay time	(see <a href="#">Figure 17</a> ),		152		ns
$t_f$	Fall time	(see <a href="#">Figure 13</a> )		98		ns
$R_g$	Gate input resistance	$f=1\text{ MHz}$ gate DC bias=0 Test signal level = 20 mV open drain	-	1.9	-	$\Omega$

1.  $C_{OSS\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{OSS}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DS}$ .

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		49	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		196	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 49\text{ A}, V_{GS} = 0$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 49\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	212		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	<i>Figure 15</i>	-	19		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 49\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	296		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}, T_j = 150\text{ }^\circ\text{C}$	-	4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	<i>Figure 15</i>	-	28		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

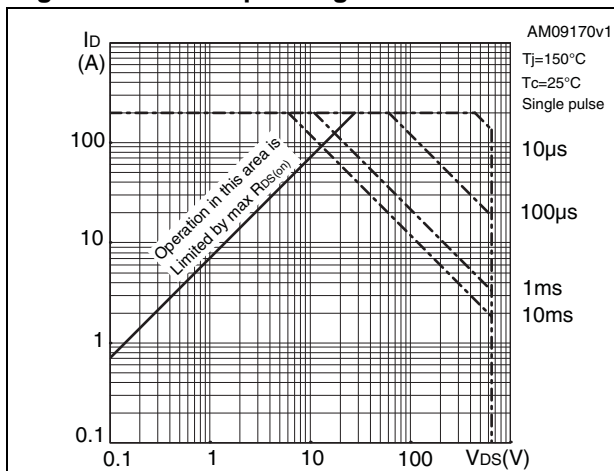


Figure 3. Thermal impedance

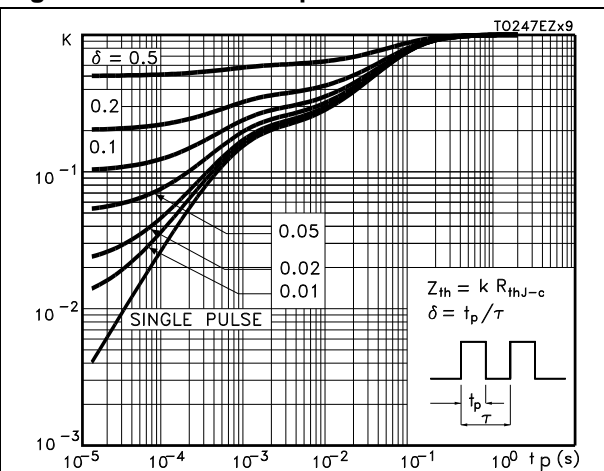


Figure 4. Output characteristics

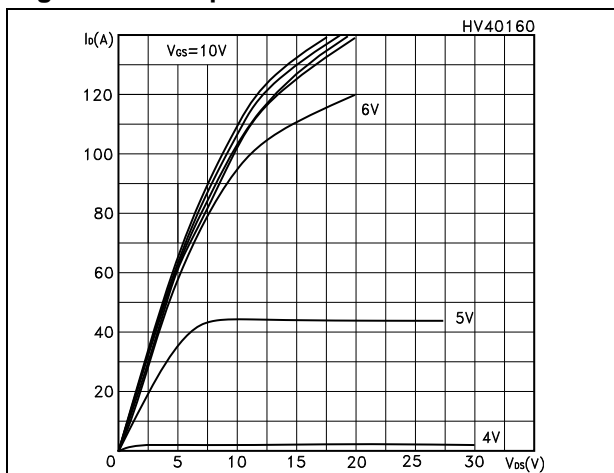


Figure 5. Transfer characteristics

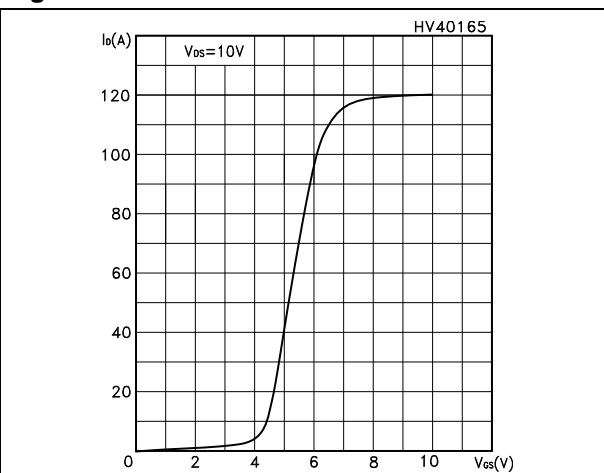


Figure 6. Normalized B<sub>V</sub>DSS vs temperature

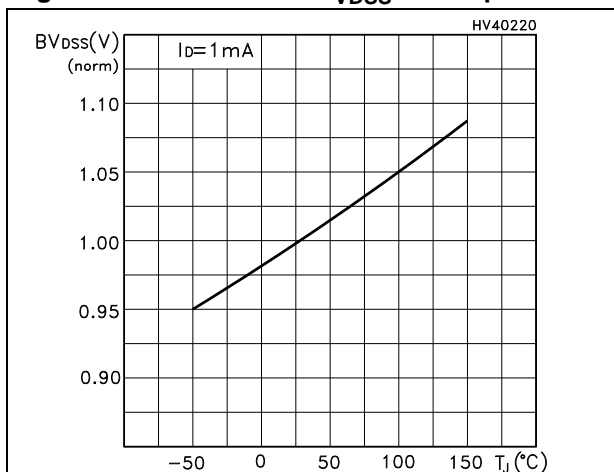


Figure 7. Static drain-source on-resistance

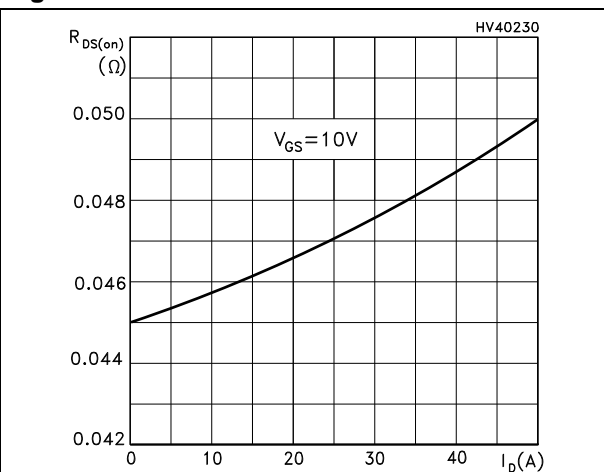


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

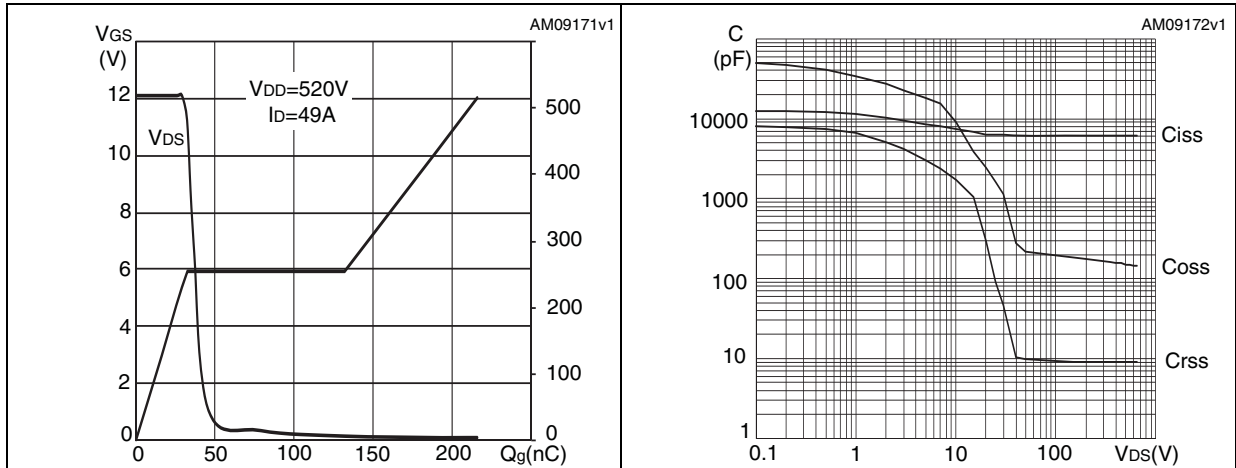


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

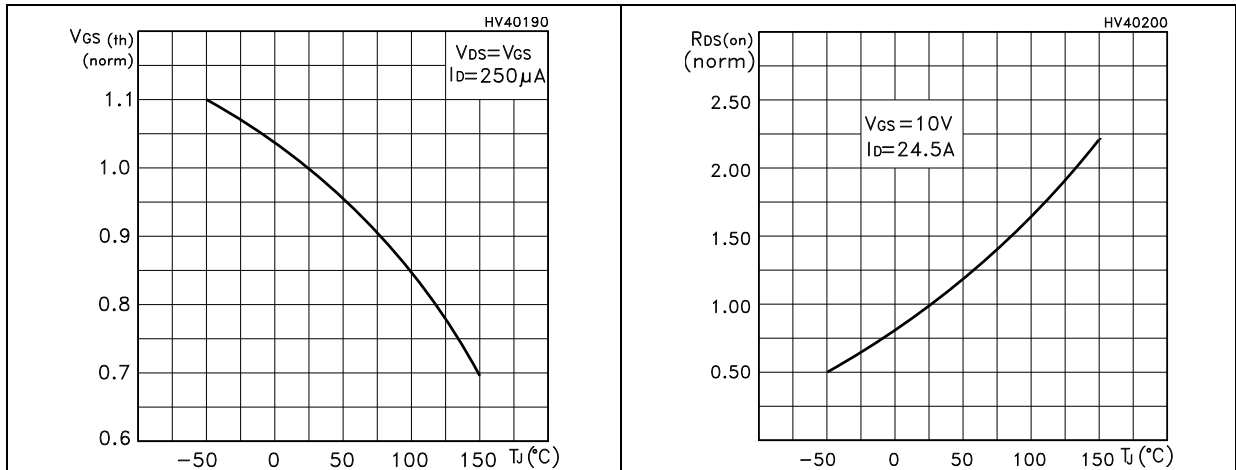
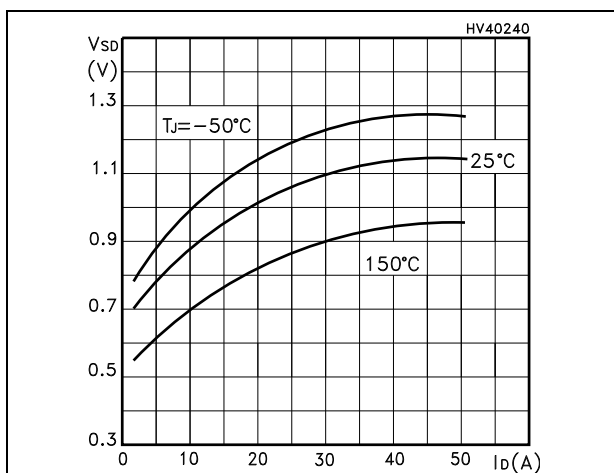


Figure 12. Source-drain diode forward characteristics

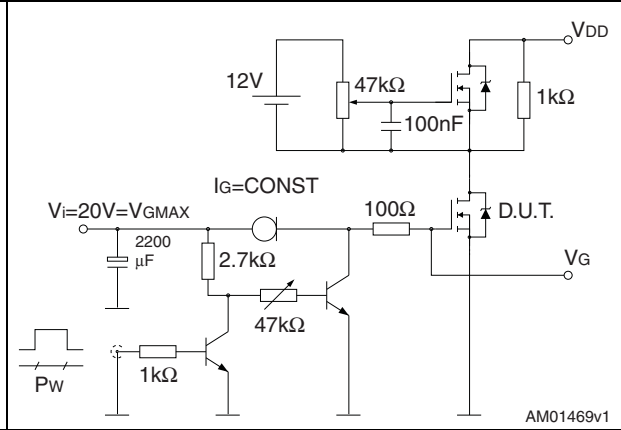


### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**



**Figure 14. Gate charge test circuit**



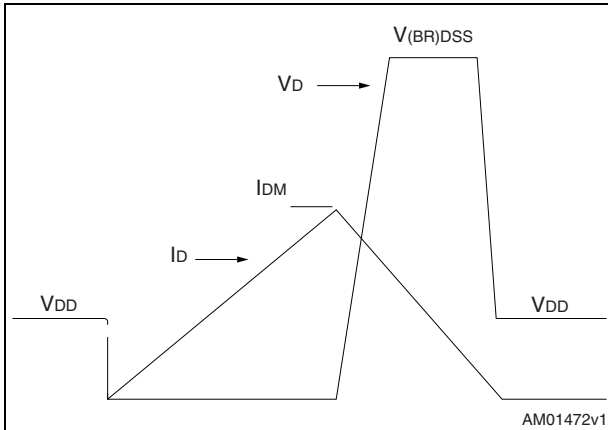
**Figure 15. Test circuit for inductive load switching and diode recovery times**



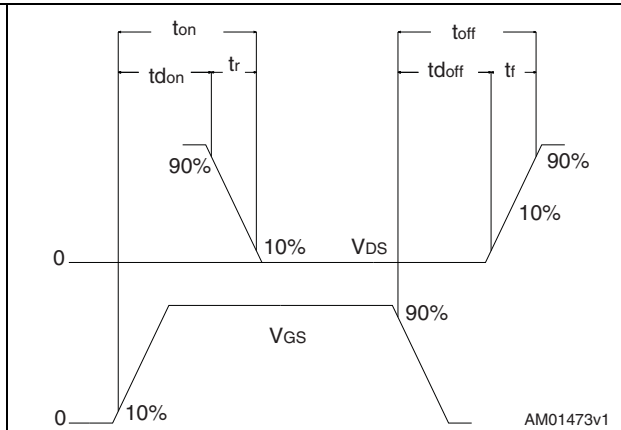
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**





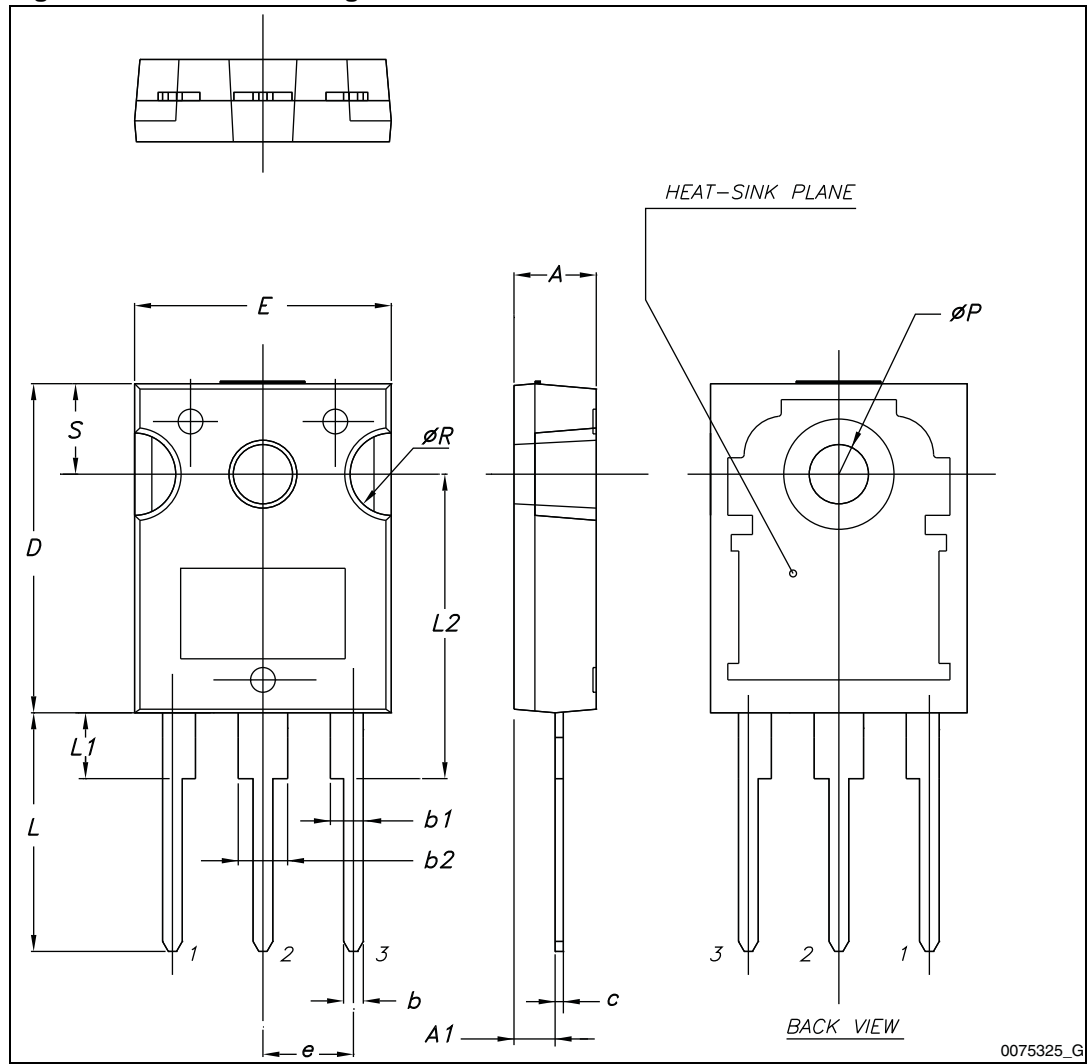
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

Table 8. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 19. TO-247 drawing



0075325\_G

## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
03-Jun-2011	1	Initial release
19-Dec-2012	2	Updated title on the cover page. Inserted dv/dt parameter in <a href="#">Table 5</a> . Updated <a href="#">Section 4: Package mechanical data</a> .

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