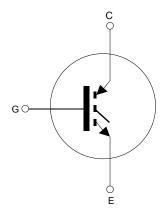


Trench gate field-stop 650 V, 30 A low-loss M series IGBT die in D7 packing



Features

- 6 µs of minimum short-circuit withstand time
- $V_{CE(sat)} = 1.55 \text{ V (typ.)} @ I_C = 30 \text{ A}$
- Positive V_{CE(sat)} temperature coefficient
- · Tight parameter distribution
- Maximum junction temperature: T_J = 175 °C

Applications

- Motor control
- PFC
- UPS

EGCD

· General purpose inverter

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the M series IGBTs, which represent an optimal balance between inverter system performance and efficiency where low-loss and short-circuit functionality are essential. Furthermore, the positive $V_{\text{CE(sat)}}$ temperature coefficient and tight parameter distribution result in safer paralleling operation.

Product status	
STG30M65F2D7	

Device summary							
Order code STG30M65F2D7							
V _{CE}	650 V						
I _{CN}	30 A						
Die size	3.6 x 4.6 mm ²						
Packing	D7						



1 Mechanical parameters

Table 1. Mechanical parameters

Symbol		Value	Unit	
Die size including scrib	e line	3.6 x 4.6	mm²	
Wafer size		200	mm	
Maximum possible dice p	er wafer	1592	dice	
Die thickness		70	μm	
Front side passivati	on	Silicon nitrio	le	
Emitter pad size including	Emitter pad size including gate pad		mm²	
Gate pad size		0.45 x 0.45	mm²	
Front side metallization	composition	AlCu		
Front side metanization	thickness	4.5	μm	
Back side metallization	composition	AI/Ti/NiV/Ag		
Dack side Metallization	thickness	0.65	μm	
Die bond	Die bond		e or soft solder	
Recommended wire bo	Recommended wire bonding		μm	



2 Electrical ratings

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings (T_J = 25 °C unless otherwise specified)

Symbol		Parameter	Value	Unit	
V _{CES}	Collector-emitter voltage (V _{GE} = 0 V)			V	
V _{GE}	Gate-emitter voltage	Gate-emitter voltage			
I _{CN} (1)	Continuous collector current at T = 100 °C			Α	
I _{CP} (2) (1)	Pulsed collector current			Α	
+ (3)	Short -circuit withstand time	V_{CC} = 400 V, V_{GE} = 15 V, $V_{CE(peak)}$ ≤ 650 V, T_{Jstart} ≤ 150 °C	6	μs	
t _{SC} (3)	V _{CC} = 400 V, V _{GE} = 13 V, V _{CE(peak)} \leq 650 V, T _{Jstart} \leq 150 °C		10	μs	
TJ	Operating junction temperature range			°C	

Nominal collector current for die packaged in ST discrete solution. Current level depends on the assembly thermal properties and is limited by maximum junction temperature.

2.2 Electrical characteristics

Table 3. Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)CES}	Collector-emitter breakdown voltage	I _C = 250 mA, V _{GE} = 0 V	650			V
V _{CE(sat)}	Collector-emitter saturation voltage	V _{GE} = 15 V, I _C = 15 A			1.9	V
V _{GE(th)}	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 500 \mu A$	5	6	7	V
I _{CES}	Collector cut-off current	V _{GE} = 0 V, V _{CE} = 650 V			25	μΑ
I _{GES}	Gate-emitter leakage current	V _{CE} = 0 V, V _{GE} = ±20 V			±250	μΑ

Table 4. Electrical characteristics (not tested at chip level, verified by design/characterization)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
VCE(cot)	Collector-emitter saturation voltage	V _{GE} = 15 V, I _C = 30 A	-	1.55	2.00	V
		V_{GE} = 15 V, I_{C} = 30 A, T_{J} = 175 °C	-	2.10		V
C _{ies}	Input capacitance	V _{CE} = 25 V, f = 1 MHz, V _{GE} = 0 V	-	2490		pF
C _{oes}	Output capacitance		-	143		pF
C _{res}	Reverse transfer capacitance	VGE VV	-	46		pF

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^{2.} Pulse width is limited by maximum junction temperature.

^{3.} Not tested at chip level, verified by design/characterization.



Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Qg	Total gate charge	V_{CC} = 520 V, I_{C} = 30 A, V_{GE} = 0 to 15 V	-	80		nC

Table 5. Switching characteristics on inductive load

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$t_{d(on)}$	Turn-on delay time		-	31.6	-	ns
t _r	Current rise time	V = 400 V I = 30 A	-	13.4	-	ns
t _{d(off)}	Turn-off-delay time	$V_{CC} = 400 \text{ V}, I_{C} = 30 \text{ A},$ $V_{GE} = 15 \text{ V}, R_{G} = 10 \Omega$	-	115	-	ns
t _f	Current fall time	VGE = 13 V, NG = 10 12	-	110	-	ns
E _{off} (1)	Turn-off switching energy		-	0.96	-	mJ
t _{d(on)}	Turn-on delay time		-	30	-	ns
t _r	Current rise time	V _{CC} = 400 V, I _C = 30 A,	-	17	-	ns
t _{d(off)}	Turn-off-delay time	V_{GE} = 15 V, R_{G} = 10 Ω , T_{J} =	-	116	-	ns
t _f	Current fall time	175 °C	-	194	-	ns
E _{off} (1)	Turn-off switching energy		-	1.36	-	mJ

^{1.} Including the tail of the collector current.

Note:

The aforementioned values are not tested at chip level and are strongly dependent on the package/module design and the mounting technology. Refer to STGWA30M65DF2 datasheet for further information.



3 Die layout

3.60 E 3.93 4.60 0.22 - 2.92

Figure 1. Die drawing (dimensions are in mm)

Table 6. Die delivery

GADG031120171015SA

Package option	Description	Details
D7	Wafer tested, inked, cut on sticky foil on 10.8" (276 mm) ring (see Figure 2. D7 drawing and die orientation)	Wafer is held by ring protected by two carton shells, inside a plastic envelope sealed under vacuum. Maximum number of wafers for each package is 5, weight is about 3.7 Kg.

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Metallic ring Wafer Gate pad

Figure 2. D7 drawing and die orientation

Demonstrating picture, not in scale

GADG031120171022SA



4 Additional information

4.1 Additional testing and screening

For customers requiring product supplied as known good die (KGD) or requiring specific die level testing (i.e. for dynamic and switching characterization), please contact the local ST sales office.

If KGD is requested, the shipping delivery is D8.

4.2 Shipping

Several shipping options are offered, consult the local ST sales office for availability:

- Die on film sticky foil suffix on sales type D7
- · Carrier tape suffix on sales type D8

4.3 Handling

- Products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- · Products must be handled only in a class 1000 or better-designated clean room environment.
- Singular die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

4.4 Wafer/die storage

Once the packaging is opened, the wafer must be stored in a dry, inert atmosphere, such as nitrogen. Optimum temperature for storage is $18 \,^{\circ}\text{C} \pm 2 \,^{\circ}\text{C}$ with as few variations as possible to avoid parasitic polymerization of the adhesive. Sawn wafers must be processed within 12 weeks after receipt by customer. After the customer opens the package, the customer is responsible for the products.

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Revision history

Table 7. Document revision history

Date	Revision	Changes
03-Nov-2017	1	Initial release
		Removed maturity status indication from cover page. The document status is production data. Modified title and features on cover page.
13-Apr-2018	2	Modified Table 3. Static characteristics (tested on wafer unless otherwise specified), Table 4. Electrical characteristics (not tested at chip level, verified by design/characterization) and Table 6. Die delivery.
		Minor text changes.

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