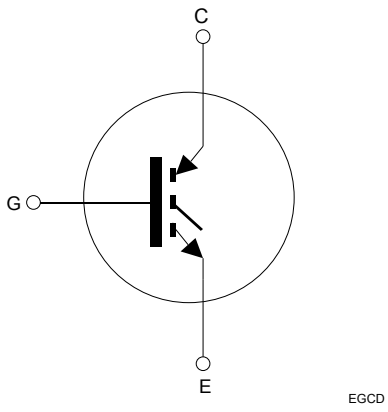
STG30M65F2D7

Datasheet

Trench gate field-stop 650 V, 30 A low-loss M series IGBT die in D7 packing



Features

- 6 µs of minimum short-circuit withstand time
- $V_{CE(sat)}$ = 1.55 V (typ.) @ I_C = 30 A
- Positive $V_{CE(sat)}$ temperature coefficient
- Tight parameter distribution
- Maximum junction temperature: T_J = 175 °C

Applications

- Motor control
- PFC
- UPS
- General purpose inverter

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the M series IGBTs, which represent an optimal balance between inverter system performance and efficiency where low-loss and short-circuit functionality are essential. Furthermore, the positive $V_{CE(sat)}$ temperature coefficient and tight parameter distribution result in safer paralleling operation.

Product status
STG30M65F2D7

Device summary	
Order code	STG30M65F2D7
V_{CE}	650 V
I_{CN}	30 A
Die size	3.6 x 4.6 mm²
Packing	D7

1 Mechanical parameters

Table 1. Mechanical parameters

Symbol		Value	Unit
Die size including scribe line		3.6 x 4.6	mm²
Wafer size		200	mm
Maximum possible dice per wafer		1592	dice
Die thickness		70	µm
Front side passivation		Silicon nitride	
Emitter pad size including gate pad		2.92 x 3.93	mm²
Gate pad size		0.45 x 0.45	mm²
Front side metallization	composition	AlCu	
	thickness	4.5	µm
Back side metallization	composition	Al/Ti/NiV/Ag	
	thickness	0.65	µm
Die bond		Electrically conductive glue or soft solder	
Recommended wire bonding		≤500	µm

2 Electrical ratings

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings (T_J = 25 °C unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0 V)		650	V
V_{GE}	Gate-emitter voltage		±20	V
I_{CN} (1)	Continuous collector current at T = 100 °C		30	A
I_{CP} (2) (1)	Pulsed collector current		90	A
t_{SC} (3)	Short -circuit withstand time	V_{CC} = 400 V, V_{GE} = 15 V, $V_{CE(peak)}$ ≤ 650 V, T_{Jstart} ≤ 150 °C	6	µs
		V_{CC} = 400 V, V_{GE} = 13 V, $V_{CE(peak)}$ ≤ 650 V, T_{Jstart} ≤ 150 °C	10	µs
T_J	Operating junction temperature range		-55 to 175	°C

1. *Nominal collector current for die packaged in ST discrete solution. Current level depends on the assembly thermal properties and is limited by maximum junction temperature.*
2. *Pulse width is limited by maximum junction temperature.*
3. *Not tested at chip level, verified by design/characterization.*

2.2 Electrical characteristics

Table 3. Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	I_C = 250 mA, V_{GE} = 0 V	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 15 A			1.9	V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 500 µA	5	6	7	V
I_{CES}	Collector cut-off current	V_{GE} = 0 V, V_{CE} = 650 V			25	µA
I_{GES}	Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = ±20 V			±250	µA

Table 4. Electrical characteristics (not tested at chip level, verified by design/characterization)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 30 A	-	1.55	2.00	V
		V_{GE} = 15 V, I_C = 30 A, T_J = 175 °C	-	2.10		V
C_{ies}	Input capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE} = 0 V	-	2490		pF
C_{oes}	Output capacitance		-	143		pF
C_{res}	Reverse transfer capacitance		-	46		pF

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Q_g	Total gate charge	V_{CC} = 520 V, I_C = 30 A, V_{GE} = 0 to 15 V	-	80		nC

Table 5. Switching characteristics on inductive load

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{CC} = 400 V, I_C = 30 A, V_{GE} = 15 V, R_G = 10 Ω	-	31.6	-	ns
t_r	Current rise time		-	13.4	-	ns
$t_{d(off)}$	Turn-off-delay time		-	115	-	ns
t_f	Current fall time		-	110	-	ns
E_{off} (1)	Turn-off switching energy		-	0.96	-	mJ
$t_{d(on)}$	Turn-on delay time	V_{CC} = 400 V, I_C = 30 A, V_{GE} = 15 V, R_G = 10 Ω, T_J = 175 °C	-	30	-	ns
t_r	Current rise time		-	17	-	ns
$t_{d(off)}$	Turn-off-delay time		-	116	-	ns
t_f	Current fall time		-	194	-	ns
E_{off} (1)	Turn-off switching energy		-	1.36	-	mJ

1. *Including the tail of the collector current.*

Note: The aforementioned values are not tested at chip level and are strongly dependent on the package/module design and the mounting technology. Refer to STGWA30M65DF2 datasheet for further information.

3 Die layout

Figure 1. **Die drawing (dimensions are in mm)**

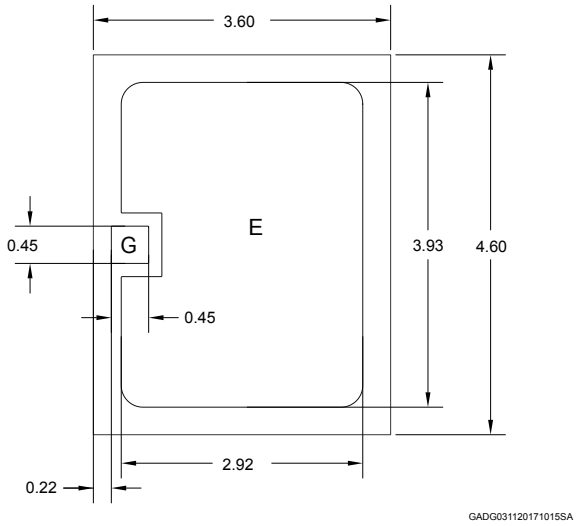
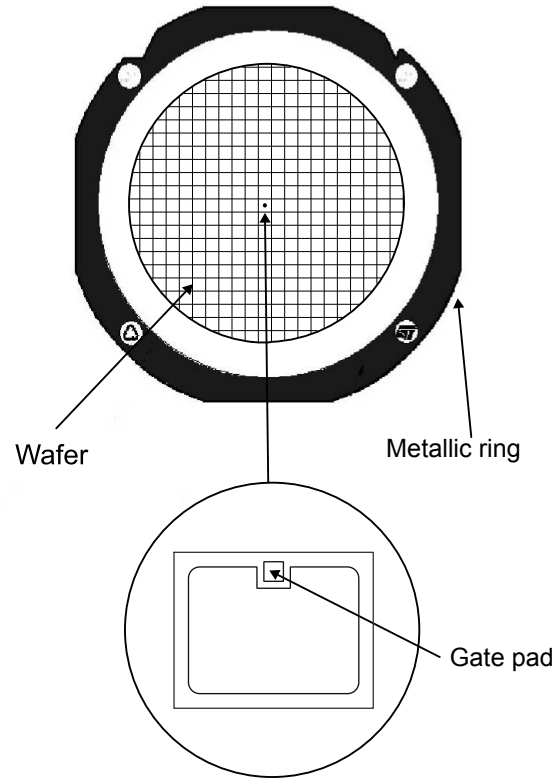


Table 6. **Die delivery**

Package option	Description	Details
D7	Wafer tested, inked, cut on sticky foil on 10.8" (276 mm) ring (see Figure 2. D7 drawing and die orientation)	Wafer is held by ring protected by two carton shells, inside a plastic envelope sealed under vacuum. Maximum number of wafers for each package is 5, weight is about 3.7 Kg.

Figure 2. D7 drawing and die orientation



Demonstrating picture, not in scale

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4 Additional information

4.1 Additional testing and screening

For customers requiring product supplied as known good die (KGD) or requiring specific die level testing (i.e. for dynamic and switching characterization), please contact the local ST sales office.

If KGD is requested, the shipping delivery is D8.

4.2 Shipping

Several shipping options are offered, consult the local ST sales office for availability:

- Die on film sticky foil - suffix on sales type D7
- Carrier tape - suffix on sales type D8

4.3 Handling

- Products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Products must be handled only in a class 1000 or better-designated clean room environment.
- Singular die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

4.4 Wafer/die storage

Once the packaging is opened, the wafer must be stored in a dry, inert atmosphere, such as nitrogen.

Optimum temperature for storage is 18 °C ±2 °C with as few variations as possible to avoid parasitic polymerization of the adhesive. Sawn wafers must be processed within 12 weeks after receipt by customer.

After the customer opens the package, the customer is responsible for the products.

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
03-Nov-2017	1	Initial release
13-Apr-2018	2	Removed maturity status indication from cover page. The document status is production data. Modified title and features on cover page. Modified Table 3. Static characteristics (tested on wafer unless otherwise specified), Table 4. Electrical characteristics (not tested at chip level, verified by design/characterization) and Table 6. Die delivery. Minor text changes.

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