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NGTB50N60FLWG

IGBT

This Insulated Gate Bipolar Transistor (IGBT) features a robust and cost effective Trench construction, and provides superior performance in demanding switching applications, offering both low on state voltage and minimal switching loss.

Features

- Low Saturation Voltage using Trench with Field Stop Technology
- Low Switching Loss Reduces System Power Dissipation
- Soft Fast Reverse Recovery Diode
- Optimized for High Speed Switching
- 5 μs Short−Circuit Capability
- These are Pb−Free Devices

Typical Applications

- Solar Inverters
- Uninterruptible Power Supplies (UPS)

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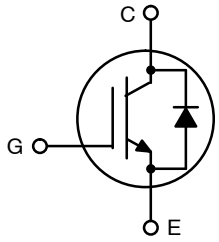
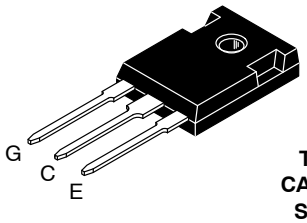
50 A, 600 V
V_{CEsat} = 1.65 V
E_{OFF} = 0.6 mJ





TO−247
CASE 340L
STYLE 4

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−emitter voltage	V_{CES}	600	V
Collector current @ Tc = 25°C @ Tc = 100°C	I_C	 100 50	A
Diode Forward Current @ Tc = 25°C @ Tc = 100°C	I_F	 100 50	A
Diode Pulsed Current T_{PULSE} Limited by T_J Max	I_{FM}	200	A
Pulsed collector current, T_{pulse} limited by T_{Jmax}	I_{CM}	200	A
Short−circuit withstand time V_{GE} = 15 V, V_{CE} = 300 V, $T_J \le$ +150°C	t_{SC}	5	μs
Gate−emitter voltage	V_{GE}	±20	V
Transient gate−emitter voltage (T_{PULSE} = 5 μs, D < 0.10)		±30	V
Power Dissipation @ Tc = 25°C @ Tc = 100°C	P_D	 223 89	W
Operating junction temperature range	T_J	−55 to +150	°C
Storage temperature range	T_{stg}	−55 to +150	°C
Lead temperature for soldering, 1/8” from case for 5 seconds	T_{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

MARKING DIAGRAM

A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
NGTB50N60FLWG	TO−247 (Pb−Free)	30 Units / Rail

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal resistance junction−to−case, for IGBT	$R_{\theta JC}$	0.56	°C/W
Thermal resistance junction−to−case, for Diode	$R_{\theta JC}$	0.74	°C/W
Thermal resistance junction−to−ambient	$R_{\theta JA}$	40	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTIC						
Collector−emitter breakdown voltage, gate−emitter short−circuited	V_{GE} = 0 V, I_C = 500 μA	$V_{(BR)CES}$	600	−	−	V
Collector−emitter saturation voltage	V_{GE} = 15 V, I_C = 50 A V_{GE} = 15 V, I_C = 50 A, T_J = 150°C	V_{CEsat}	1.40 −	1.65 1.85	1.90 −	V
Gate−emitter threshold voltage	V_{GE} = V_{CE}, I_C = 350 μA	$V_{GE(th)}$	4.5	5.5	6.5	V
Collector−emitter cut−off current, gate−emitter short−circuited	V_{GE} = 0 V, V_{CE} = 600 V V_{GE} = 0 V, V_{CE} = 600 V, T_J = 150°C	I_{CES}	− −	− −	0.5 2	mA
Gate leakage current, collector−emitter short−circuited	V_{GE} = 20 V , V_{CE} = 0 V	I_{GES}	−	−	200	nA
DYNAMIC CHARACTERISTIC						
Input capacitance	V_{CE} = 20 V, V_{GE} = 0 V, f = 1 MHz	C_{ies}	−	7500	−	pF
Output capacitance		C_{oes}	−	300	−	
Reverse transfer capacitance		C_{res}	−	190	−	
Gate charge total	V_{CE} = 480 V, I_C = 50 A, V_{GE} = 15 V	Q_g	−	310	−	nC
Gate to emitter charge		Q_{ge}	−	60	−	
Gate to collector charge		Q_{gc}	−	150	−	
SWITCHING CHARACTERISTIC, INDUCTIVE LOAD						
Turn−on delay time	T_J = 25°C V_{CC} = 400 V, I_C = 50 A R_g = 10 Ω V_{GE} = 0 V/ 15 V	$t_{d(on)}$	−	116	−	ns
Rise time		t_r	−	43	−	
Turn−off delay time		$t_{d(off)}$	−	292	−	
Fall time		t_f	−	78	−	
Turn−on switching loss		E_{on}	−	1.1	−	mJ
Turn−off switching loss		E_{off}	−	0.6	−	
Total switching loss		E_{ts}	−	1.7	−	
Turn−on delay time	T_J = 150°C V_{CC} = 400 V, I_C = 50 A R_g = 10 Ω V_{GE} = 0 V/ 15 V	$t_{d(on)}$	−	110	−	ns
Rise time		t_r	−	45	−	
Turn−off delay time		$t_{d(off)}$	−	300	−	
Fall time		t_f	−	105	−	
Turn−on switching loss		E_{on}	−	1.4	−	mJ
Turn−off switching loss		E_{off}	−	1.1	−	
Total switching loss		E_{ts}	−	2.5	−	
DIODE CHARACTERISTIC						
Forward voltage	V_{GE} = 0 V, I_F = 50 A V_{GE} = 0 V, I_F = 50 A, T_J = 150°C	V_F	1.55 −	1.85 1.85	2.1 −	V
Reverse recovery time	T_J = 25°C I_F = 50 A, V_R = 200 V di_F/dt = 200 A/μs	t_{rr}	−	85	−	ns
Reverse recovery charge		Q_{rr}	−	0.40	−	μC
Reverse recovery current		I_{rrm}	−	8	−	A

TYPICAL CHARACTERISTICS

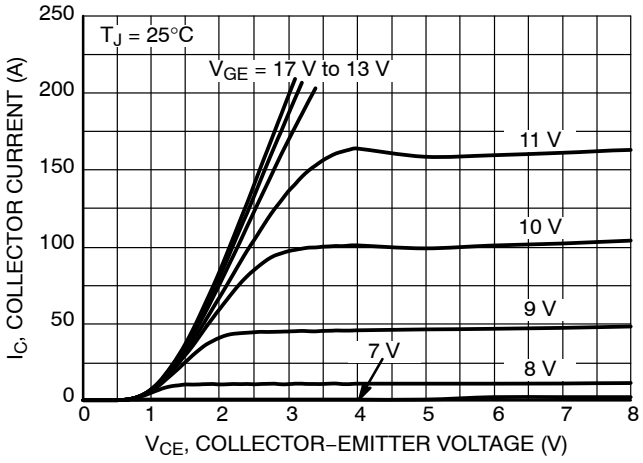


Figure 1. Output Characteristics

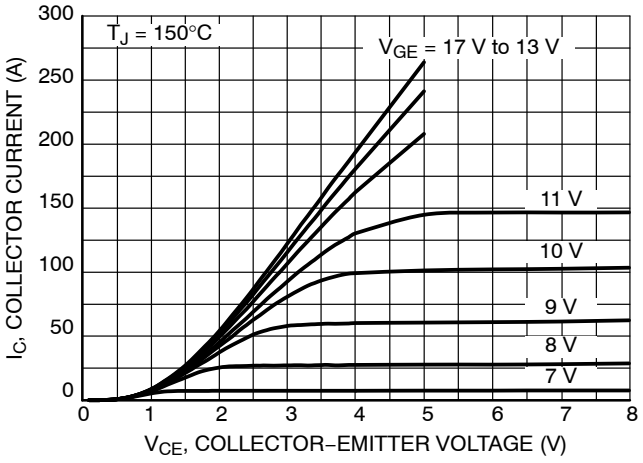


Figure 2. Output Characteristics

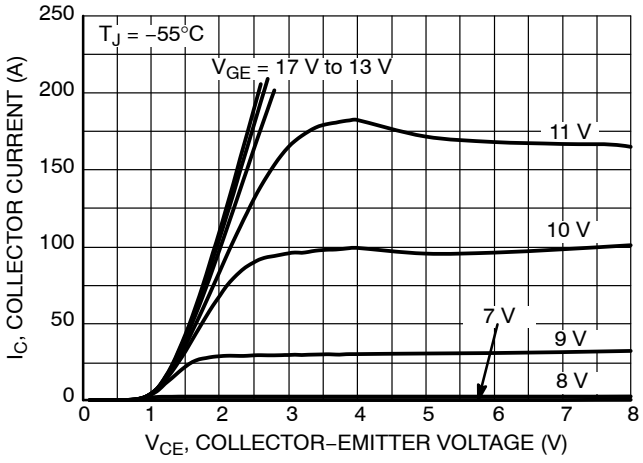


Figure 3. Output Characteristics

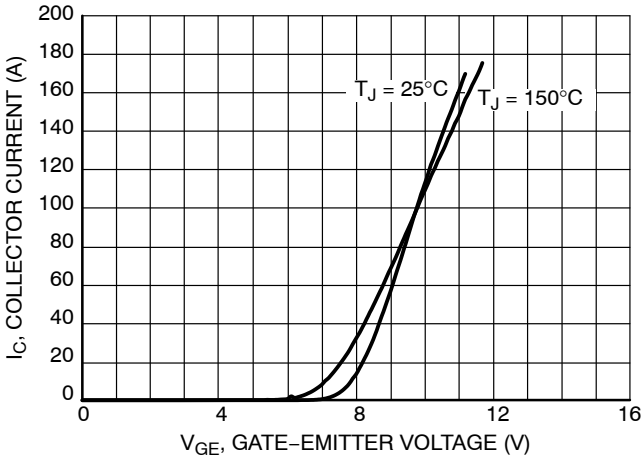


Figure 4. Typical Transfer Characteristics

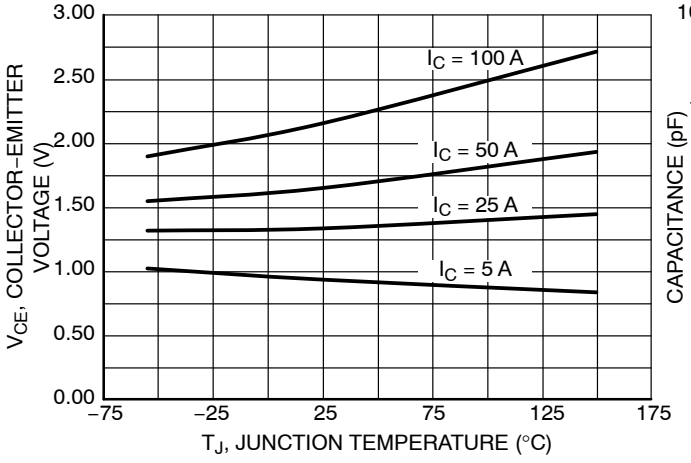


Figure 5. $V_{CE(sat)}$ vs. T_J

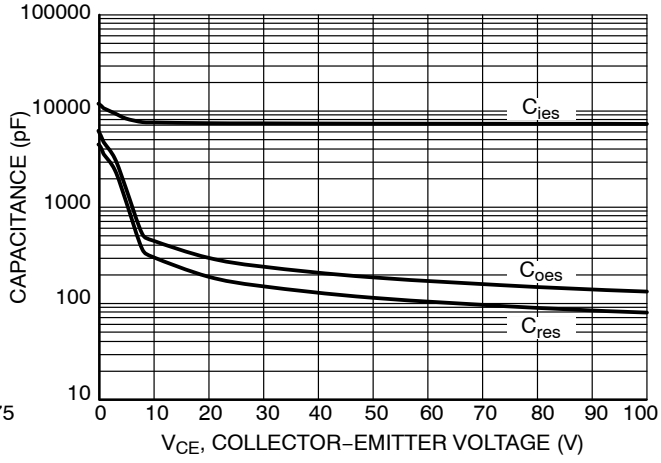


Figure 6. Typical Capacitance

TYPICAL CHARACTERISTICS

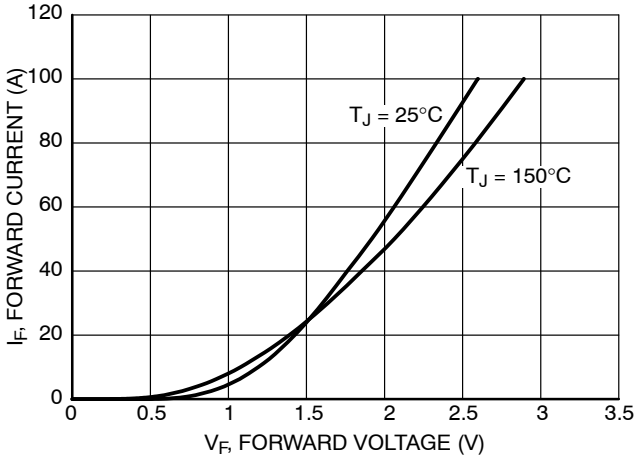


Figure 7. Diode Forward Characteristics

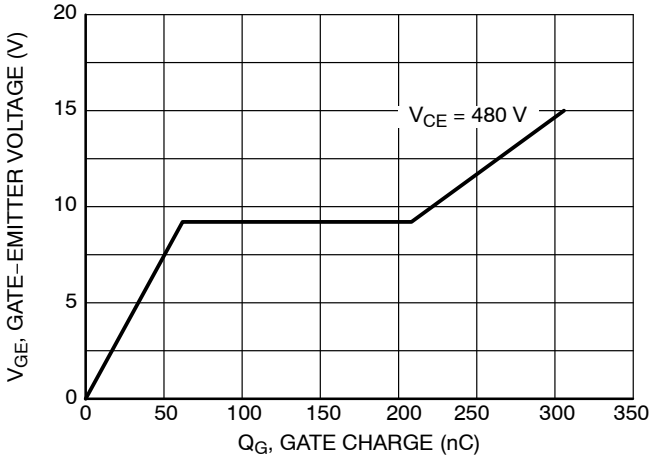


Figure 8. Typical Gate Charge

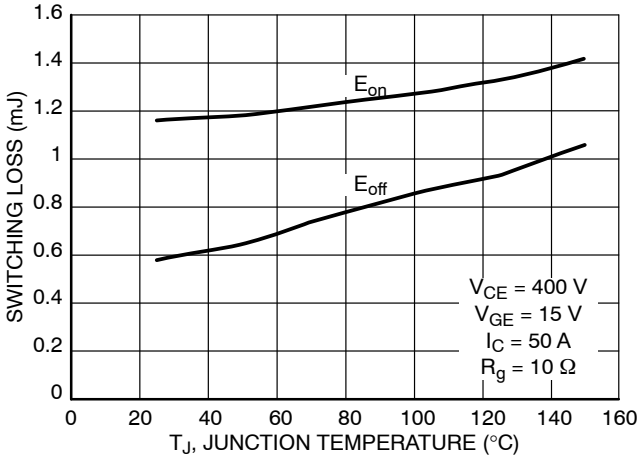


Figure 9. Switching Loss vs. Temperature

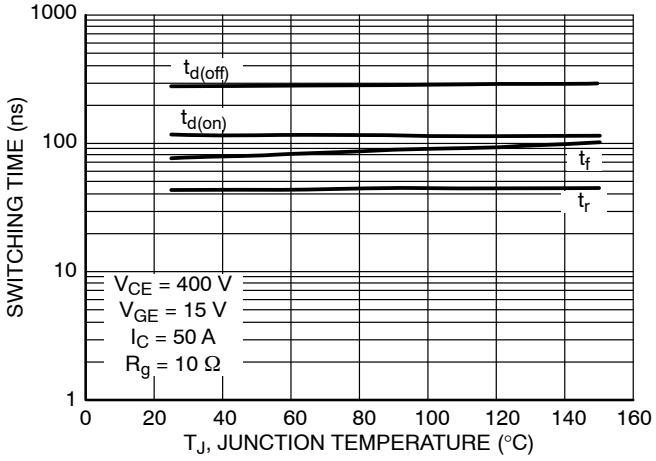


Figure 10. Switching Time vs. Temperature

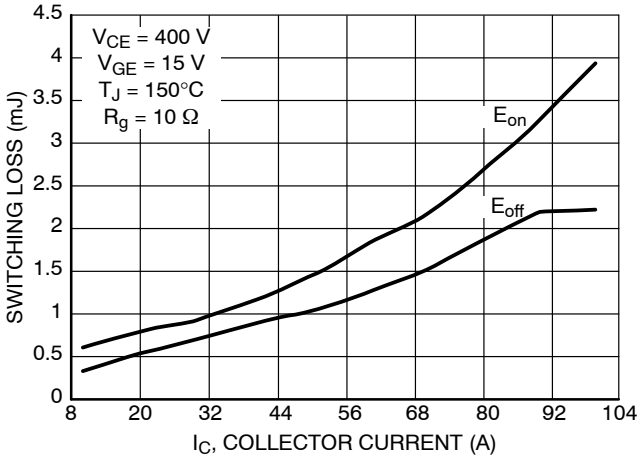


Figure 11. Switching Loss vs. I_C

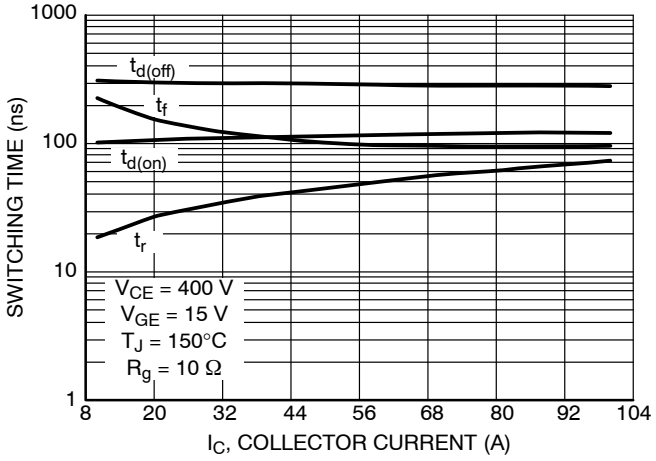


Figure 12. Switching Time vs. I_C

TYPICAL CHARACTERISTICS

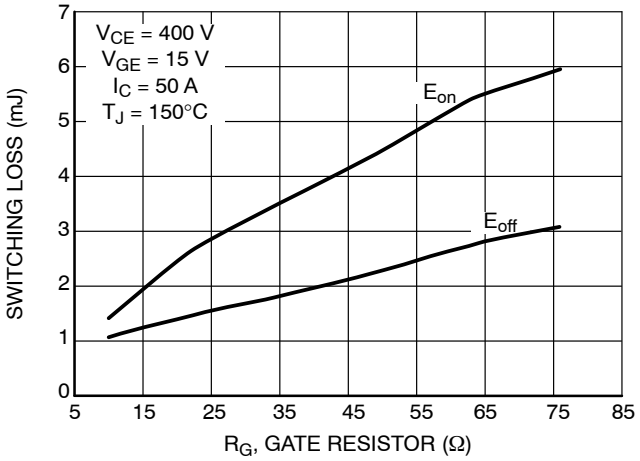


Figure 13. Switching Loss vs. R_G

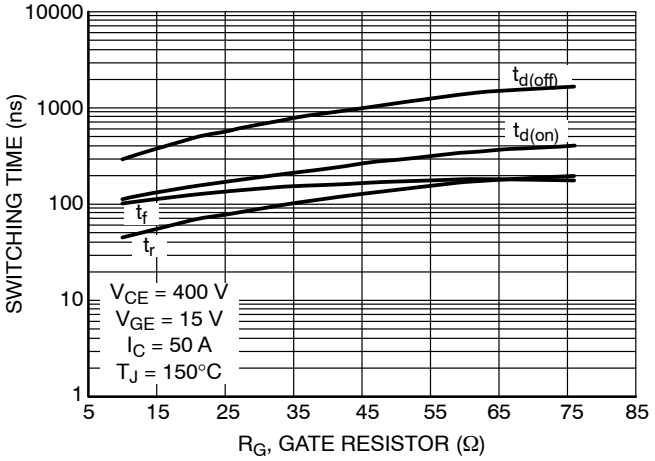


Figure 14. Switching Time vs. R_G

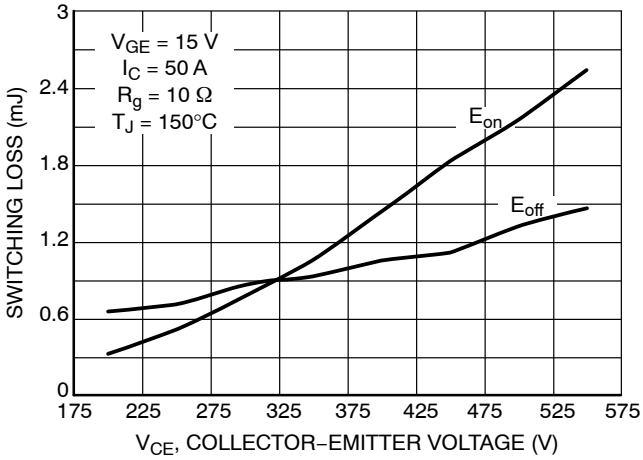


Figure 15. Switching Loss vs. V_{CE}

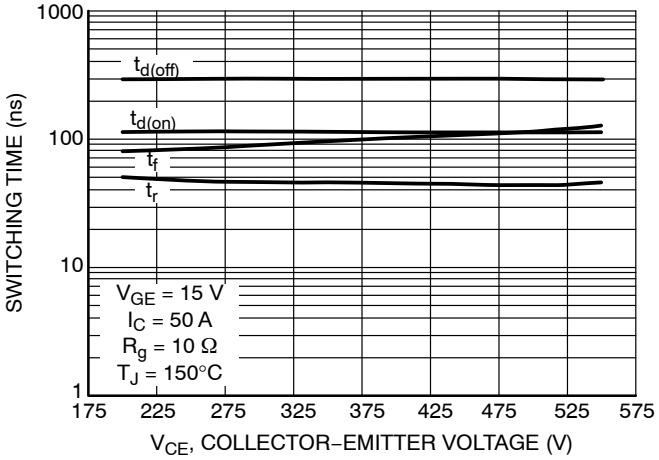


Figure 16. Switching Time vs. V_{CE}

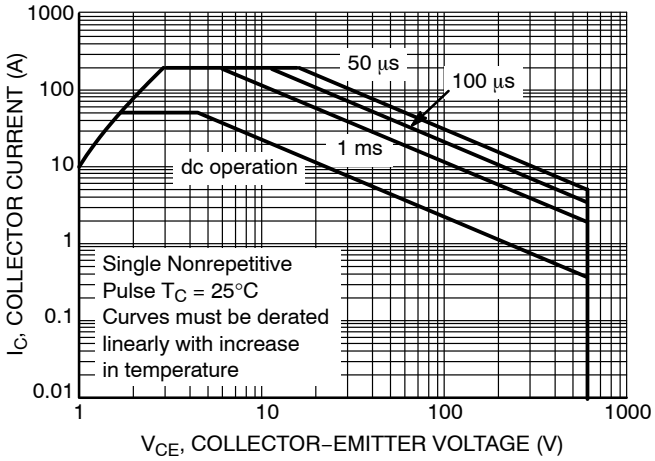


Figure 17. Safe Operating Area

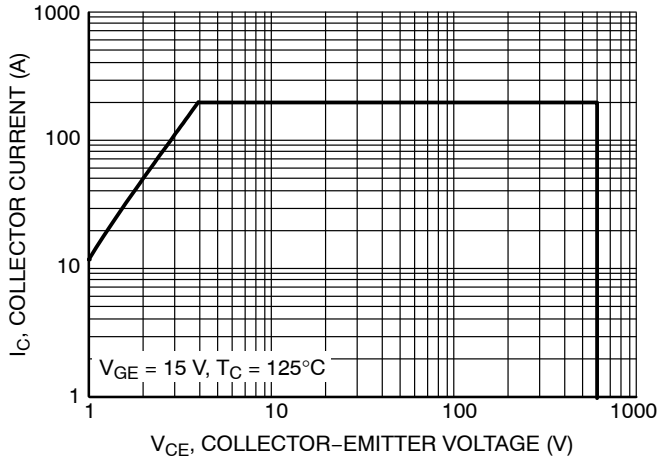


Figure 18. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

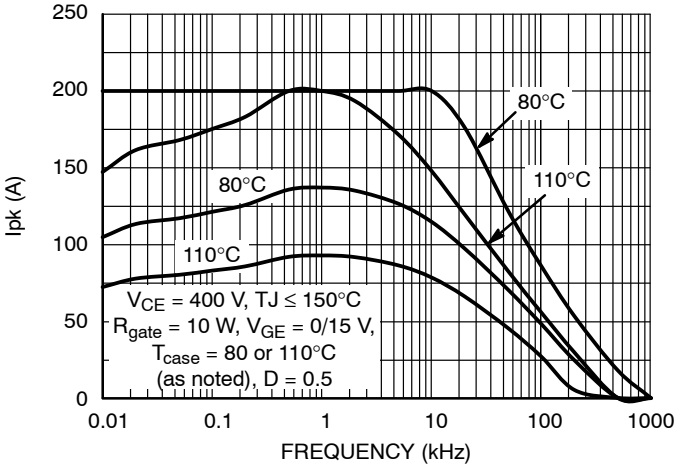
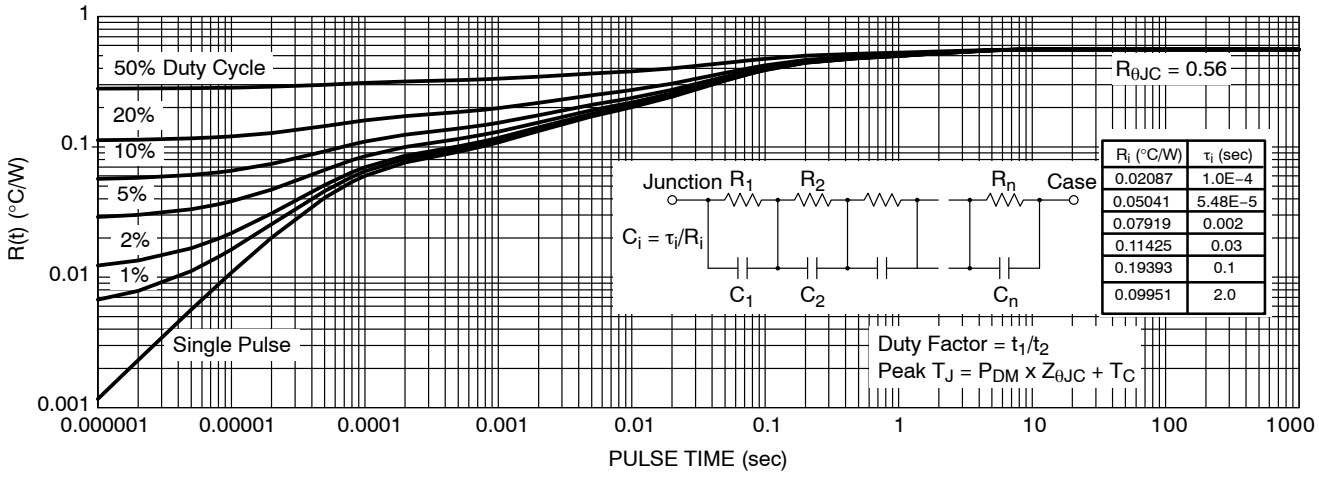
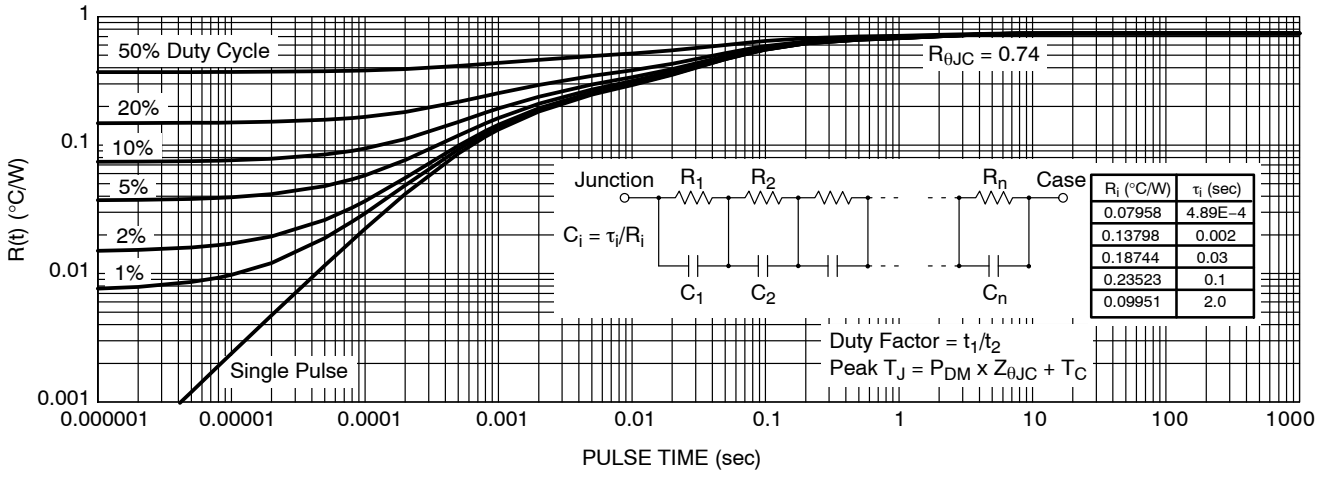


Figure 19. Collector Current vs. Switching Frequency



R_i (°C/W)	τ_i (sec)
0.02087	1.0E−4
0.05041	5.48E−5
0.07919	0.002
0.11425	0.03
0.19393	0.1
0.09951	2.0

Figure 20. IGBT Transient Thermal Impedance



R_i (°C/W)	τ_i (sec)
0.07958	4.89E−4
0.13798	0.002
0.18744	0.03
0.23523	0.1
0.09951	2.0

Figure 21. Diode Transient Thermal Impedance

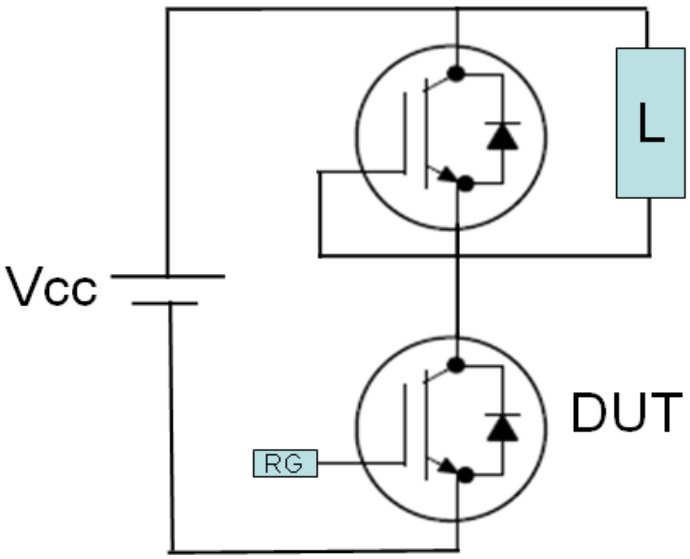


Figure 22. Test Circuit for Switching Characteristics

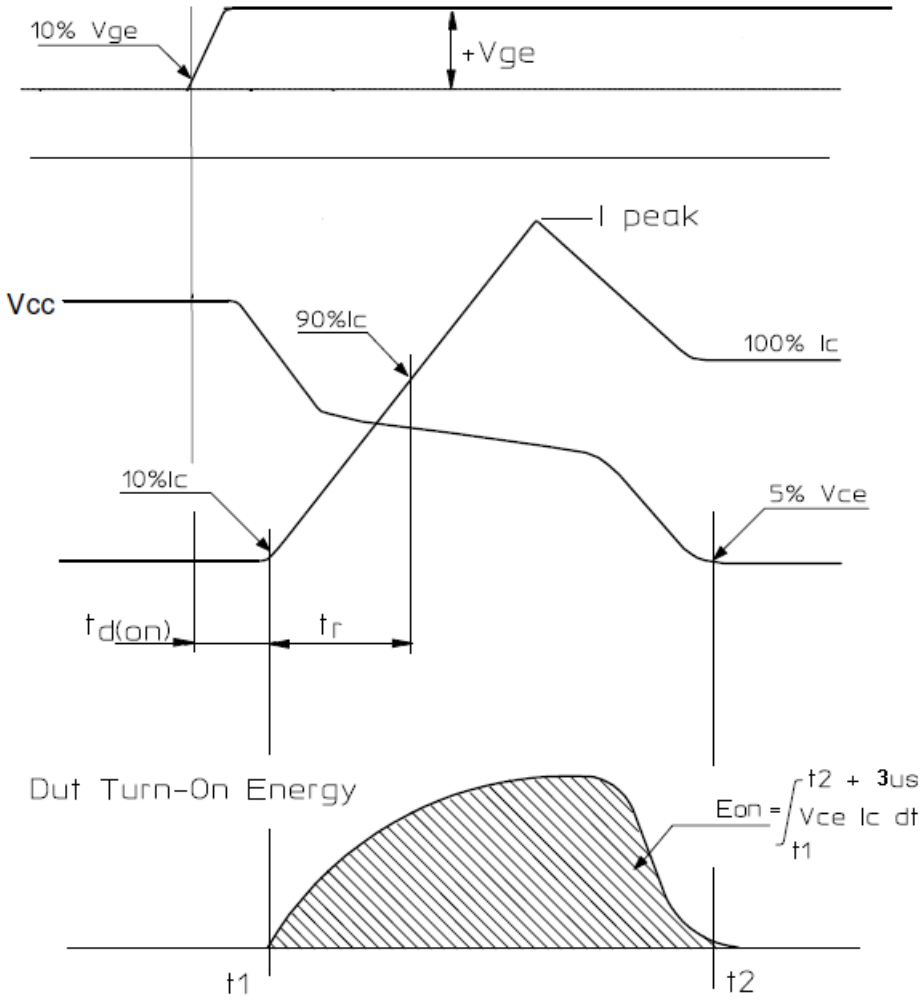


Figure 23. Definition of Turn On Waveform

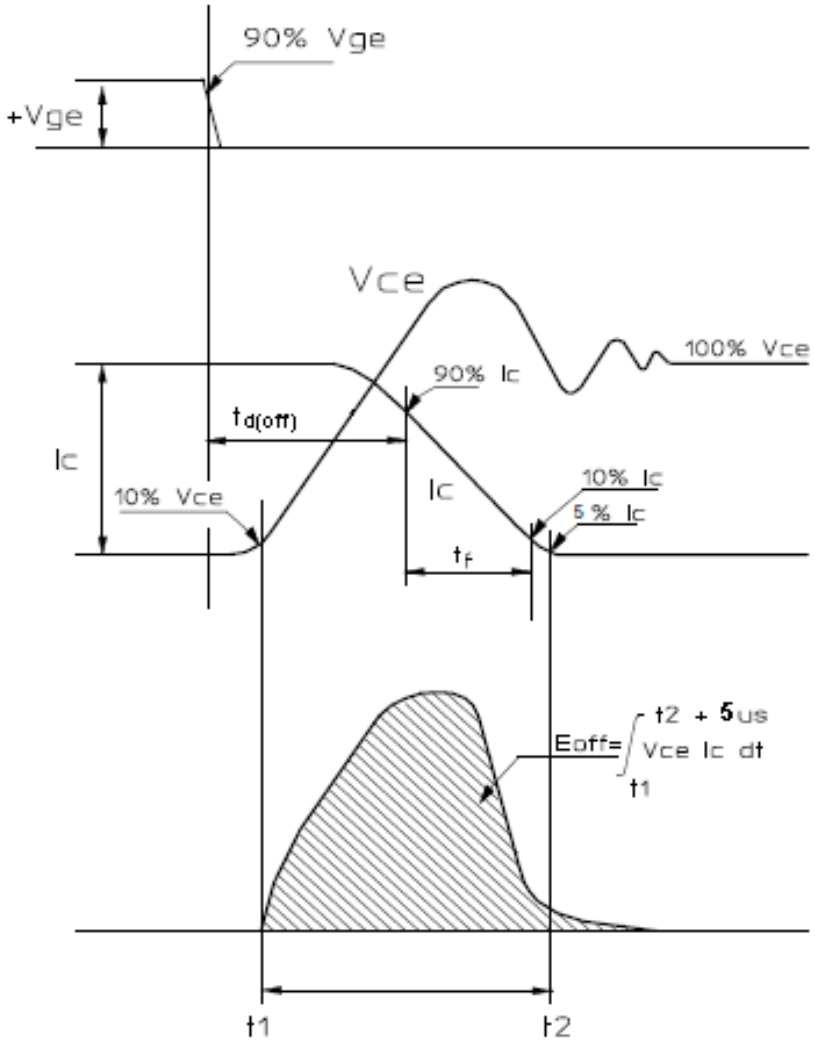


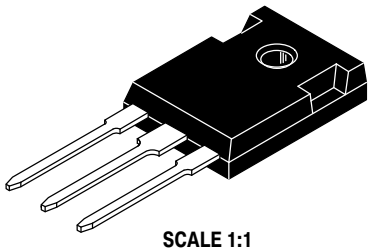
Figure 24. Definition of Turn Off Waveform

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

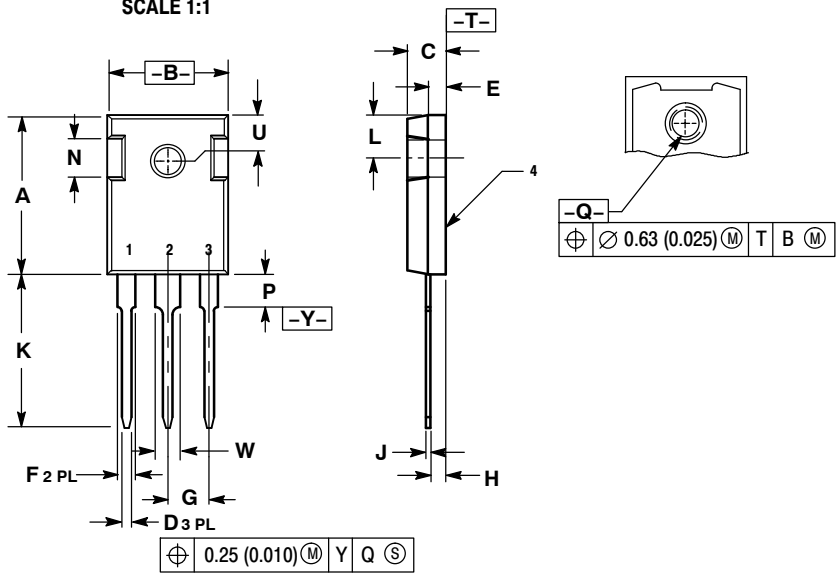
ON Semiconductor®

TO−247
CASE 340L−02
ISSUE F

DATE 26 OCT 2011



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	8.30
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	---	4.50	---	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)

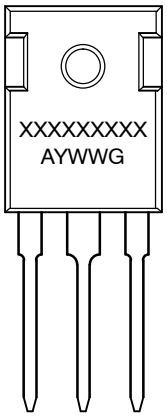
STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ASB15080C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO−247	PAGE 1 OF 2

ISSUE	REVISION	DATE
D	CHANGE OF OWNERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. DIM A WAS 20.80–21.46/0.819–0.845. DIM K WAS 19.81–20.32/0.780–0.800. UPDATED STYLE 1, ADDED STYLES 2, 3, & 4. REQ. BY L. HAYES.	25 AUG 2000
E	DIM E MINIMUM WAS 2.20/0.087. DIM K MINIMUM WAS 20.06/0.790. ADDED GENERIC MARKING DIAGRAM. REQ. BY S. ALLEN.	26 FEB 2010
F	ADDED STYLES 5 AND 6. REQ. BY J. PEREZ.	26 OCT 2011

PUBLICATION ORDERING INFORMATION

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