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# **IGBT**

This Insulated Gate Bipolar Transistor (IGBT) features a robust and cost effective Field Stop (FS) Trench construction, and provides superior performance in demanding switching applications, offering both low on state voltage and minimal switching loss. The IGBT is well suited for half bridge resonant applications. Incorporated into the device is a soft and fast co–packaged free wheeling diode with a low forward voltage.

#### **Features**

- Low Saturation Voltage using Trench with Fieldstop Technology
- Low Switching Loss Reduces System Power Dissipation
- Low Gate Charge
- Soft, Fast Free Wheeling Diode
- These are Pb-Free Devices

# **Typical Applications**

• Inverter Welding

#### **ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-emitter voltage	$V_{CES}$	600	V
Collector current @ Tc = 25°C @ Tc = 100°C	Ι <sub>C</sub>	120 60	A
Diode forward current @ Tc = 25°C @ Tc = 100°C	l <sub>F</sub>	120 60	А
Pulsed collector current, T <sub>pulse</sub> limited by T <sub>Jmax</sub>	I <sub>CM</sub>	240	А
Diode pulsed current, T <sub>pulse</sub> limited by T <sub>Jmax</sub>	I <sub>FM</sub>	240	Α
Gate-emitter voltage	$V_{GE}$	±20	V
Power Dissipation @ Tc = 25°C @ Tc = 100°C	P <sub>D</sub>	298 119	W
Operating junction temperature range	$T_J$	-55 to +150	°C
Storage temperature range	T <sub>stg</sub>	-55 to +150	°C
Lead temperature for soldering, 1/8" from case for 5 seconds	T <sub>SLD</sub>	260	°C

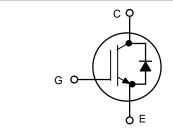
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

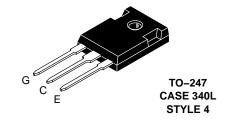


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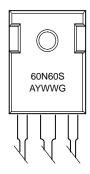
http://onsemi.com

60 A, 600 V V<sub>CEsat</sub> = 2.0 V E<sub>off</sub> = 0.60 mJ





## **MARKING DIAGRAM**



A = Assembly Location

Y = Year WW = Work Week G = Pb-Free Package

#### **ORDERING INFORMATION**

Device	Package	Shipping
NGTB60N60SWG	TO-247 (Pb-Free)	30 Units / Rail

## THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal resistance junction-to-case, for IGBT	$R_{ heta JC}$	0.42	°C/W
Thermal resistance junction-to-case, for Diode	$R_{ heta JC}$	1.00	°C/W
Thermal resistance junction-to-ambient	$R_{ heta JA}$	40	°C/W

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Тур	Max	Unit
STATIC CHARACTERISTIC						
Collector–emitter breakdown voltage, gate–emitter short–circuited	$V_{GE} = 0 \text{ V, I}_{C} = 500 \mu\text{A}$	V <sub>(BR)CES</sub>	600	_	-	V
Collector-emitter saturation voltage	V <sub>GE</sub> = 15 V, I <sub>C</sub> = 60 A V <sub>GE</sub> = 15 V, I <sub>C</sub> = 60 A, T <sub>J</sub> = 150°C	V <sub>CEsat</sub>	- -	2.0 2.6	2.5 -	V
Gate-emitter threshold voltage	$V_{GE} = V_{CE}, I_{C} = 150 \mu A$	V <sub>GE(th)</sub>	4.5	5.5	6.5	V
Collector–emitter cut–off current, gate– emitter short–circuited	V <sub>GE</sub> = 0 V, V <sub>CE</sub> = 600 V V <sub>GE</sub> = 0 V, V <sub>CE</sub> = 600 V, T <sub>J</sub> = 150°C	I <sub>CES</sub>	- -	- -	0.2 2	mA
Gate leakage current, collector–emitter short–circuited	V <sub>GE</sub> = 20 V , V <sub>CE</sub> = 0 V	I <sub>GES</sub>	-	-	200	nA
DYNAMIC CHARACTERISTIC						
Input capacitance		C <sub>ies</sub>	-	4112	-	pF
Output capacitance	$V_{CE} = 20 \text{ V}, V_{GE} = 0 \text{ V}, f = 1 \text{ MHz}$	C <sub>oes</sub>	-	169	-	
Reverse transfer capacitance	1	C <sub>res</sub>	-	107	_	
Gate charge total		$Q_g$		173		nC
Gate to emitter charge	$V_{CE} = 480 \text{ V}, I_{C} = 60 \text{ A}, V_{GE} = 15 \text{ V}$	Q <sub>ge</sub>		38		1
Gate to collector charge	1	Q <sub>gc</sub>		87		1
SWITCHING CHARACTERISTIC, INDUC	TIVE LOAD					-
Turn-on delay time		t <sub>d(on)</sub>		87		ns
Rise time	1	t <sub>r</sub>		48		1
Turn-off delay time	$T_J = 25^{\circ}C$ $V_{CC} = 400 \text{ V, } I_C = 60 \text{ A}$	t <sub>d(off)</sub>		180		1
Fall time	$R_g = 10 \Omega$ $V_{GE} = 0 \text{ V/ } 15 \text{ V}$	t <sub>f</sub>		70		1
Turn-off switching loss	VGE = 0 V/ 13 V	E <sub>off</sub>		0.60		mJ
Turn-on switching loss	1	E <sub>on</sub>		1.41		1
Turn-on delay time		t <sub>d(on)</sub>		85		ns
Rise time	1	t <sub>r</sub>		50		1
Turn-off delay time	$T_J = 150^{\circ}C$ $V_{CC} = 400 \text{ V, } I_C = 60 \text{ A}$	t <sub>d(off)</sub>		186		1
Fall time	$R_g = 10 \Omega$ $V_{GE} = 0 \text{ V/ } 15 \text{ V}$	t <sub>f</sub>		91		1
Turn-off switching loss	VGE = 0 V/ 15 V	E <sub>off</sub>		1.11		mJ
Turn-on switching loss	1	E <sub>on</sub>		1.77		
DIODE CHARACTERISTIC		•				
Forward voltage	V <sub>GE</sub> = 0 V, I <sub>F</sub> = 30 A V <sub>GE</sub> = 0 V, I <sub>F</sub> = 30 A, T <sub>J</sub> = 150°C	V <sub>F</sub>		1.98 2.10	2.30	V
Reverse recovery time	T <sub>J</sub> = 25°C	t <sub>rr</sub>		76		ns
Reverse recovery charge	$I_F = 30 \text{ Å}, V_R = 200 \text{ V}$ $di_F/dt = 200 \text{ A}/\mu \text{s}$	Q <sub>rr</sub>		291		nc
Reverse recovery current	1	I <sub>rrm</sub>		7		Α

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

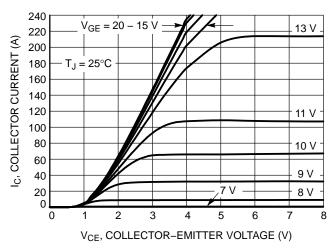


Figure 1. Output Characteristics

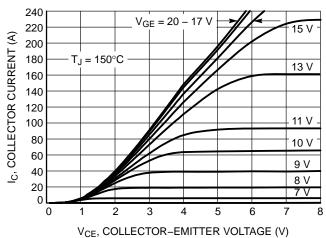


Figure 2. Output Characteristics

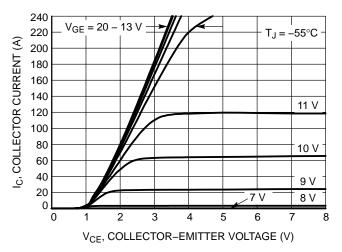
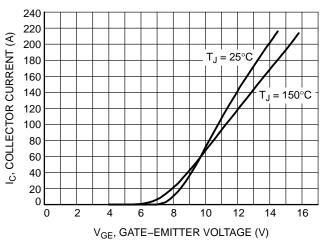


Figure 3. Output Characteristics



**Figure 4. Typical Transfer Characteristics** 

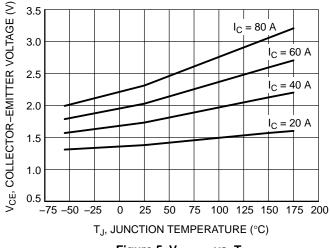


Figure 5. V<sub>CE(sat)</sub> vs. T<sub>J</sub>

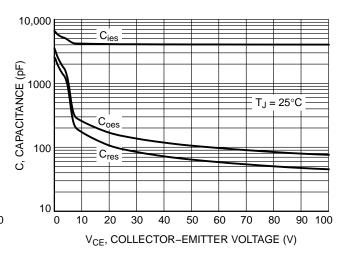
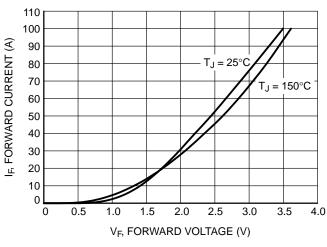


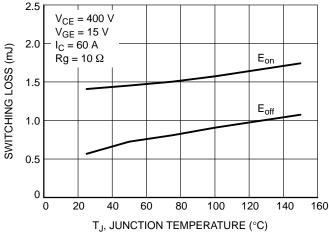
Figure 6. Typical Capacitance



20 V<sub>GE</sub>, GATE-EMITTER VOLTAGE (V) 18 16 14 12 10 8 V<sub>CE</sub> = 480 V 6 V<sub>GE</sub> = 15 V  $I_{C} = 60 \text{ A}$ 2 0 20 40 80 100 120 140 160 180 200 QG, GATE CHARGE (nC)

Figure 7. Diode Forward Characteristics

Figure 8. Typical Gate Charge



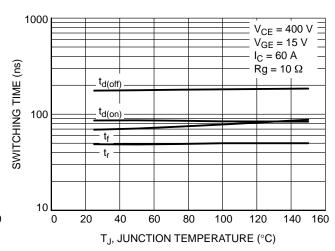
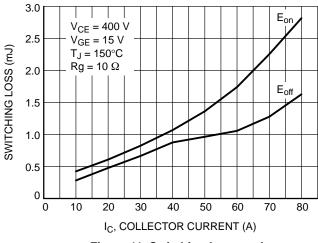


Figure 9. Switching Loss vs. Temperature

Figure 10. Switching Time vs. Temperature



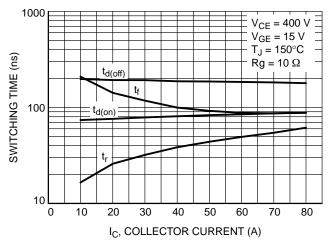


Figure 11. Switching Loss vs. I<sub>C</sub>

Figure 12. Switching Time vs. I<sub>C</sub>

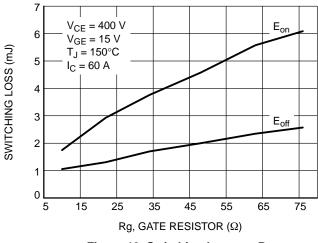


Figure 13. Switching Loss vs. Rg

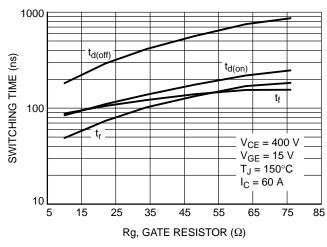


Figure 14. Switching Time vs. Rg

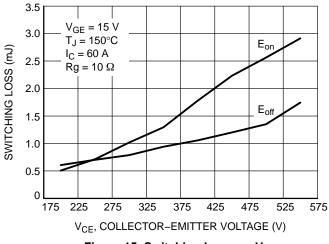


Figure 15. Switching Loss vs. V<sub>CE</sub>

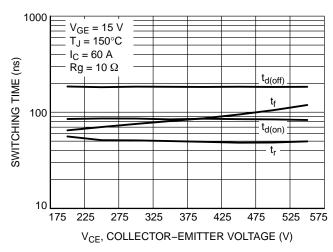


Figure 16. Switching Time vs. V<sub>CE</sub>

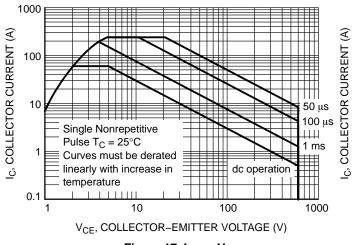
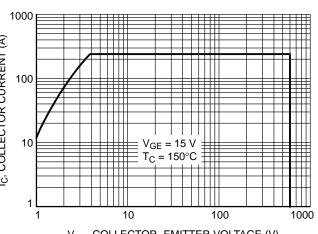


Figure 17. I<sub>C</sub> vs. V<sub>CE</sub>



V<sub>CE</sub>, COLLECTOR-EMITTER VOLTAGE (V)

Figure 18. I<sub>C</sub> vs. V<sub>CE</sub>

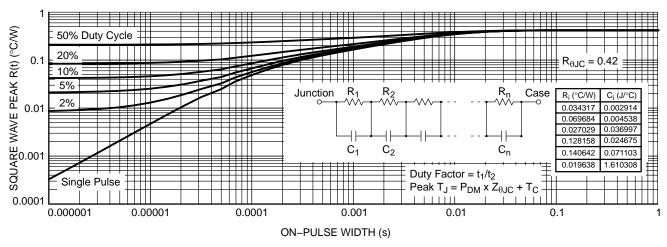


Figure 19. IGBT Transient Thermal Impedance

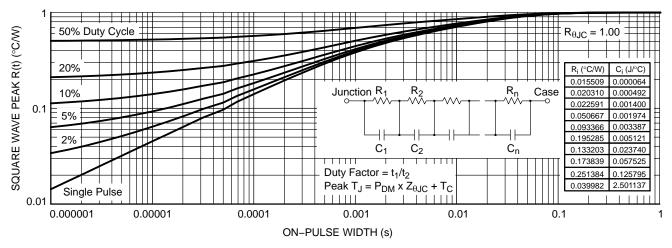
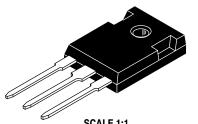


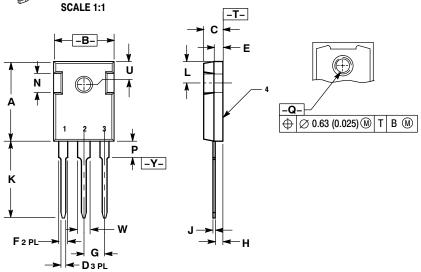
Figure 20. Diode Transient Thermal Impedance



3. GATE 4. ANODE

TO-247 CASE 340L-02 ISSUE F

**DATE 26 OCT 2011** 



STYLE 1: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 2: PIN 1. ANODE 2. CATHODE (S) 3. ANODE 2 4. CATHODES (S)	STYLE 3: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 4: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR
STYLE 5: PIN 1. CATHODE 2. ANODE	STYLE 6: PIN 1. MAIN TERMINAL 1 2. MAIN TERMINAL 2		

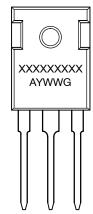
⊕ 0.25 (0.010) M Y Q S

3. GATE 4. MAIN TERMINAL 2

- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	20.32	21.08	0.800	8.30
В	15.75	16.26	0.620	0.640
С	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
Е	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45	BSC	0.215	BSC
Н	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P		4.50		0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242	BSC
W	2.87	3.12	0.113	0.123

#### **GENERIC MARKING DIAGRAM\***



XXXXX = Specific Device Code

= Assembly Location Υ = Year WW = Work Week

G

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

= Pb-Free Package

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ISSUE	REVISION	DATE
D	CHANGE OF OWNERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. DIM A WAS 20.80-21.46/0.819-0.845. DIM K WAS 19.81-20.32/0.780-0.800. UPDATED STYLE 1, ADDED STYLES 2, 3, & 4. REQ. BY L. HAYES.	25 AUG 2000
E	DIM E MINIMUM WAS 2.20/0.087. DIM K MINIMUM WAS 20.06/0.790. ADDED GENERIC MARKING DIAGRAM. REQ. BY S. ALLEN.	26 FEB 2010
F	ADDED STYLES 5 AND 6. REQ. BY J. PEREZ.	26 OCT 2011

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