N-channel 600 V, 0.175 Ω typ., 18 A MDmesh™ M2 EP Power MOSFET in a TO-220FP package

TO-220FP

D(2)

G(1)

S(3)

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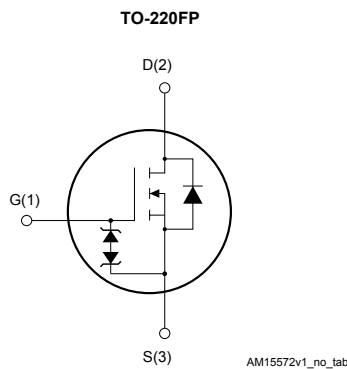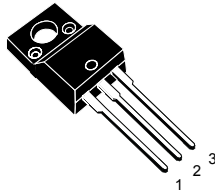
Features

Order code	V_{DS} at T_J max.	$R_{DS(on)}$ max.	I_D
STF25N60M2-EP	650 V	0.188 Ω	18 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- Tailored for Very high frequency converters (f > 150 kHz)

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 enhanced performance (EP) technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

Product status link
STF25N60M2-EP

Product summary	
Order code	STF25N60M2-EP
Marking	25N60M2EP
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
V_{GS}	Transient gate-source voltage ($t_p \leq 10$ ns)	±35	V
I_D[1]	Drain current (continuous) at $T_C = 25$ °C	18	A
I_D[1]	Drain current (continuous) at $T_C = 100$ °C	11.3	A
I_{DM}[2]	Drain current (pulsed)	72	A
P_{TOT}	Total dissipation at $T_C = 25$ °C	30	W
dv/dt[3]	Peak diode recovery voltage slope	15	V/ns
dv/dt[4]	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1$ s, $T_C = 25$ °C)	2500	V
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 18$ A, di/dt ≤ 400 A/µs, $V_{DS\ peak} < V_{(BR)DSS}$, $V_{DD} = 400$ V
4. $V_{DS} \leq 480$ V

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	4.2	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	3.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	200	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C [1]			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 9 A		0.175	0.188	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	1090	-	pF
C_{oss}	Output capacitance		-	56	-	pF
C_{rss}	Reverse transfer capacitance		-	1.6	-	pF
$C_{oss\ eq.}$[1]	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	255	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 18 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	29	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	12	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{(off)}$	Turn-off energy (from 90% V_{GS} to 0% I_D)	V_{DD} = 400 V, I_D = 2 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	7	-	µJ
		V_{DD} = 400 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	8	-	µJ

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 9 A,	-	15	-	ns
t_r	Rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	10	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	61	-	ns
t_f	Fall time		-	16	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
I_{SDM} [1]	Source-drain current (pulsed)		-		72	A
V_{SD} [2]	Forward on voltage	V_{GS} = 0 V, I_{SD} = 18 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs, V_{DD} = 100 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	360		ns
Q_{rr}	Reverse recovery charge		-	5		µC
I_{RRM}	Reverse recovery current		-	28		A
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	445		ns
Q_{rr}	Reverse recovery charge		-	6.5		µC
I_{RRM}	Reverse recovery current		-	29		A

1. *Pulse width is limited by safe operating area*

2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1   Electrical characteristics (curves)

Figure 1. Safe operating area
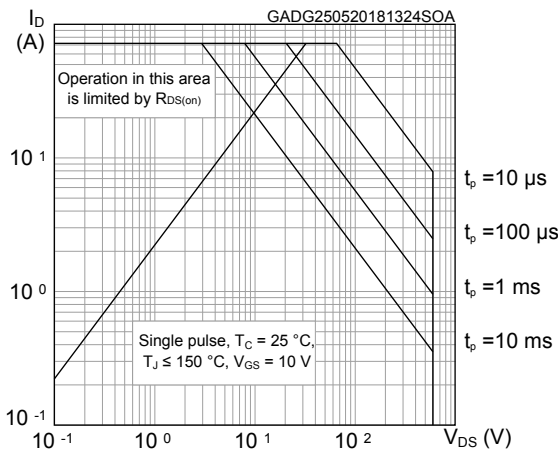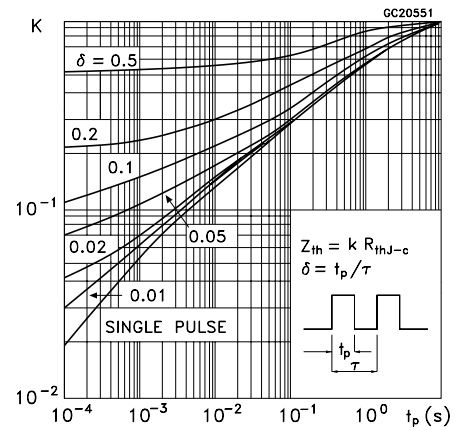

Figure 2. Thermal impedance
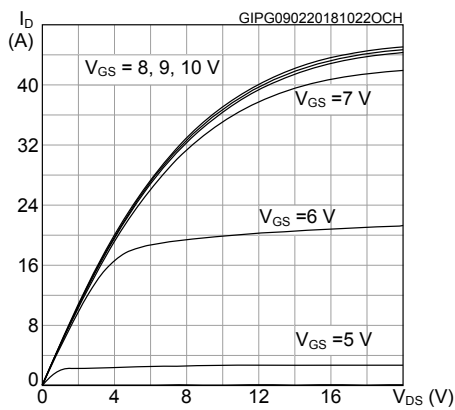

Figure 3. Output characteristics
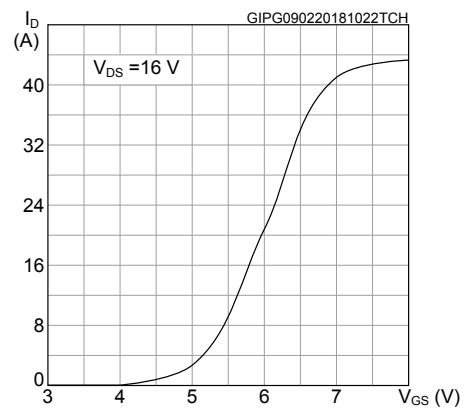

Figure 4. Transfer characteristics

Figure 5. Gate charge vs gate-source voltage
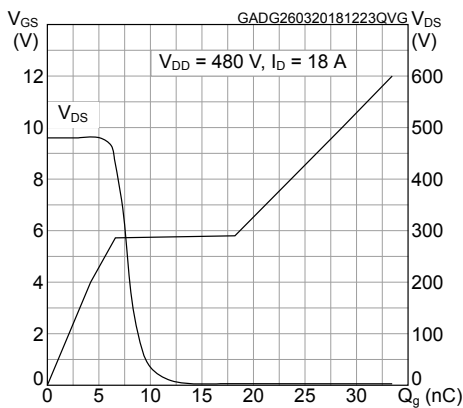

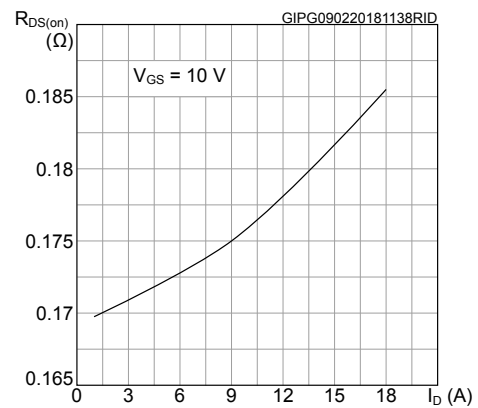**Figure 6. Static drain-source on-resistance**

Figure 7. Capacitance variations

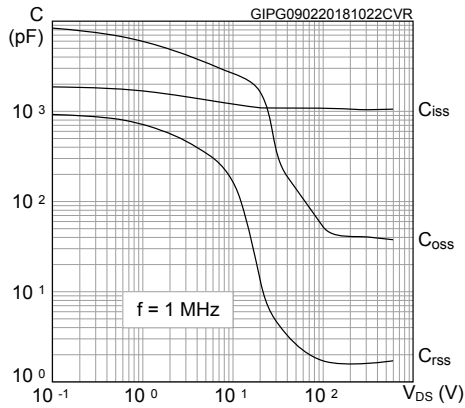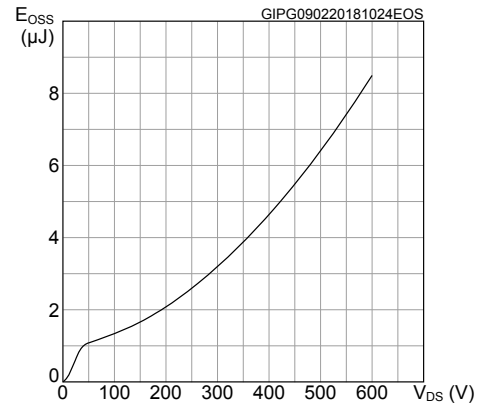### Figure 8. Output capacitance stored energy
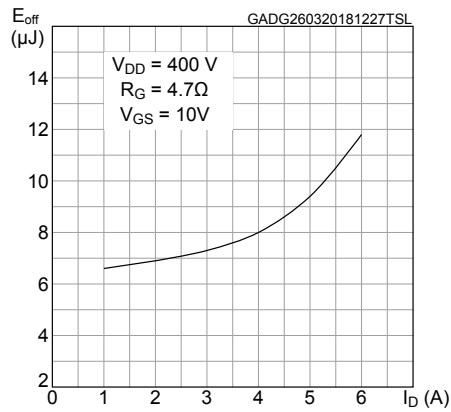

Figure 9. Turn-off switching energy vs drain current

Figure 10. Normalized gate threshold voltage vs temperature
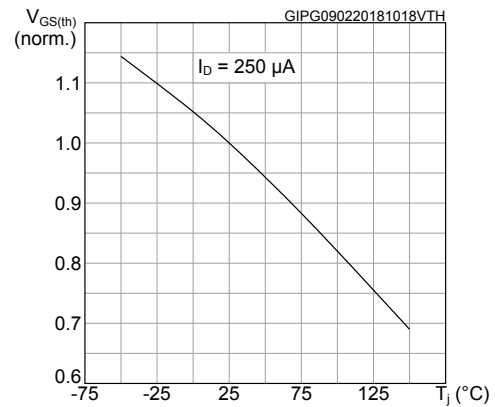
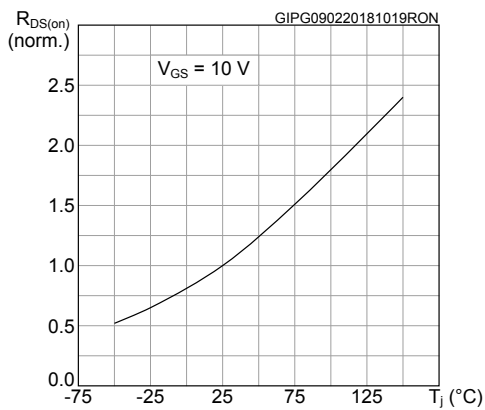### Figure 11. Normalized on-resistance vs temperature
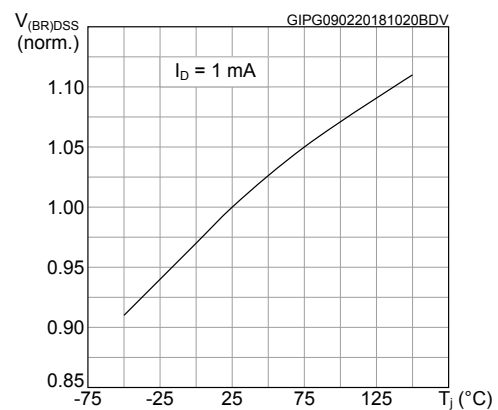

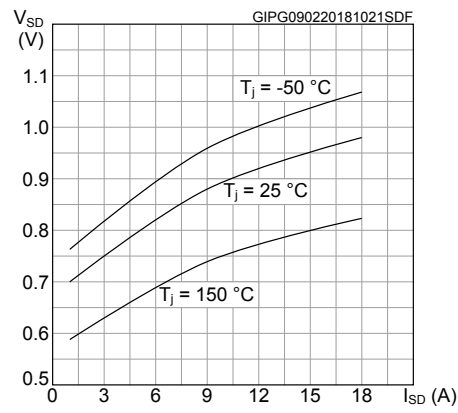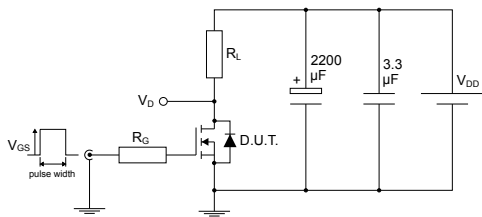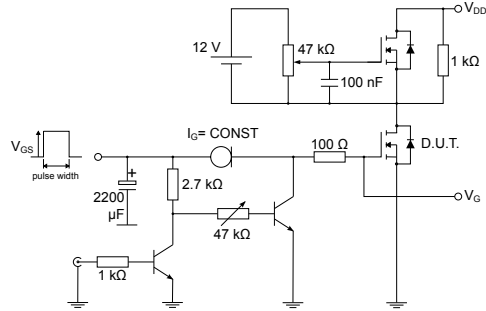### Figure 12. Normalized $V_{(BR)DSS}$ vs temperature

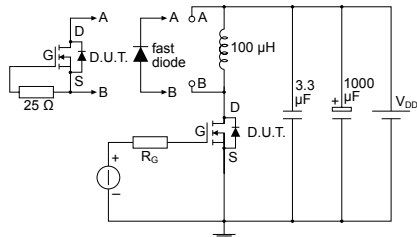**Figure 13. Source-drain diode forward characteristics**

3 Test circuits

Figure 14. Test circuit for resistive load switching times
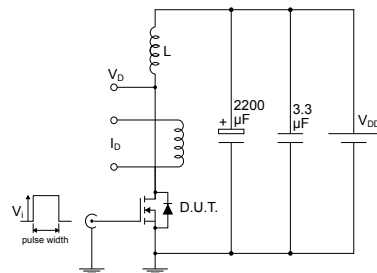

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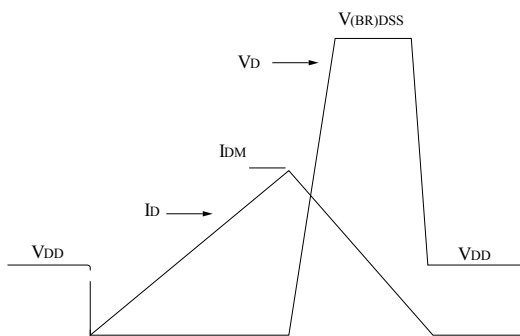**Figure 15. Test circuit for gate charge behavior**

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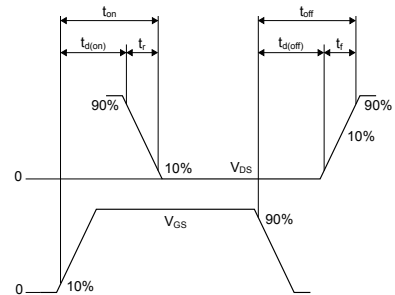**Figure 16. Test circuit for inductive load switching and diode recovery times**

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Figure 17. Unclamped inductive load test circuit

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Figure 18. Unclamped inductive waveform

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Figure 19. Switching time waveform

AM01473v1

# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 20. TO-220FP package outline
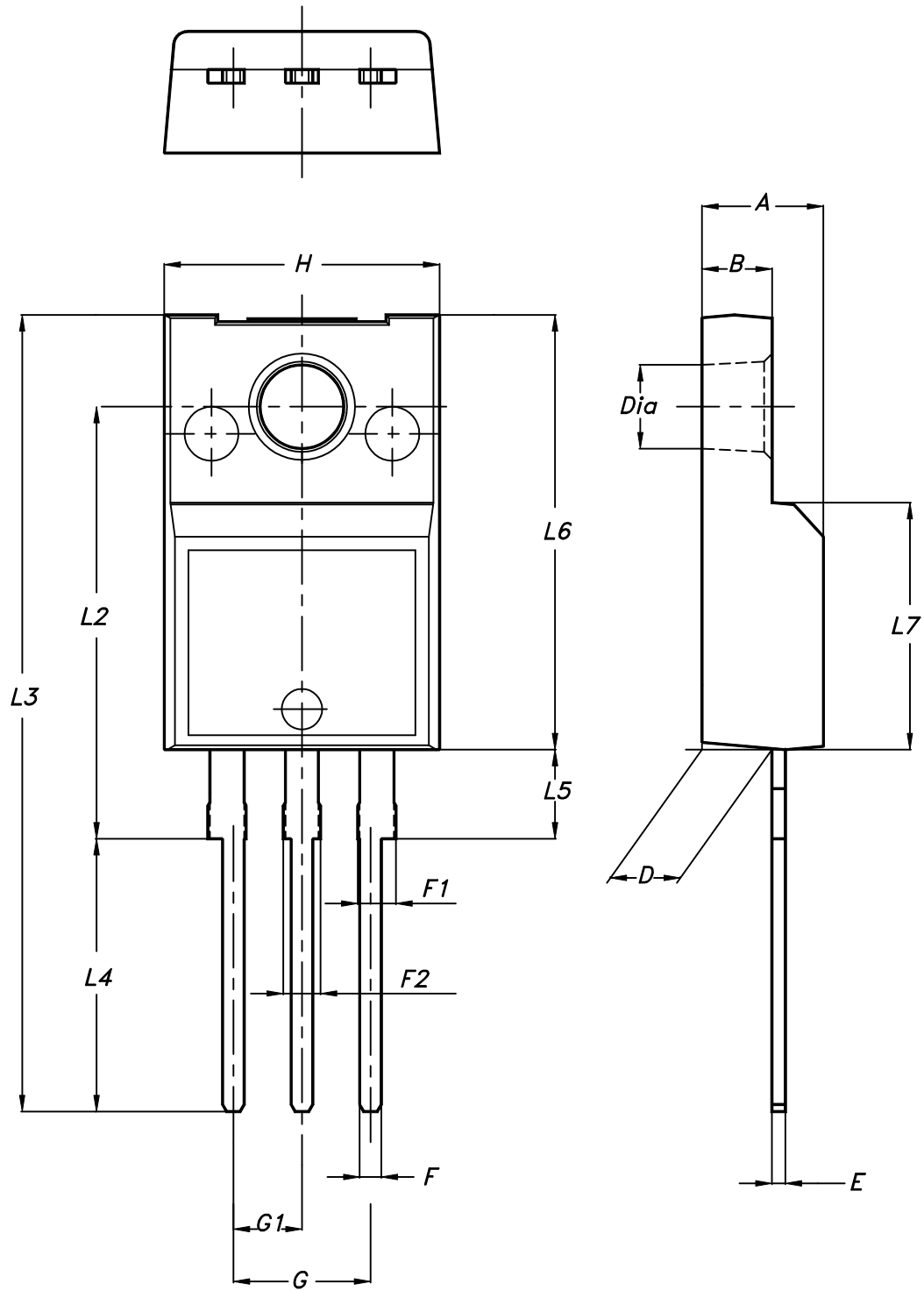
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Table 9. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history

Table 10. Document revision history

Date	Revision	Changes
02-Dec-2014	1	First release.
12-Jan-2015	2	Updated product status from "preliminary data" to "production data".
14-Jan-2015	3	Corrected product status information on cover page.
25-Aug-2016	4	Modified: *Table 2: "Absolute maximum ratings"* Minor text changes
13-Feb-2018	5	Removed maturity status indication from cover page. Modified *Table 1. Absolute maximum ratings*, *Table 4. On/off states*, *Table 5. Dynamic*, *Table 6. Switching Energy*, *Table 7. Switching times* and *Table 8. Source drain diode*. Updated Section 2.1 Electrical characteristics (curves). Minor text changes.
28-May-2018	6	Updated Table 1. Absolute maximum ratings. Updated Section 2 Electrical characteristics and Section 2.1 Electrical characteristics (curves). Minor text changes

Contents

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