# BC549C, BC550C

# Low Noise Transistors

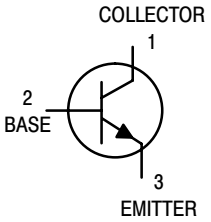
## NPN Silicon

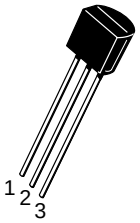
ON Semiconductor®

http://onsemi.com

### Features

- These are Pb−Free Devices*




STRAIGHT LEAD
BULK PACK

**TO−92**
**CASE 29**
**STYLE 17**

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector−Emitter Voltage<br>BC549C<br>BC550C | $V_{CEO}$ | <br>30<br>45 | Vdc |
| Collector−Base Voltage<br>BC549C<br>BC550C | $V_{CBO}$ | <br>30<br>50 | Vdc |
| Emitter−Base Voltage | $V_{EBO}$ | 5.0 | Vdc |
| Collector Current − Continuous | $I_C$ | 100 | Vdc |
| Total Device Dissipation @ $T_A$ = 25°C<br>Derate above = 25°C | $P_D$ | 625<br>5.0 | mW<br>mW/°C |
| Total Device Dissipation @ $T_A$ = 25°C<br>Derate above = 25°C | $P_D$ | 1.5<br>12 | W<br>mW/°C |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |

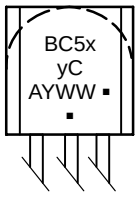
### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction−to−Ambient | $R_{\theta JA}$ | 200 | °C/W |
| Thermal Resistance, Junction−to−Case | $R_{\theta JC}$ | 83.3 | °C/W |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### MARKING DIAGRAM




BC5xyC = Device Code
x = 4 or 5
y = 9 or 0
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| BC549CG | TO−92<br>(Pb−Free) | 5000 Units / Bulk |
| BC550CG | TO−92<br>(Pb−Free) | 5000 Units / Bulk |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector−Emitter Breakdown Voltage ($I_C$ = 10 mAdc, $I_B$ = 0) | $V_{(BR)CEO}$ | 45 | – | – | Vdc |
| Collector−Base Breakdown Voltage ($I_C$ = 10 μAdc, $I_E$ = 0) | $V_{(BR)CBO}$ | 50 | – | – | Vdc |
| Emitter−Base Breakdown Voltage ($I_E$ = 10 μAdc, $I_C$ = 0) | $V_{(BR)EBO}$ | 5.0 | – | – | Vdc |
| Collector Cutoff Current ($V_{CB}$ = 30 V, $I_E$ = 0)<br>($V_{CB}$ = 30 V, $I_E$ = 0, $T_A$ = +125°C) | $I_{CBO}$ | –<br>– | –<br>– | 15<br>5.0 | nAdc<br>μAdc |
| Emitter Cutoff Current ($V_{EB}$ = 4.0 Vdc, $I_C$ = 0) | $I_{EBO}$ | – | – | 15 | nAdc |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain ($I_C$ = 10 μAdc, $V_{CE}$ = 5.0 Vdc)<br>($I_C$ = 2.0 mAdc, $V_{CE}$ = 5.0 Vdc) | $h_{FE}$ | 100<br>420 | 270<br>500 | –<br>800 | – |
| Collector−Emitter Saturation Voltage ($I_C$ = 10 mAdc, $I_B$ = 0.5 mAdc)<br>($I_C$ = 10 mAdc, $I_B$ = see note 1)<br>($I_C$ = 100 mAdc, $I_B$ = 5.0 mAdc, see note 2) | $V_{CE(sat)}$ | –<br>–<br>– | 0.075<br>0.3<br>0.25 | 0.25<br>0.6<br>0.6 | Vdc |
| Base−Emitter Saturation Voltage ($I_C$ = 100 mAdc, $I_B$ = 5.0 mAdc) | $V_{BE(sat)}$ | – | 1.1 | – | Vdc |
| Base−Emitter On Voltage ($I_C$ = 10 μAdc, $V_{CE}$ = 5.0 Vdc)<br>($I_C$ = 100 μAdc, $V_{CE}$ = 5.0 Vdc)<br>($I_C$ = 2.0 mAdc, $V_{CE}$ = 5.0 Vdc) | $V_{BE(on)}$ | –<br>–<br>0.55 | 0.52<br>0.55<br>0.62 | –<br>–<br>0.7 | Vdc |
| **SMALL−SIGNAL CHARACTERISTICS** | | | | | |
| Current−Gain — Bandwidth Product ($I_C$ = 10 mAdc, $V_{CE}$ = 5.0 Vdc, f = 100 MHz) | $f_T$ | – | 250 | – | MHz |
| Collector−Base Capacitance ($V_{CB}$ = 10 Vdc, $I_E$ = 0, f = 1.0 MHz) | $C_{cbo}$ | – | 2.5 | – | pF |
| Small−Signal Current Gain ($I_C$ = 2.0 mAdc, $V_{CE}$ = 5.0 V, f = 1.0 kHz) | $h_{fe}$ | 450 | 600 | 900 | – |
| Noise Figure ($I_C$ = 200 μAdc, $V_{CE}$ = 5.0 Vdc, $R_S$ = 2.0 kΩ, f = 1.0 kHz)<br>($I_C$ = 200 μAdc, $V_{CE}$ = 5.0 Vdc, $R_S$ = 100 kΩ, f = 1.0 kHz) | $NF_1$<br>$NF_2$ | –<br>– | 0.6<br>– | 2.5<br>10 | dB |

1. $I_B$ is value for which $I_C$ = 11 mA at $V_{CE}$ = 1.0 V.
2. Pulse test = 300 μs − Duty cycle = 2%.

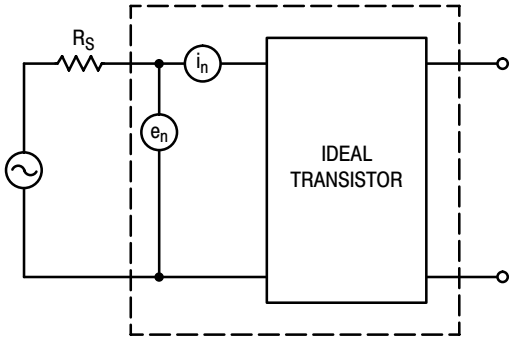



**Figure 1. Transistor Noise Model**

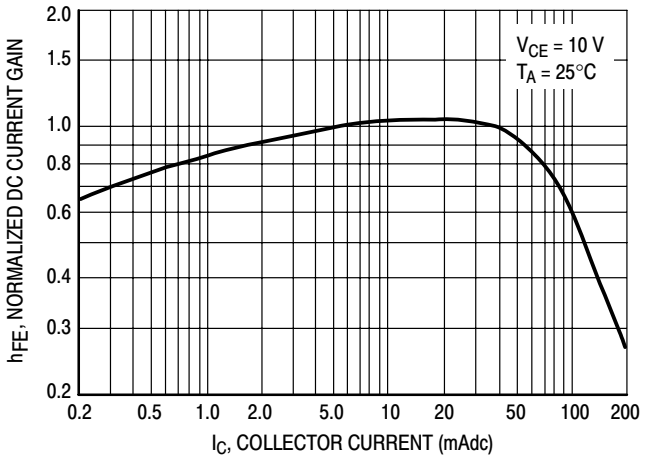



**Figure 2. Normalized DC Current Gain**

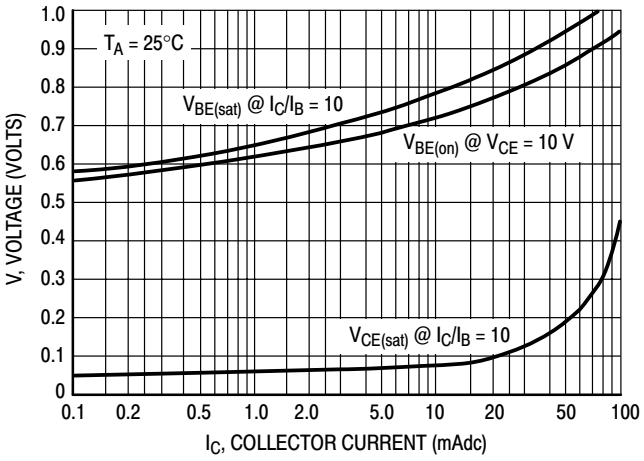



**Figure 3. “Saturation” and “On” Voltages**

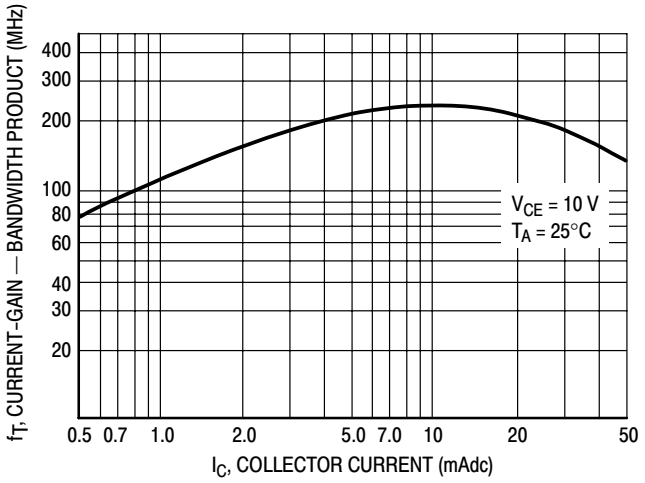



**Figure 4. Current−Gain — Bandwidth Product**

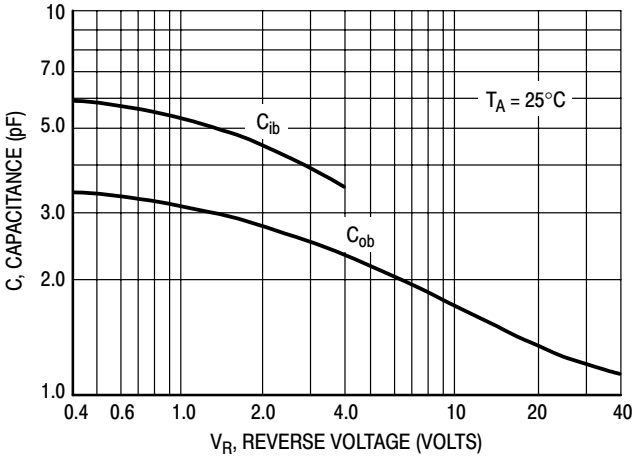



**Figure 5. Capacitance**

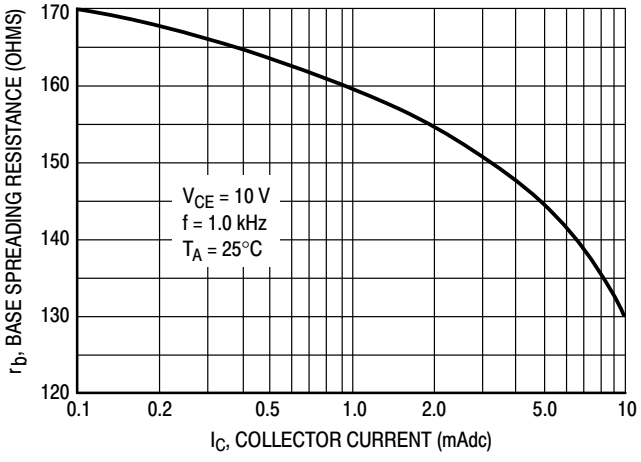



**Figure 6. Base Spreading Resistance**

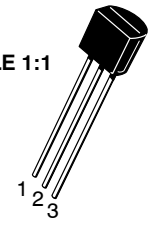
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

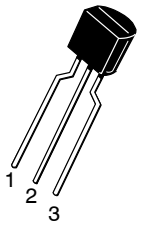
**TO−92 (TO−226)**
CASE 29−11
ISSUE AM

DATE 09 MAR 2007

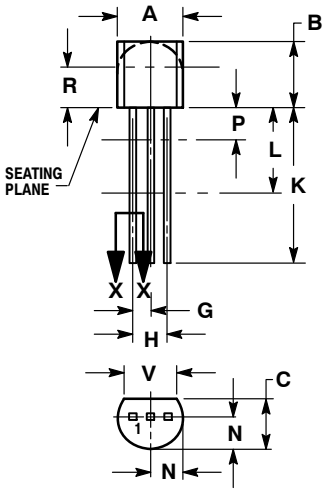
SCALE 1:1



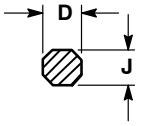

STRAIGHT LEAD
BULK PACK




BENT LEAD
TAPE & REEL
AMMO PACK



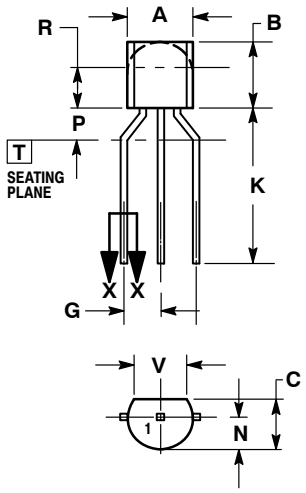

STRAIGHT LEAD
BULK PACK



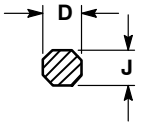

**SECTION X−X**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.175 | 0.205 | 4.45 | 5.20 |
| B | 0.170 | 0.210 | 4.32 | 5.33 |
| C | 0.125 | 0.165 | 3.18 | 4.19 |
| D | 0.016 | 0.021 | 0.407 | 0.533 |
| G | 0.045 | 0.055 | 1.15 | 1.39 |
| H | 0.095 | 0.105 | 2.42 | 2.66 |
| J | 0.015 | 0.020 | 0.39 | 0.50 |
| K | 0.500 | --- | 12.70 | --- |
| L | 0.250 | --- | 6.35 | --- |
| N | 0.080 | 0.105 | 2.04 | 2.66 |
| P | --- | 0.100 | --- | 2.54 |
| R | 0.115 | --- | 2.93 | --- |
| V | 0.135 | --- | 3.43 | --- |




BENT LEAD
TAPE & REEL
AMMO PACK




**SECTION X−X**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 4.45 | 5.20 |
| B | 4.32 | 5.33 |
| C | 3.18 | 4.19 |
| D | 0.40 | 0.54 |
| G | 2.40 | 2.80 |
| J | 0.39 | 0.50 |
| K | 12.70 | --- |
| N | 2.04 | 2.66 |
| P | 1.50 | 4.00 |
| R | 2.93 | --- |
| V | 3.43 | --- |

**STYLES ON PAGE 2**

| | | |
|---|---|---|
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| **STATUS:** | **ON SEMICONDUCTOR STANDARD** | |
| **NEW STANDARD:** | | |
| **DESCRIPTION:** | **TO−92 (TO−226)** | **PAGE 1 OF 3** |

**TO−92 (TO−226)**
CASE 29−11
ISSUE AM

DATE 09 MAR 2007

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. $V_{CC}$
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

| ISSUE | REVISION | DATE |
|---|---|---|
| AM | ADDED BENT−LEAD TAPE & REEL VERSION. REQ. BY J. SUPINA. | 09 MAR 2007 |
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