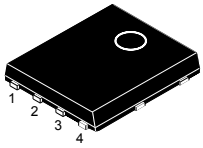
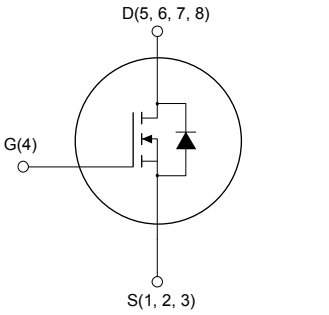
Datasheet

N-channel 650 V, 215 mΩ typ., 15 A MDmesh M5 Power MOSFET in a PowerFLAT 5x6 HV package



PowerFLAT 5x6 HV



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL18N65M5	650 V	240 mΩ	15 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Product status link
STL18N65M5

Product summary	
Order code	STL18N65M5
Marking	18N65M5
Package	PowerFLAT 5x6 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D[(1)]	Drain current (continuous) at T_C = 25 °C	15	A
	Drain current (continuous) at T_C = 100 °C	9.4	
I_{DM}[(2)]	Drain current (pulsed)	60	A
P_{TOT}	Total power dissipation at T_C = 25 °C	57	W
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	210	mJ
dv/dt[(3)]	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *I_D is limited by package.*
2. *Pulse width is limited by safe operating area.*
3. *I_{SD} ≤ 15 A, di/dt ≤ 400 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	2.2	°C/W
R_{thJB}[(1)]	Thermal resistance, junction-to-board	59	°C/W

1. *When mounted on an 1-inch² FR-4, 2oz Cu board.*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 7.5 A		215	240	mΩ

1. *Specified by design, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1240	-	pF
C_{oss}	Output capacitance		-	32	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	99	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	30	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	3	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 7.5 A	-	31	-	nC
Q_{gs}	Gate-source charge	V_{GS} = 0 to 10 V	-	8	-	nC
Q_{gd}	Gate-drain charge	(see Figure 15. Test circuit for gate charge behavior)	-	14	-	nC

1. *$C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*
2. *$C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 9.5 A,	-	36	-	ns
$t_{r(v)}$	Voltage rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	7	-	ns
$t_{f(i)}$	Current fall time	(see Figure 16. Test circuit for inductive load switching and diode recovery times	-	9	-	ns
$t_{c(off)}$	Crossing time	and Figure 19. Switching time waveform)	-	11	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		15	A
I_{SDM} (2)	Source-drain current (pulsed)		-		60	A
V_{SD} (3)	Forward on voltage	I_{SD} = 15 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs,	-	290		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	3.4		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	23.5		A
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs,	-	352		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_J = 150 °C	-	4		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	24		A

1. *I_{SD} is limited by package.*
2. *Pulse width is limited by safe operating area.*
3. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

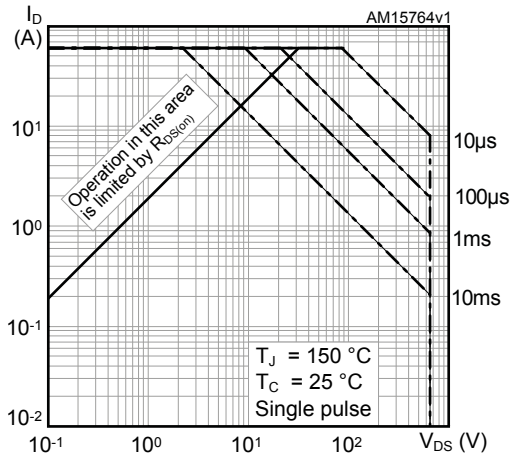


Figure 2. Normalized transient thermal impedance

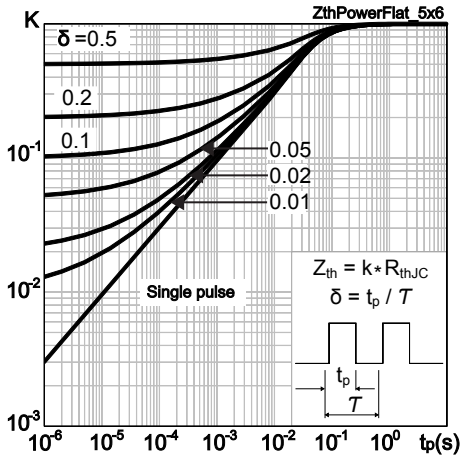


Figure 3. Typical output characteristics

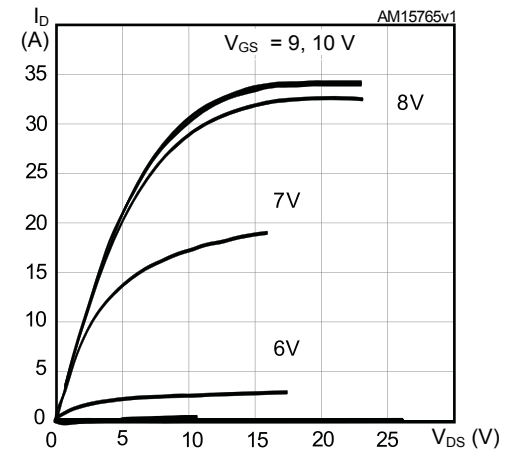


Figure 4. Typical transfer characteristics

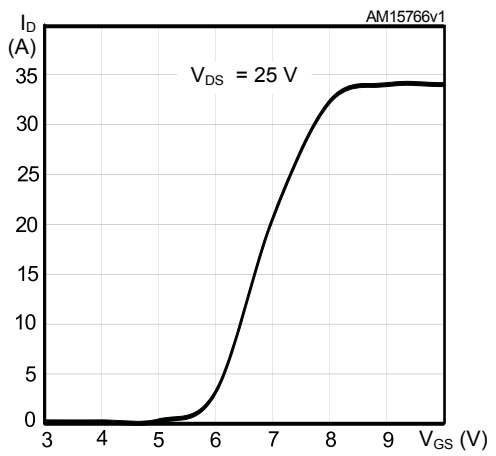


Figure 5. Typical gate charge characteristics

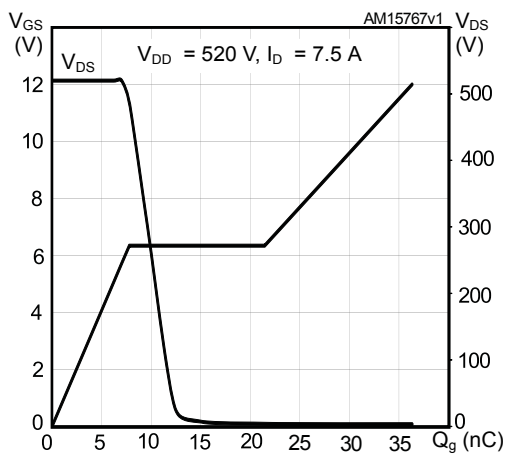


Figure 6. Typical drain-source on-resistance

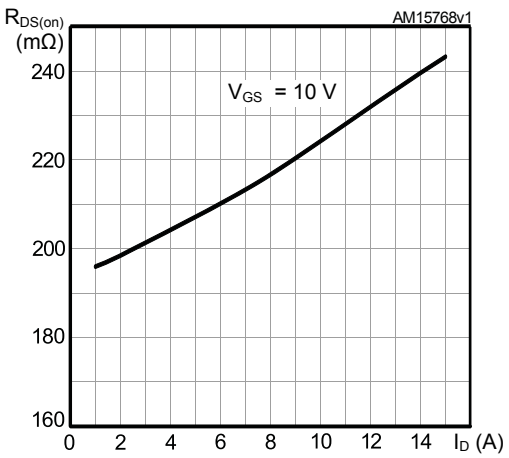


Figure 7. Typical capacitance characteristics

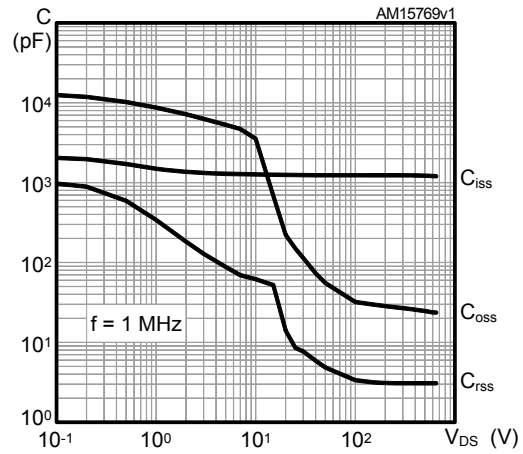


Figure 8. Typical output capacitance stored energy

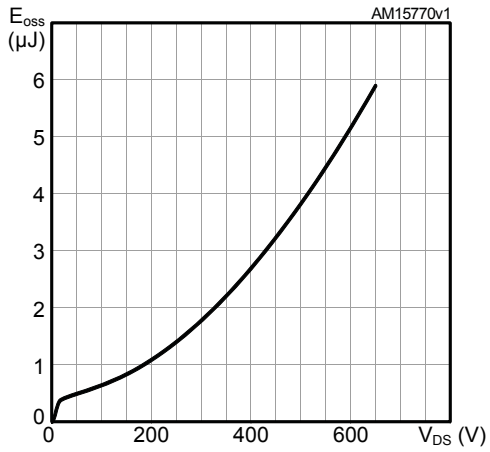


Figure 9. Normalized gate threshold voltage vs temperature

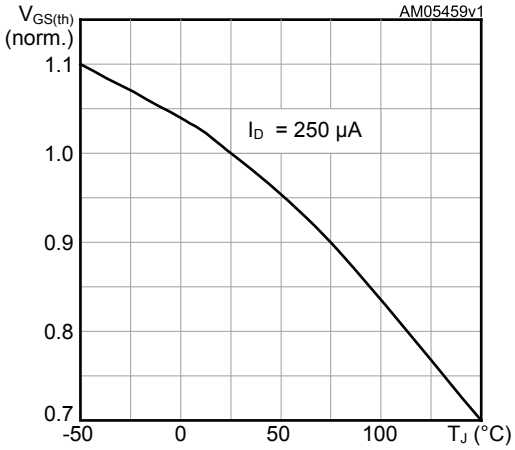


Figure 10. Normalized on-resistance vs temperature

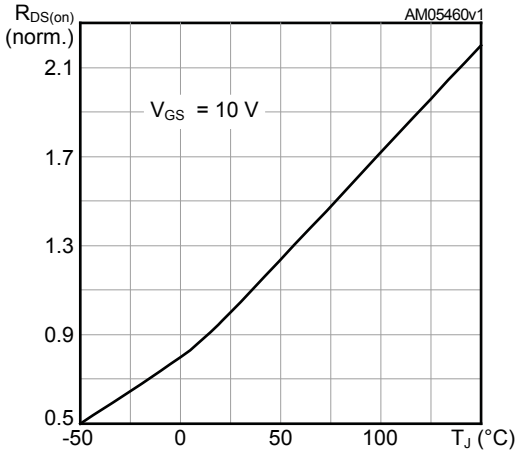


Figure 11. Normalized breakdown voltage vs temperature

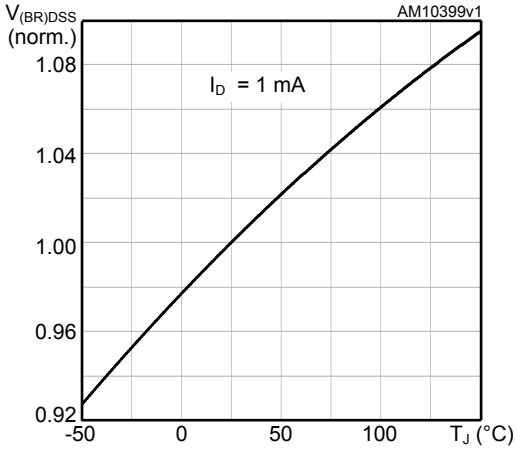


Figure 12. Typical reverse diode forward characteristics

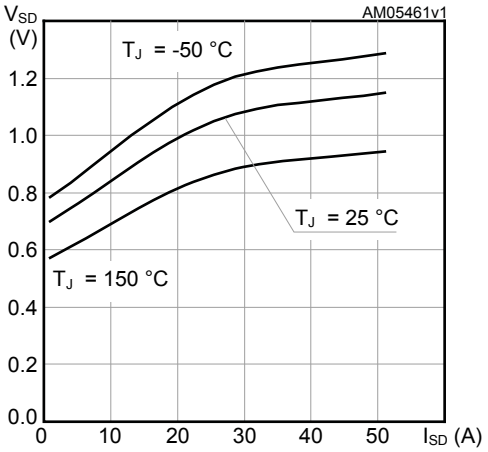
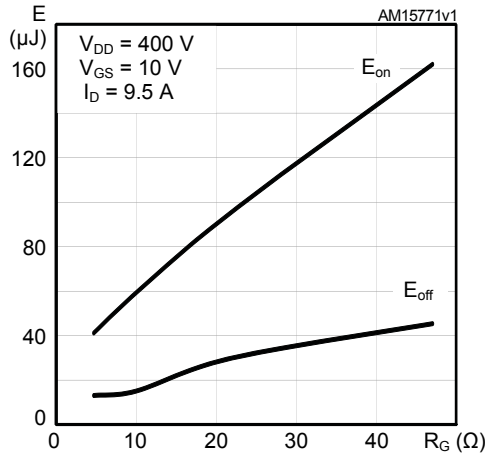


Figure 13. **Typical switching energy vs gate resistance**



3 Test circuits

Figure 14. Test circuit for resistive load switching times

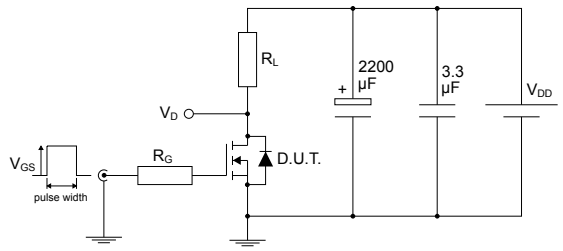


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Figure 15. Test circuit for gate charge behavior

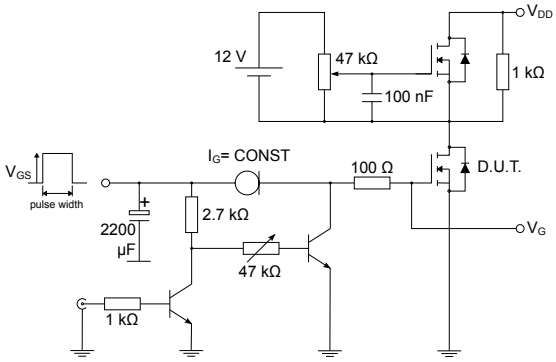

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Figure 16. Test circuit for inductive load switching and diode recovery times

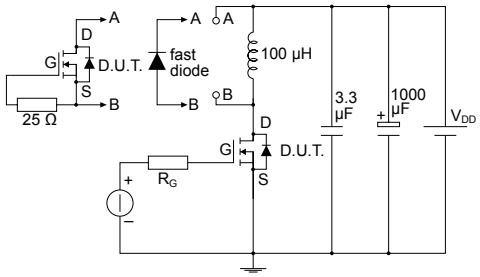

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Figure 17. Unclamped inductive load test circuit

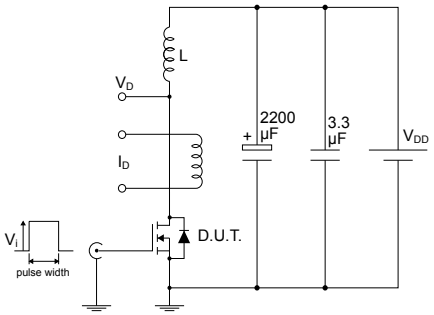

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Figure 18. Unclamped inductive waveform

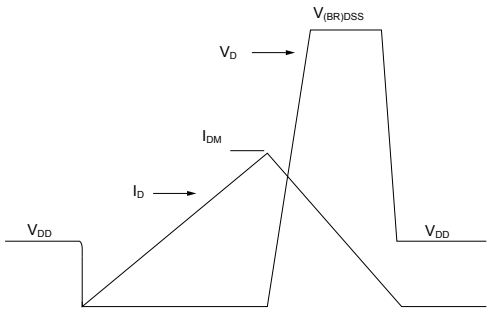

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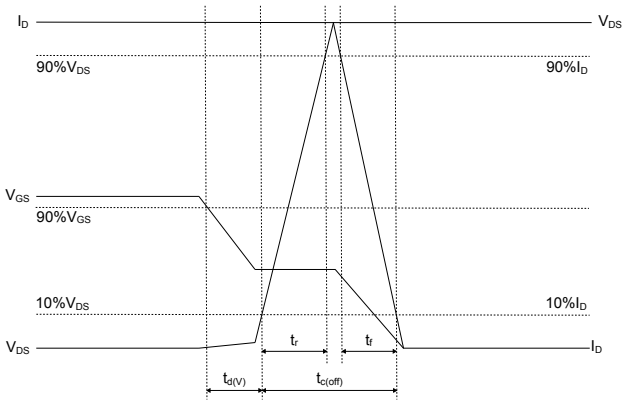
Figure 19. Switching time waveform



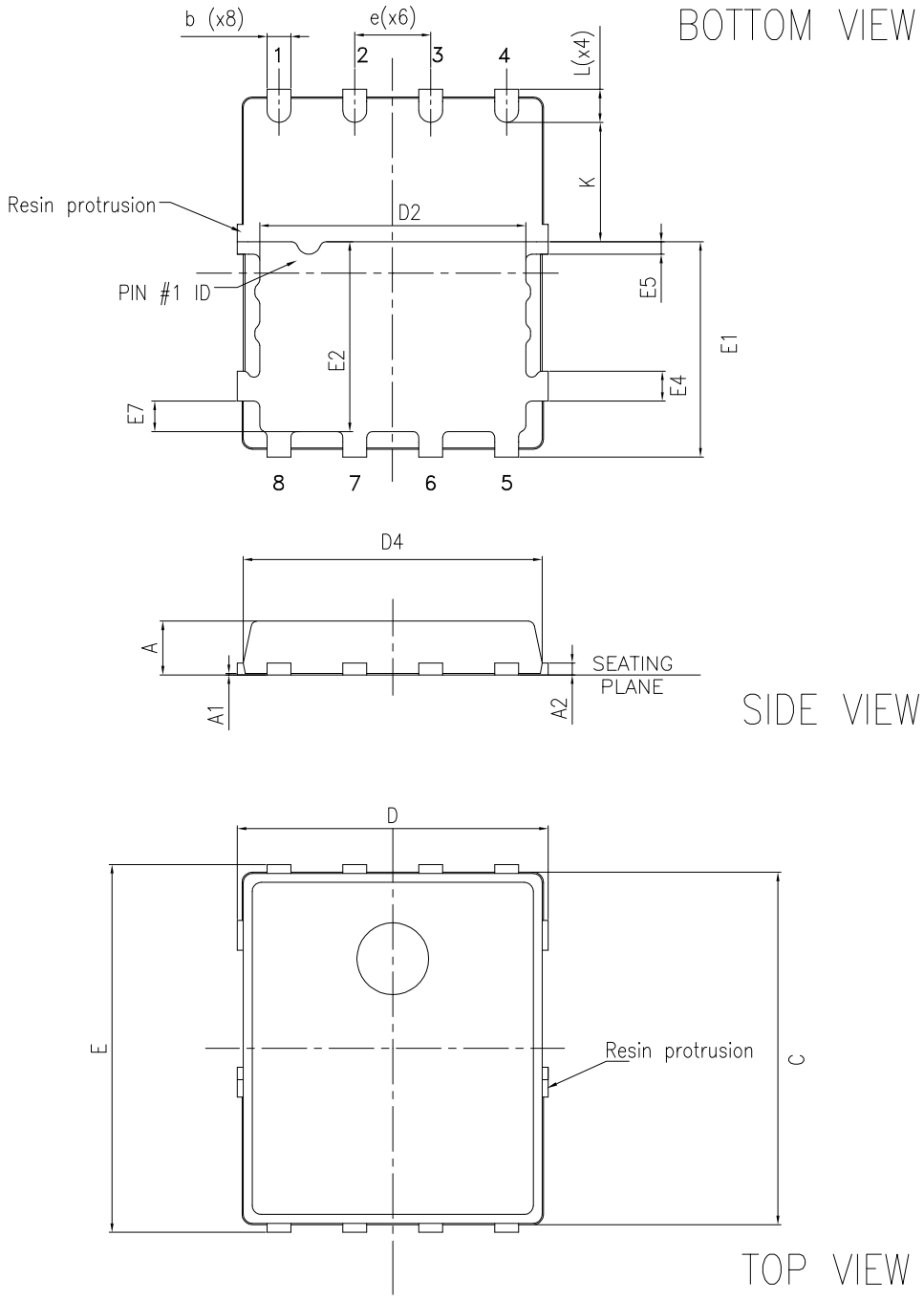
AM05540v2

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 HV package information

Figure 20. PowerFLAT 5x6 HV package outline

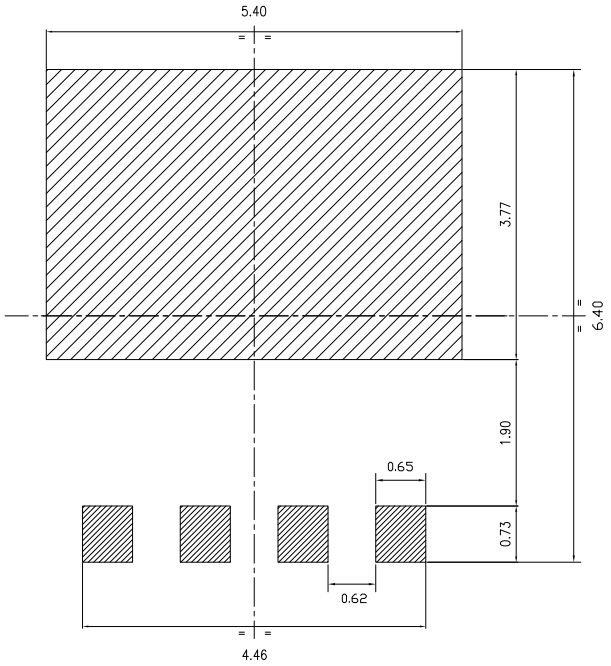


8368143_Rev_4

Table 7. **PowerFLAT 5x6 HV mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.60	5.80	6.00
D	5.10	5.20	5.30
D2	4.30	4.40	4.50
D4	4.60	4.80	5.00
E	6.05	6.15	6.25
E1	3.50	3.60	3.70
E2	3.10	3.20	3.30
E4	0.40	0.50	0.60
E5	0.10	0.20	0.30
E7	0.40	0.50	0.60
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

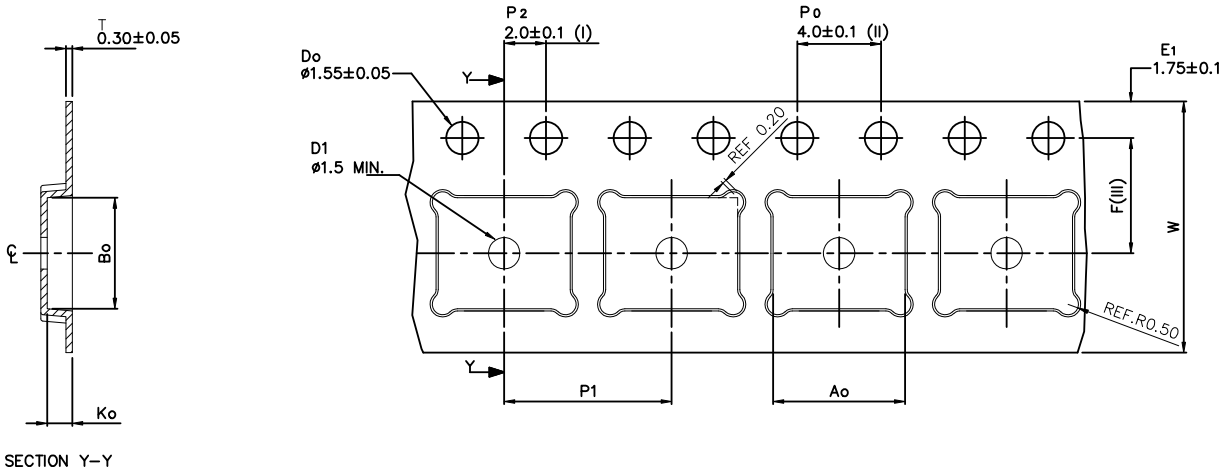
Figure 21. **PowerFLAT 5x6 HV recommended footprint (dimensions are in mm)**



8368143_Rev_4_footprint

4.2 PowerFLAT 5x6 packing information

Figure 22. **PowerFLAT 5x6 tape (dimensions are in mm)**



Ao	6.30 +/– 0.1
Bo	5.30 +/– 0.1
Ko	1.20 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ±0.20.

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 23. **PowerFLAT 5x6 package orientation in carrier tape**

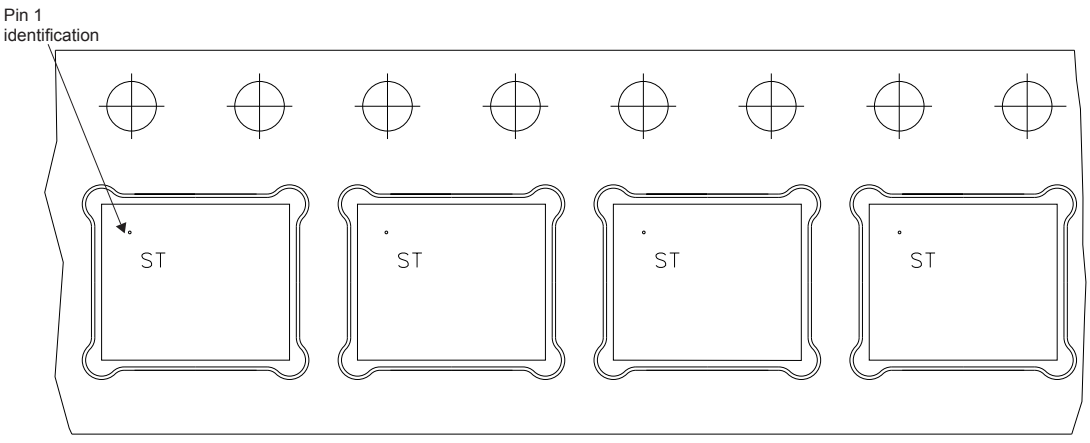
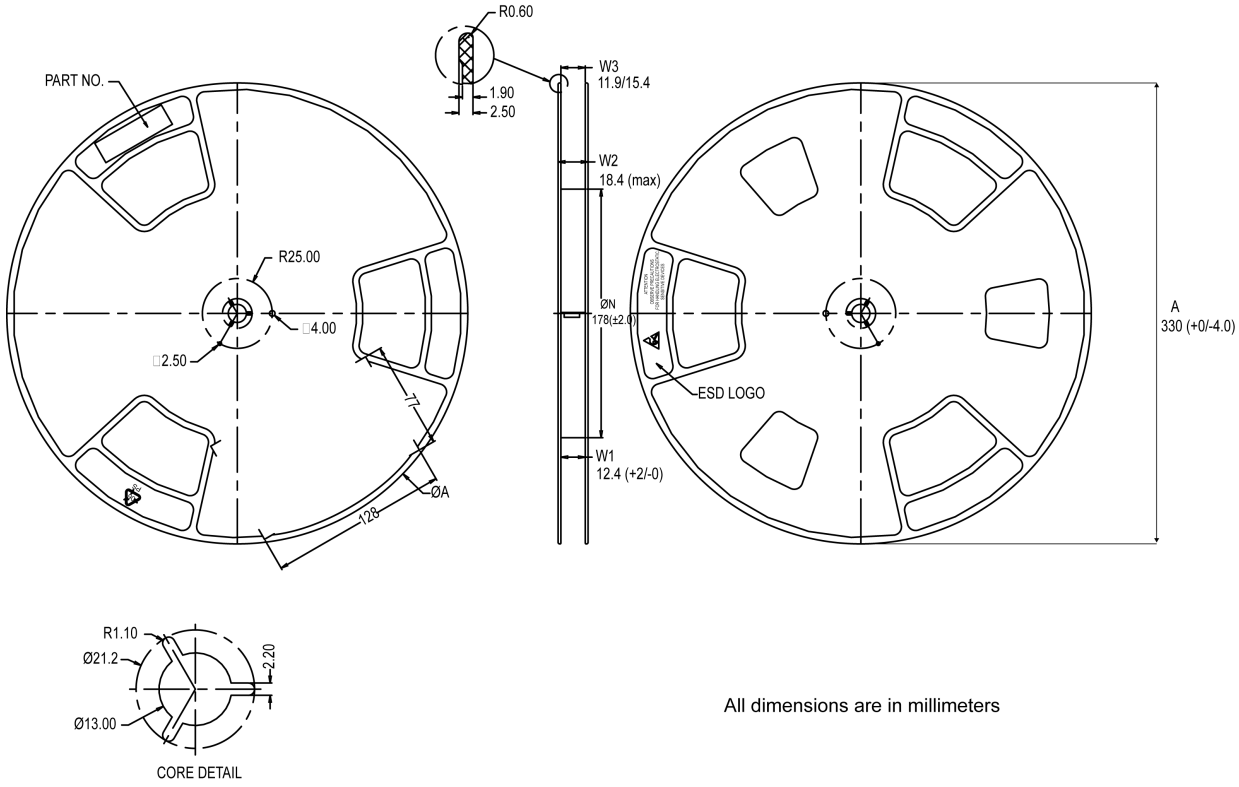


Figure 24. **PowerFLAT 5x6 reel**



All dimensions are in millimeters

8234350_Reel_rev_C

Revision history

Table 8. **Document revision history**

Date	Version	Changes
24-Apr-2013	1	First release.
26-Jun-2013	2	– Modified: *Figure 6*, *15*, *16*, *17*, *18*. – Minor text changes.
08-Mar-2022	3	Updated title, Features and Internal schematic on cover page. Updated Table 1. Absolute maximum ratings. Updated Section 4 Package information. Minor text changes.

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