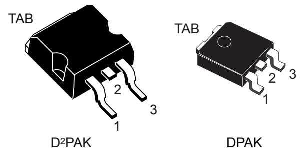
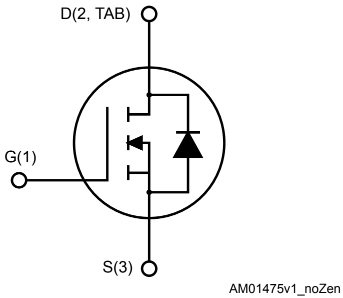
STB18N65M5, STD18N65M5

Datasheet

N-channel 650 V, 0.198 Ω typ., 15 A, MDmesh™ M5 Power MOSFETs in D²PAK and DPAK packages





Features

Order codes	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D
STB18N65M5	710 V	0.220 Ω	15 A
STD18N65M5			

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Product status link
STB18N65M5
STD18N65M5

Product summary	
STB18N65M5	
Order code	STB18N65M5
Marking	18N65M5
Package	D²PAK
Packing	Tape and reel
STD18N65M5	
Order code	STD18N65M5
Marking	18N65M5
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	15	A
	Drain current (continuous) at T_C = 100 °C	9.4	A
I_{DM} (1)	Drain current (pulsed)	60	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_j	Operating junction temperature range	-55 to 150	°C
T	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *$I_{SD} \leq 15$ A, di/dt ≤ 400 A/µs, V_{DD} = 400 V, $V_{DS(peak)} < V_{(BR)DSS}$.*

Table 2. **Thermal data**

Symbol	Parameter	Value		Unit
		D^2PAK	DPAK	
$R_{thj-case}$	Thermal resistance junction-case	1.14		°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-pcb	30	50	°C/W

1. *When mounted on an 1 inch² FR-4, 2 Oz copper board.*

Table 3. **Avalanche characteristics**

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_{jmax})	4	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	210	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C (1)			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 7.5 A		0.198	0.220	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1240	-	pF
C_{oss}	Output capacitance			32		
C_{rss}	Reverse transfer capacitance			3.2		
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	99	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related			30	-	
R_g	Gate input resistance	f = 1 MHz, I_D = 0 A	-	3	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 7.5 A, V_{GS} = 0 to 10 V (see Figure 17. Test circuit for gate charge behavior)	-	31	-	nC
Q_{gs}	Gate-source charge			8	-	
Q_{gd}	Gate-drain charge			14		

1. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 9.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 18. Test circuit for inductive load switching and diode recovery times and Figure 21. Switching time waveform)	-	36	-	ns
$t_{r(v)}$	Voltage rise time			7		
$t_{f(i)}$	Current fall time			9		
$t_{c(off)}$	Crossing time			11		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		15	A
I_{SDM}[1]	Source-drain current (pulsed)				60	
V_{SD}[2]	Forward on voltage	I_{SD} = 15 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs	-	290		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V		3.4		µC
I_{RRM}	Reverse recovery current	(see Figure 18. Test circuit for inductive load switching and diode recovery times)		23.5		A
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs	-	352		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_j = 150 °C		4		µC
I_{RRM}	Reverse recovery current	(see Figure 18. Test circuit for inductive load switching and diode recovery times)		24		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for D^2PAK

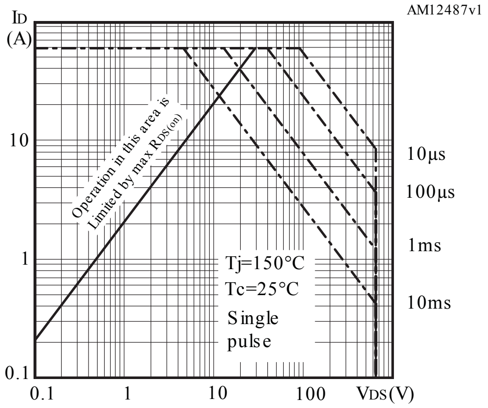


Figure 2. Thermal impedance for D^2PAK

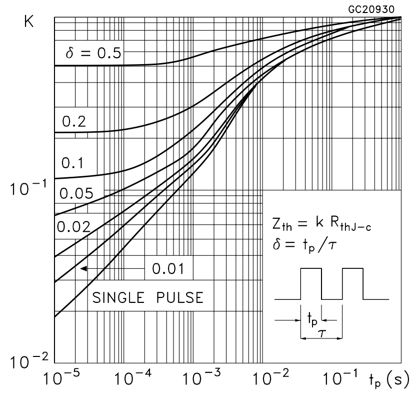


Figure 3. Safe operating area for DPAK

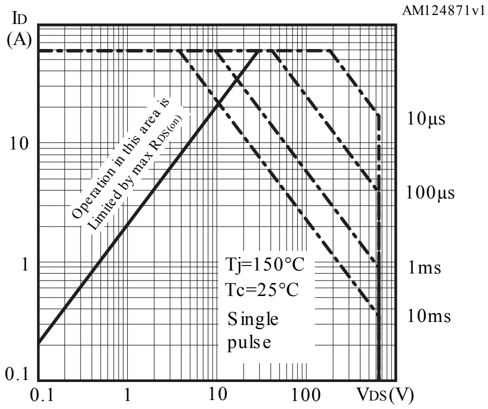


Figure 4. Thermal impedance for DPAK

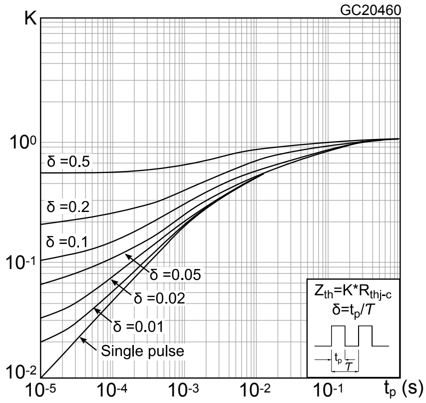


Figure 5. Output characteristics

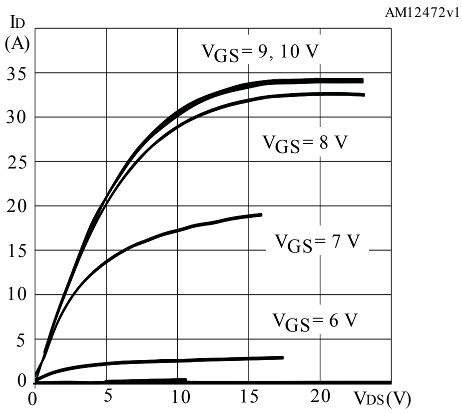


Figure 6. Transfer characteristics

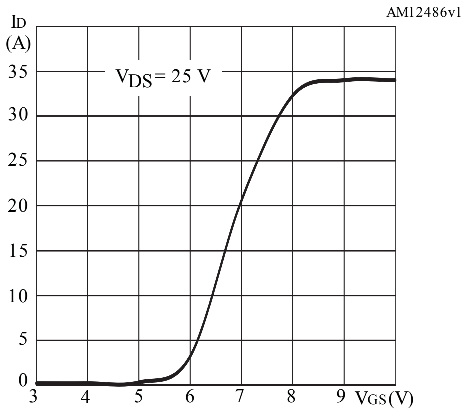


Figure 7. Gate charge vs gate-source voltage

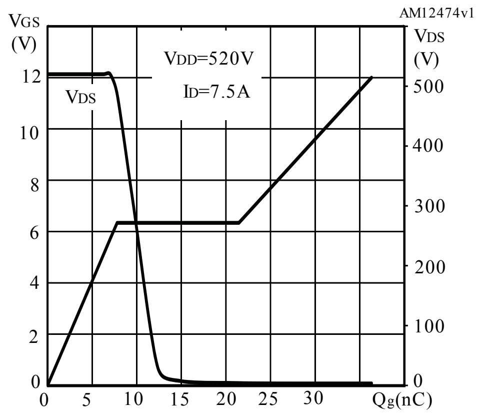


Figure 8. Static drain-source on-resistance

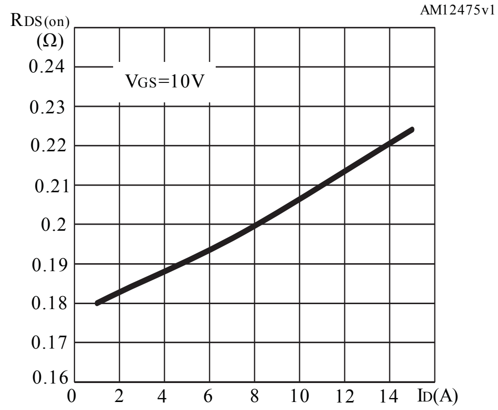


Figure 9. Capacitance variations

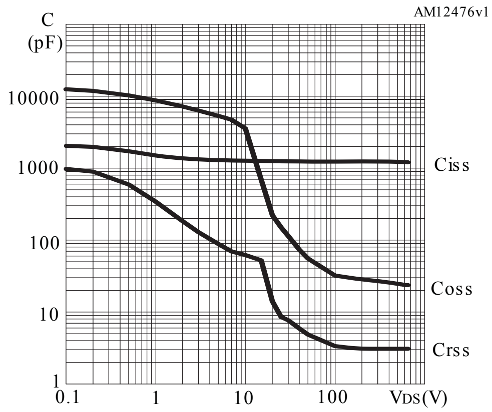


Figure 10. Output capacitance stored energy

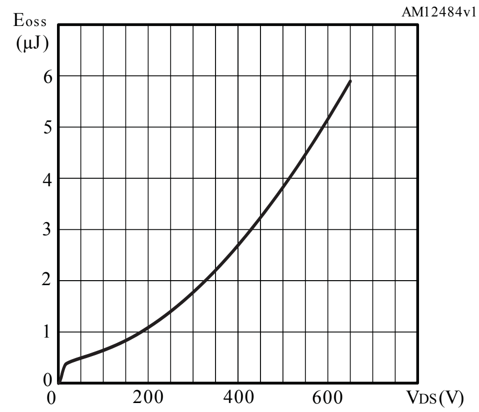


Figure 11. Normalized gate threshold voltage vs temperature

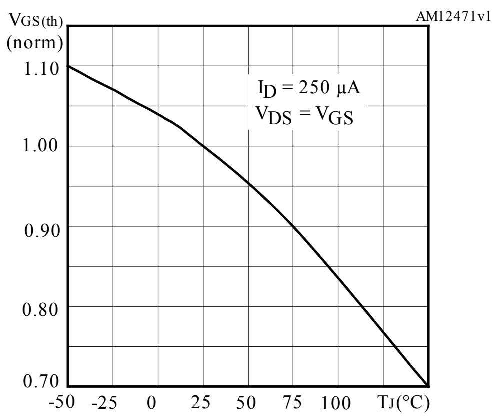


Figure 12. Normalized on-resistance vs temperature

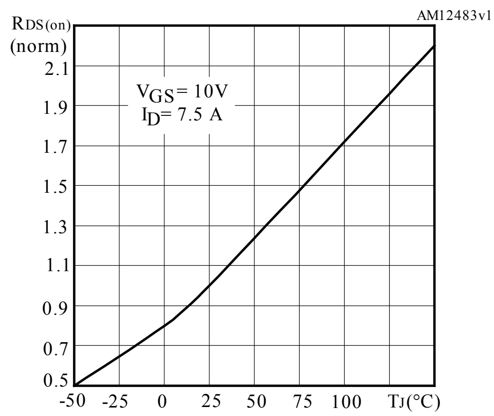


Figure 13. Source-drain diode forward characteristics

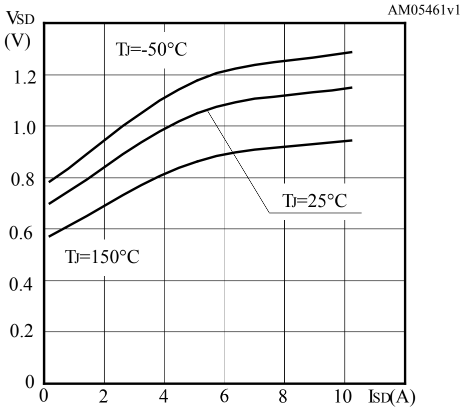


Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

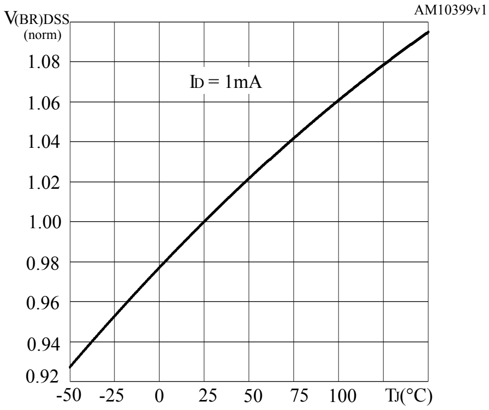
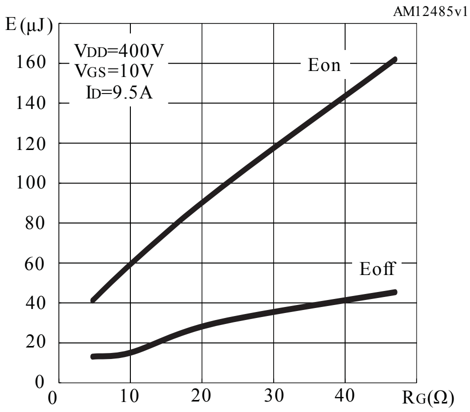


Figure 15. Switching losses vs gate resistance



3 Test circuits

Figure 16. Test circuit for resistive load switching times

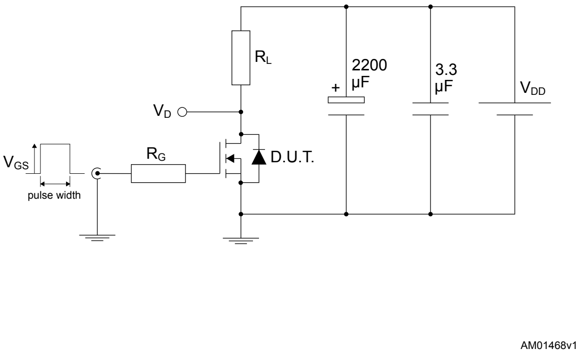


Figure 17. Test circuit for gate charge behavior

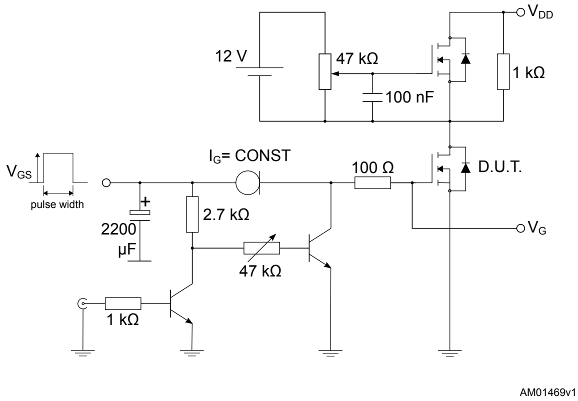


Figure 18. Test circuit for inductive load switching and diode recovery times

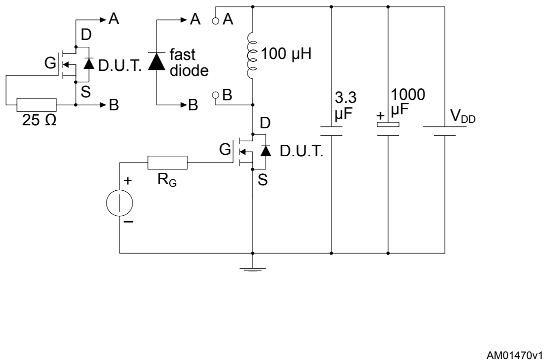


Figure 19. Unclamped inductive load test circuit

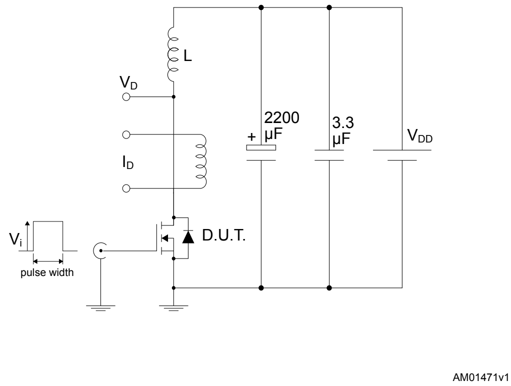


Figure 20. Unclamped inductive waveform

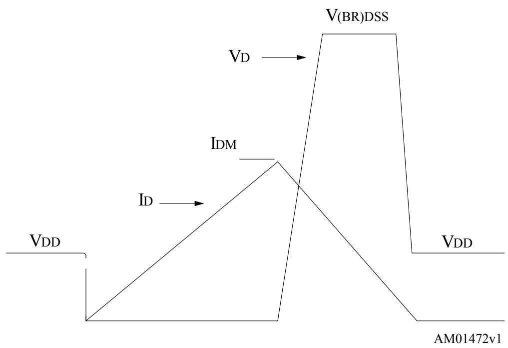
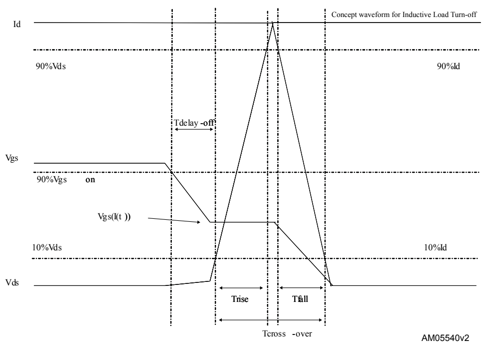


Figure 21. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A package information

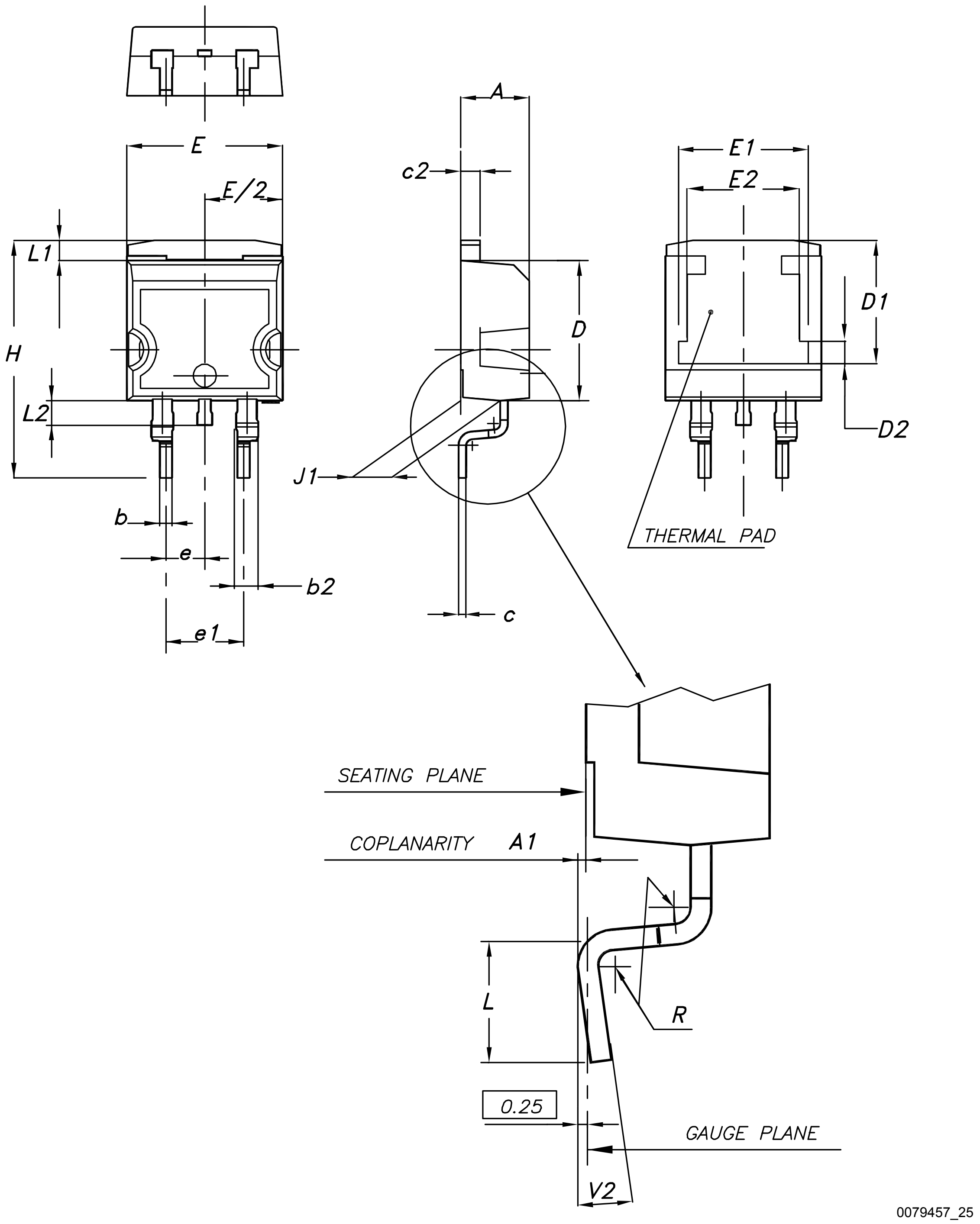
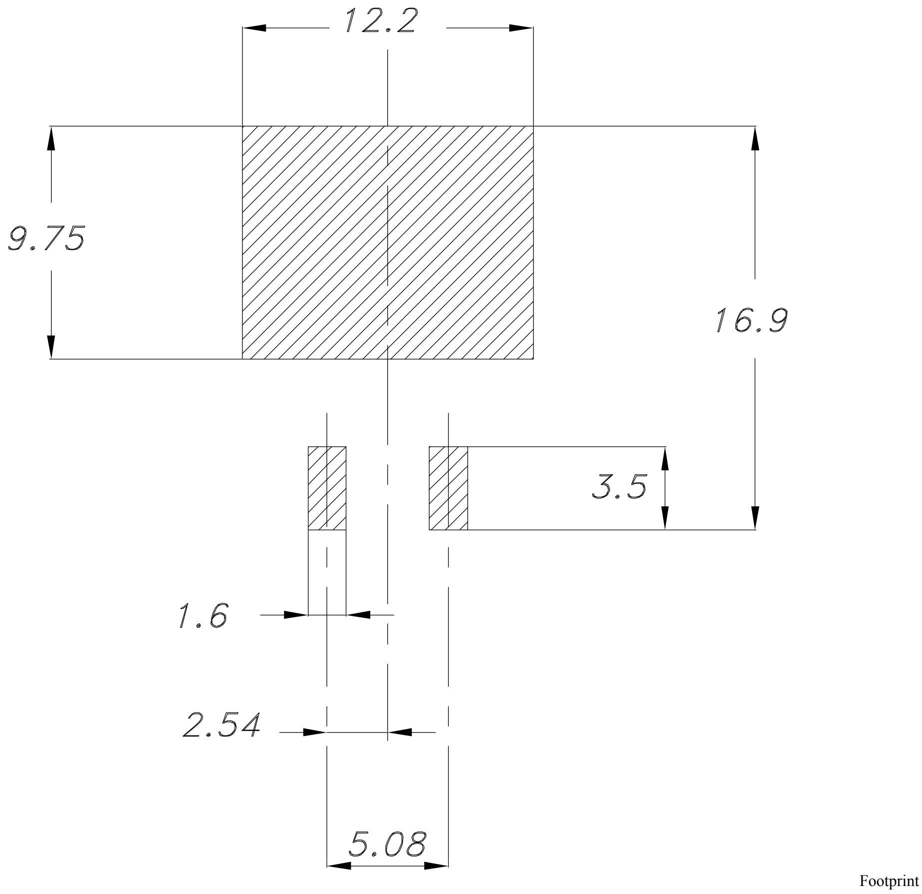


Figure 22. D²PAK (TO-263) type A package outline

Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 23. D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) type A2 package information

Figure 24. **DPAK (TO-252) type A2 package outline**

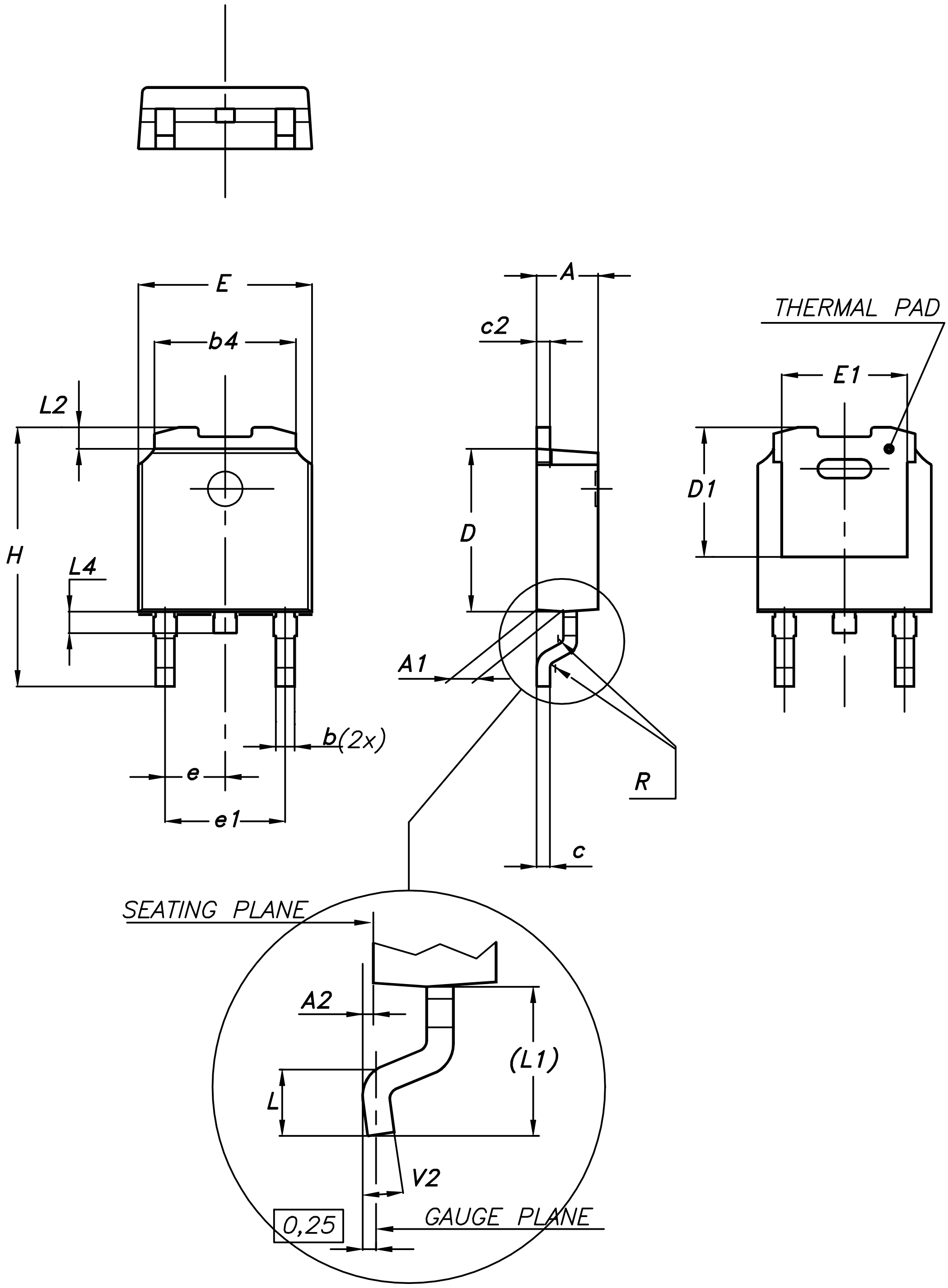


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Table 9. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.3 DPAK (TO-252) type C2 package information

Figure 25. **DPAK (TO-252) type C2 package outline**

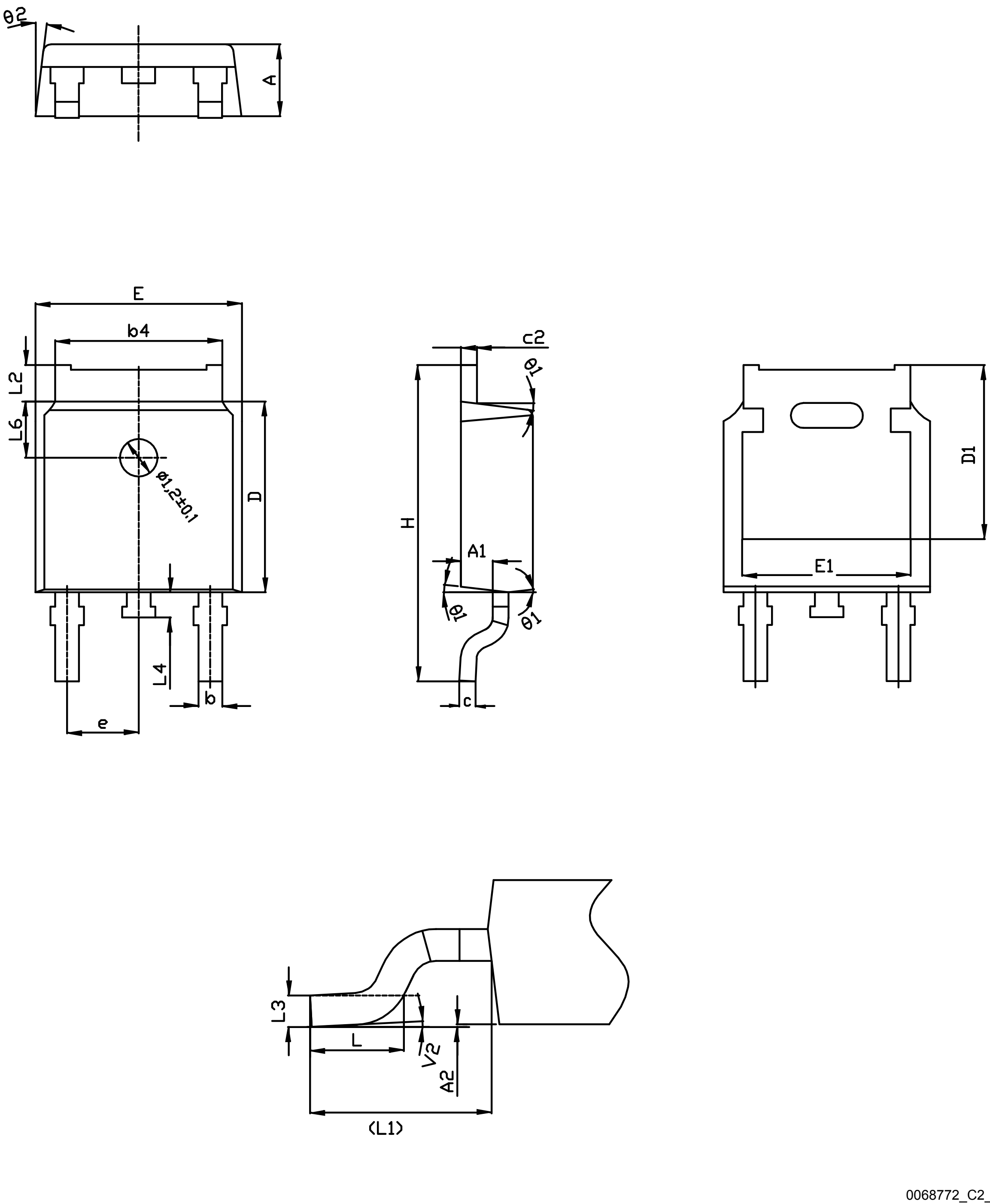
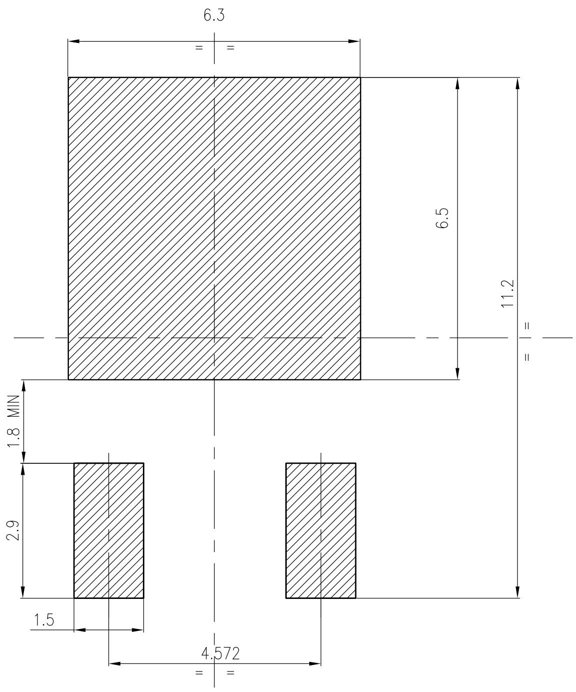


Table 10. DPAK (TO-252) type C2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 26. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



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4.4 D²PAK and DPAK packing information

Figure 27. Tape outline

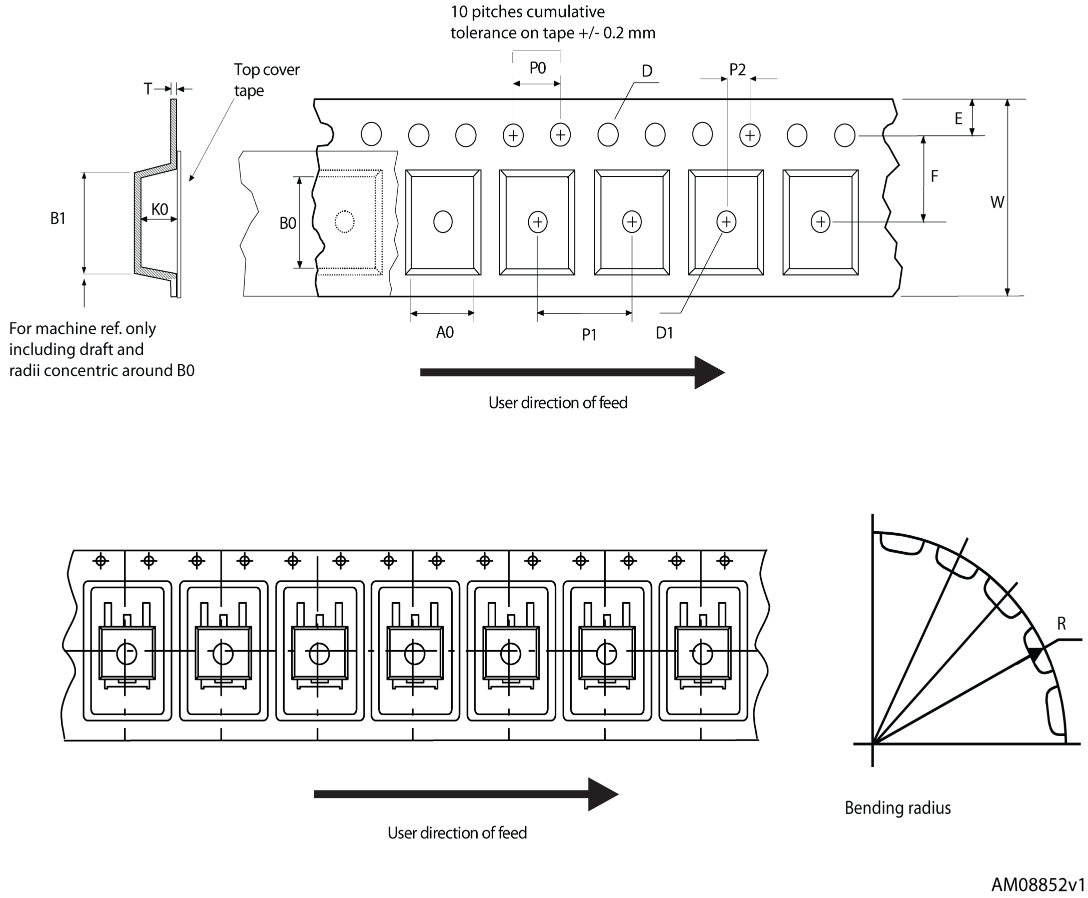

Figure 28. Reel outline

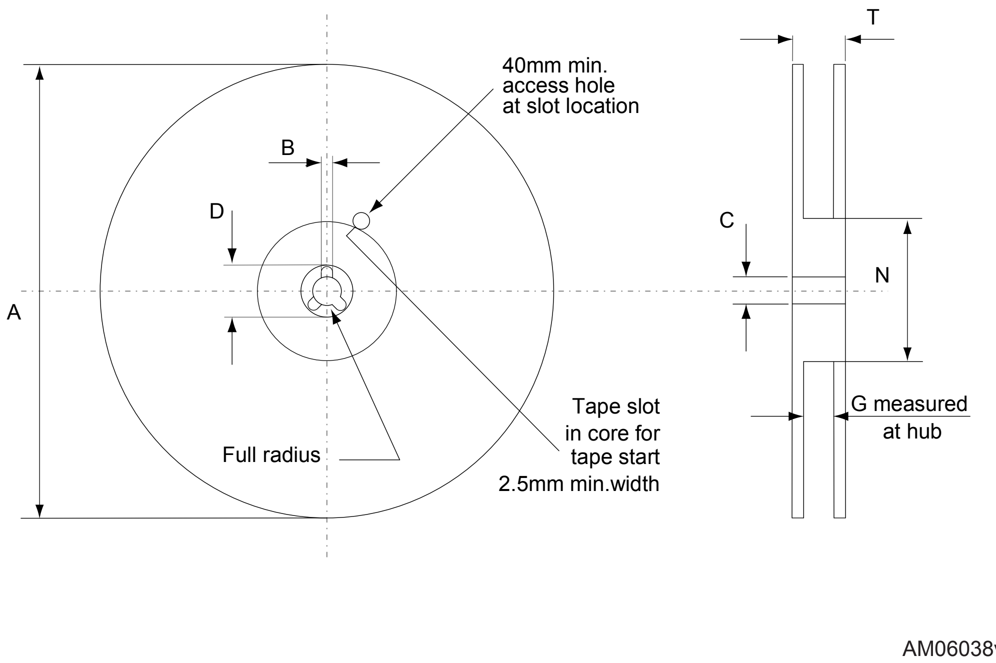

Table 11. D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 12. **DPAK tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 13. Document revision history

Date	Version	Changes
18-Jul-2012	1	First release.
09-Aug-2018	2	Removed maturity status indication from cover page. The document status is production data. Updated Section 4 Package information. Minor text changes

Contents