STF6N62K3, STFI6N62K3, STI6N62K3, STP6N62K3, STU6N62K3

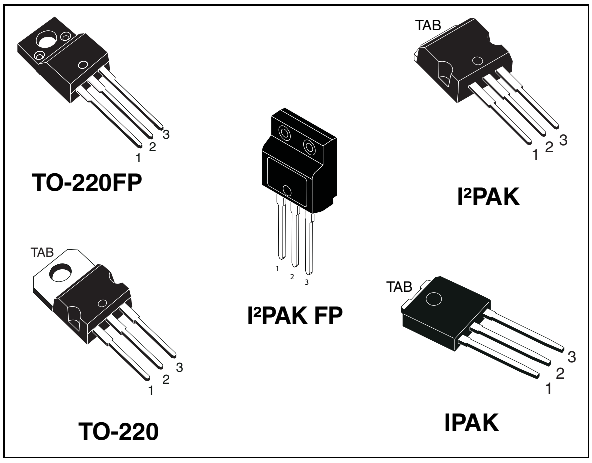
N-channel 620 V, 0.95 Ω typ., 5.5 A SuperMESH3™ Power MOSFET in TO-220FP, I²PAKFP, I²PAK, TO-220, IPAK packages

Datasheet — production data

Features

Order codes	V_{DSS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STF6N62K3	620 V	< 1.2 Ω	5.5 A	30 W
STFI6N62K3				30 W
STI6N62K3				90 W
STP6N62K3				90 W
STU6N62K3				90 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected



Applications

- Switching applications

Description

These SuperMESH3™ Power MOSFETs are the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

Figure 1. Internal schematic diagram

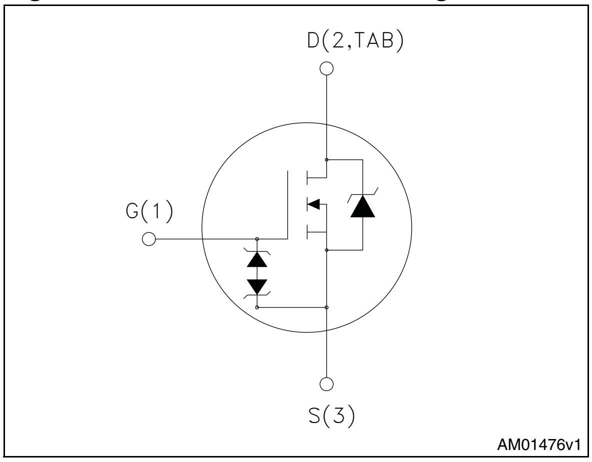


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF6N62K3	6N62K3	TO-220FP	Tube
STFI6N62K3		I²PAKFP	
STI6N62K3		I²PAK	
STP6N62K3		TO-220	
STU6N62K3		IPAK	

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Contents

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-220FP I²PAKFP	I²PAK TO-220	IPAK	
V_{DS}	Drain-source voltage	620			V
V_{GS}	Gate- source voltage	± 30			V
I_D	Drain current (continuous) at T_C = 25 °C	5.5 (1)	5.5		A
I_D	Drain current (continuous) at T_C = 100 °C	3 (1)	3		A
I_{DM} (2)	Drain current (pulsed)	22 (1)	22		A
P_{TOT}	Total dissipation at T_C = 25 °C	30	90		W
I_{AR} (3)	Avalanche current, repetitive or not-repetitive	5.5			A
E_{AS} (4)	Single pulse avalanche energy	140			mJ
ESD	Gate-source human body model (R=1.5 kΩ, C=100 pF)	2.5			kV
dv/dt (5)	Peak diode recovery voltage slope	12			V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; Tc = 25 °C)	2500			V
T_{stg}	Storage temperature	-55 to 150			°C
T_j	Max. operating junction temperature	150			°C

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. Pulse width limited by Tj max.
4. Starting Tj = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V.
5. $I_{SD} \leq$ 5.5 A, di/dt $\leq$ 400 A/µs, V_{DD} = 80% $V_{(BR)DSS}$, $V_{DSpeak} \leq V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	TO-220FP I²PAKFP	I²PAK TO-220	IPAK	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	4.17	1.39		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max.	62.5		100	°C/W

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2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	620			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 620 V V_{DS} = 620 V, T_C=125 °C			0.8 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 9	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.8 A		0.95	1.2	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	875 100 17	-	pF pF pF
$C_{oss(er)}$ (1)	Equivalent output capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 480 V	-	28	-	pF
$C_{oss(tr)}$ (2)	Equivalent output capacitance time related		-	63	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 496 V, I_D = 5.5 A, V_{GS} = 10 V (see *Figure 20*)	-	34 4 22	-	nC nC nC

1. Is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Is defined as a constant equivalent capacitance giving the same storage energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

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Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 310 V, I_D = 2.75 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 19*)	-	22 12 49 20	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		5.5 27	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 5.5 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5.5 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 24*)	-	290 1.9 13.5		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5.5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 24*)	-	335 2.4 14.5		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage (I_D = 0)	Igs=± 1 mA	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

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2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, I²PAK

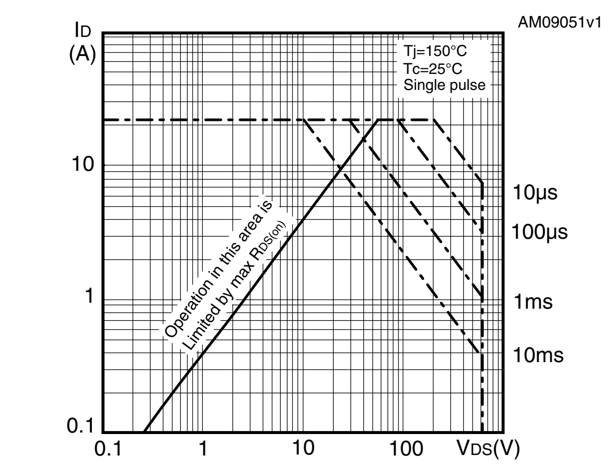

Figure 3. Thermal impedance for TO-220, I²PAK

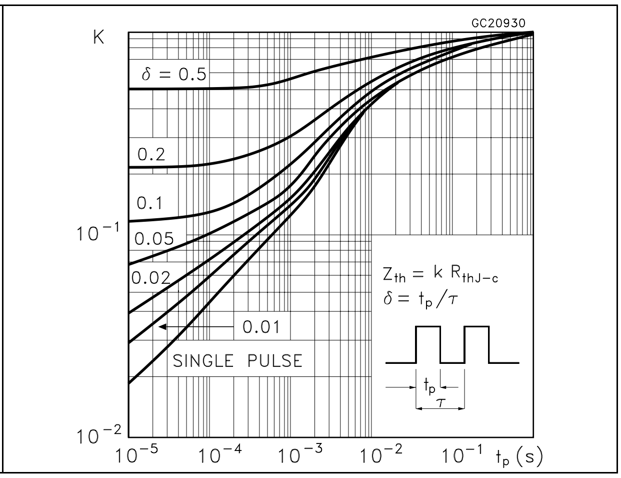

Figure 4. Safe operating area for TO-220FP, I²PAKFP

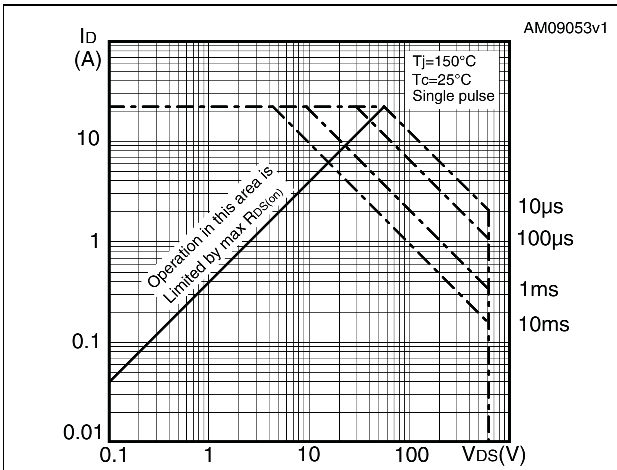

Figure 5. Thermal impedance for TO-220FP, I²PAKFP

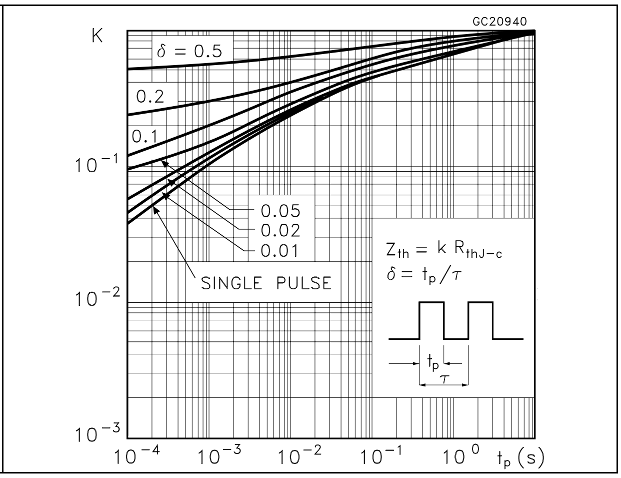

Figure 6. Safe operating area for IPAK

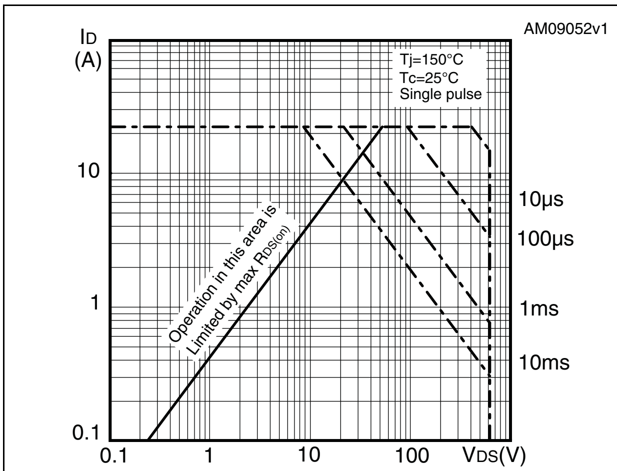

Figure 7. Thermal impedance for IPAK

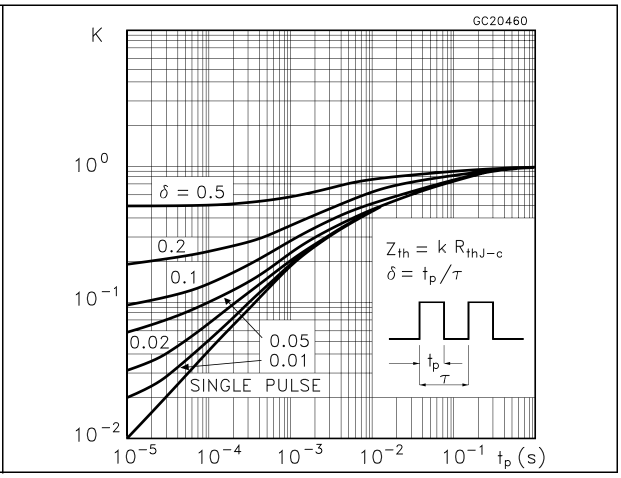

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Figure 8. Output characteristics

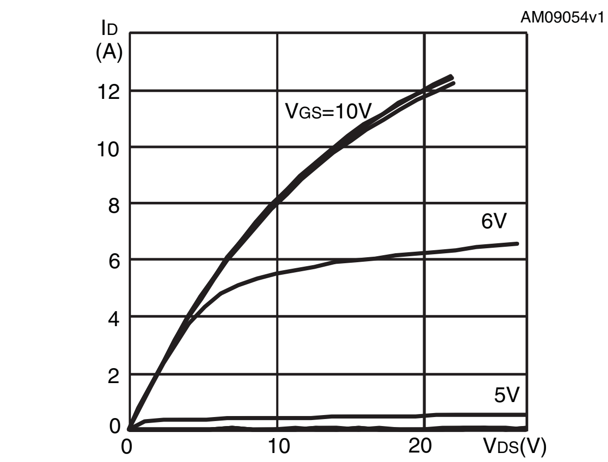

Figure 9. Transfer characteristics

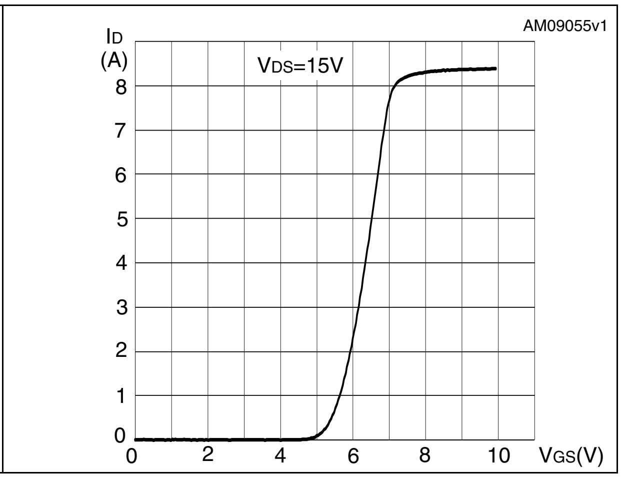

Figure 10. Gate charge vs gate-source voltage

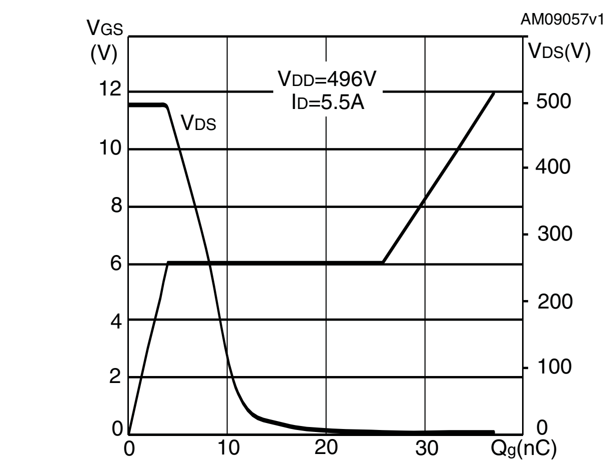

Figure 11. Static drain-source on-resistance

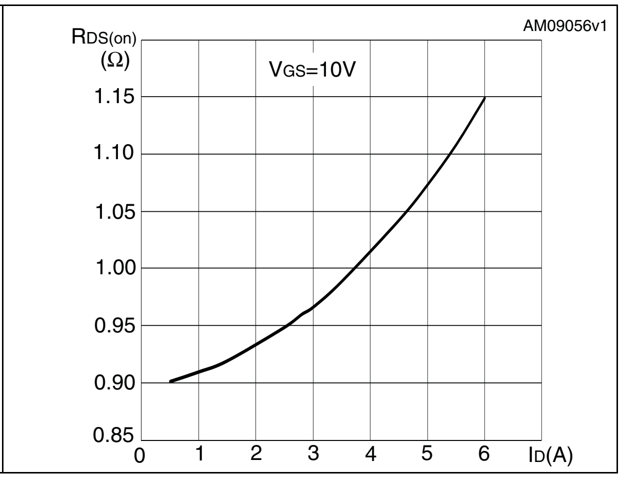

Figure 12. Capacitance variations

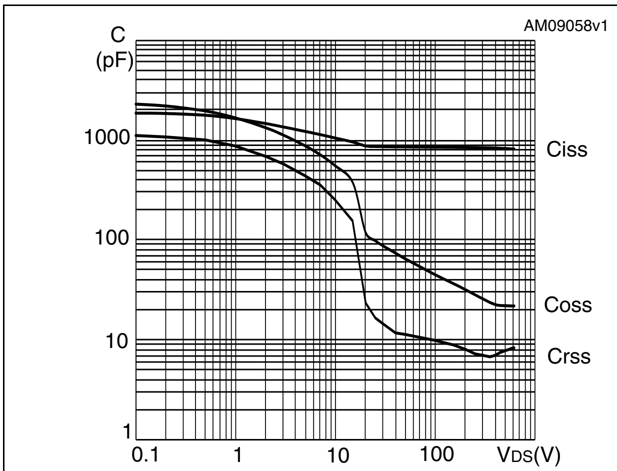

Figure 13. Output capacitance stored energy

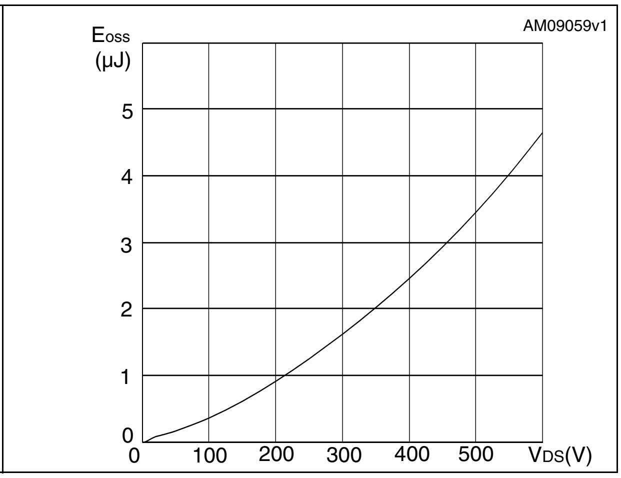

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Figure 14. Normalized gate threshold voltage vs temperature

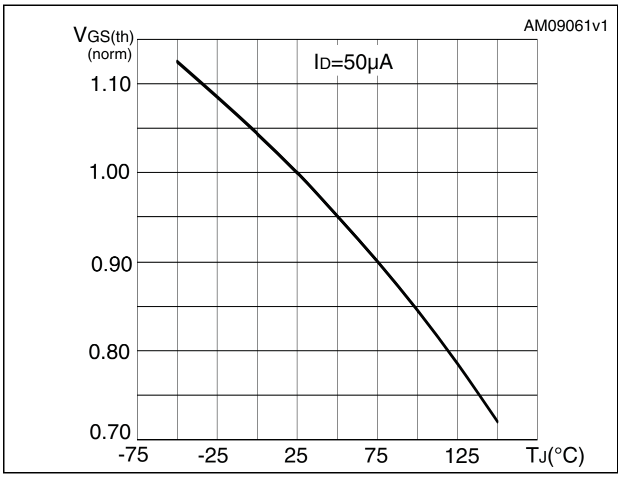


Figure 15. Normalized on-resistance vs temperature

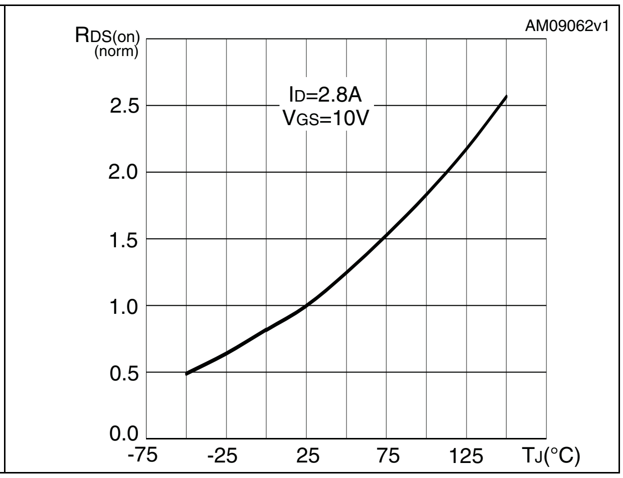


Figure 16. Normalized B_{VDSS} vs temperature

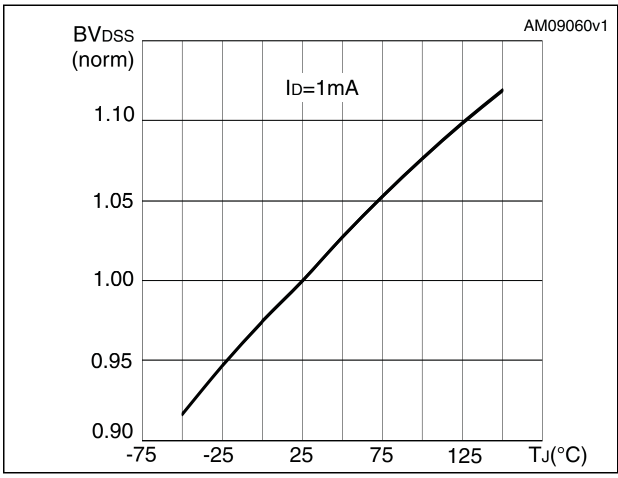


Figure 17. Source-drain diode forward characteristics

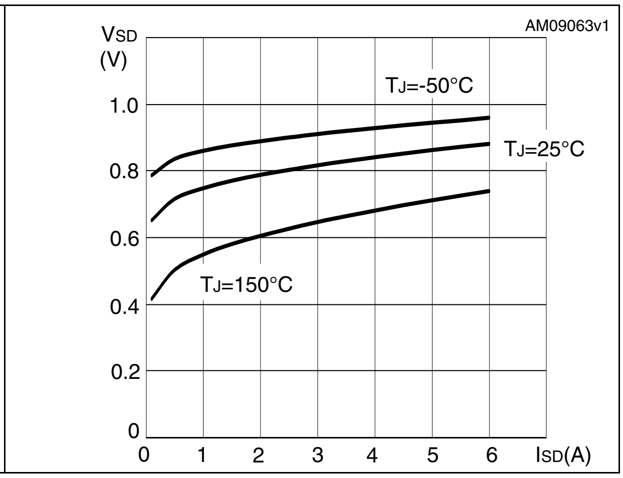
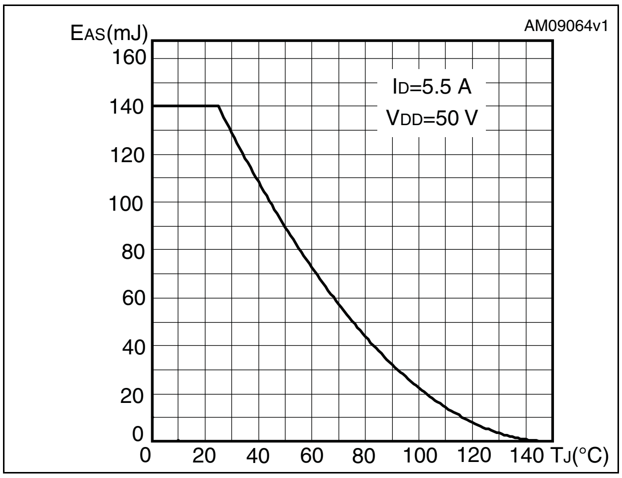


Figure 18. Maximum avalanche energy vs temperature



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3 Test circuits

Figure 19. Switching times test circuit for resistive load

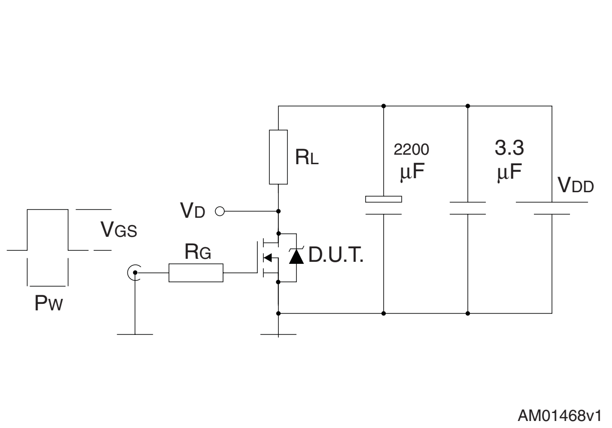


Figure 20. Gate charge test circuit

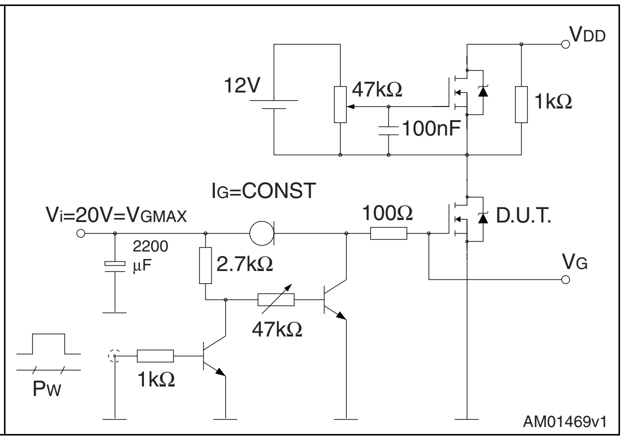


Figure 21. Test circuit for inductive load switching and diode recovery times

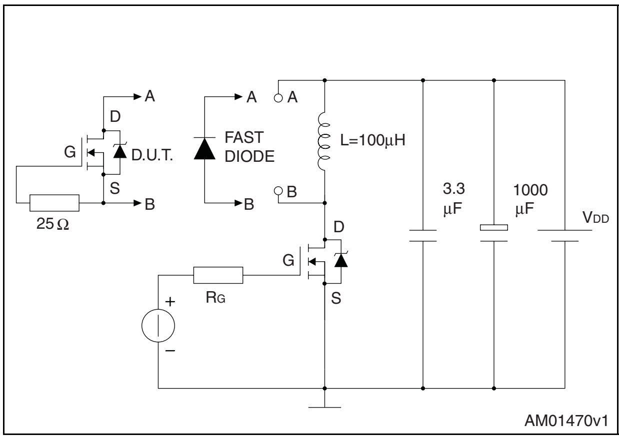


Figure 22. Unclamped Inductive load test circuit

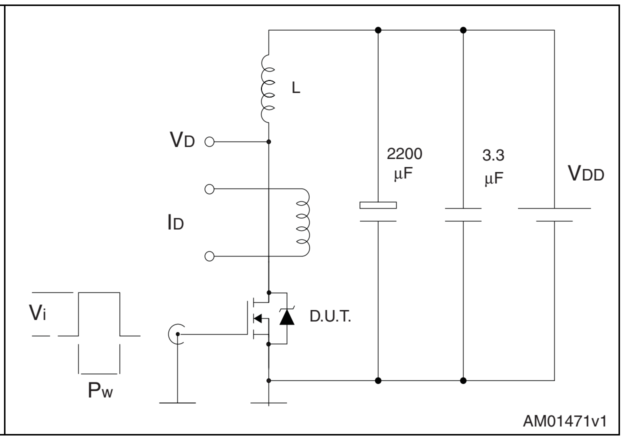


Figure 23. Unclamped inductive waveform

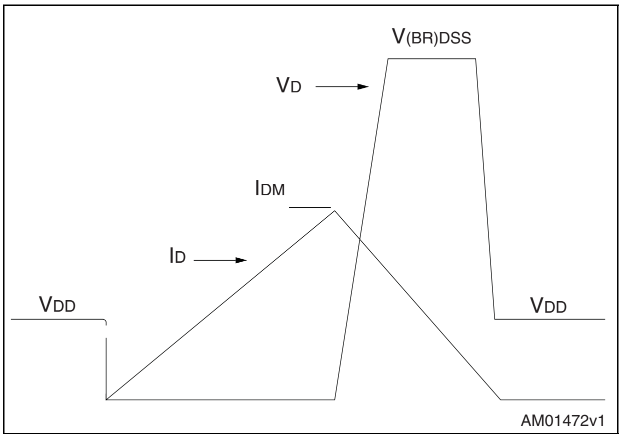
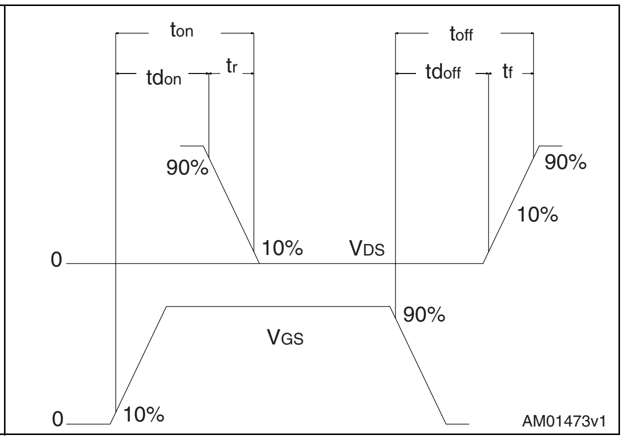


Figure 24. Switching time waveform



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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

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Figure 25. TO-220FP drawing

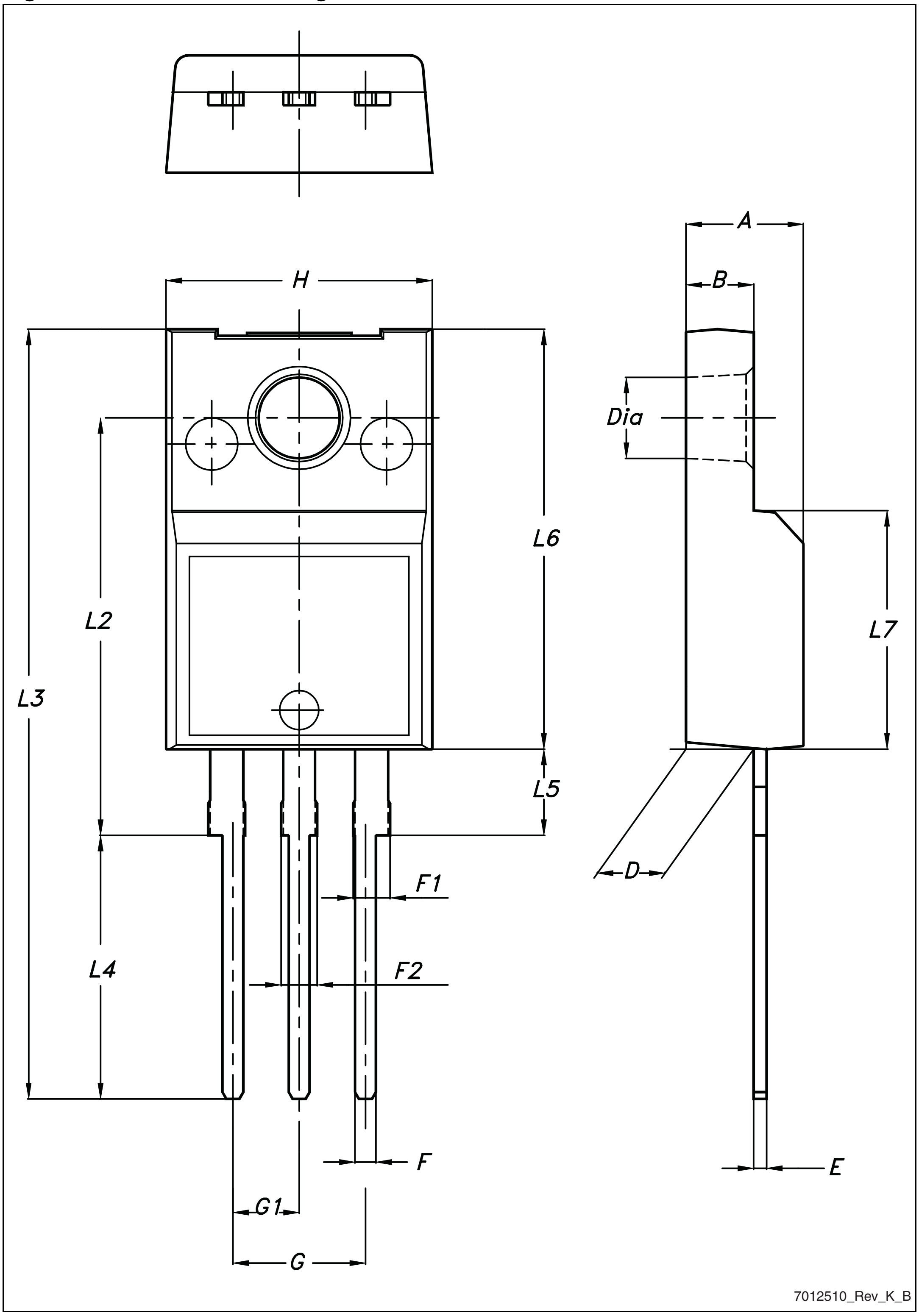

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Table 10. I^2PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 26. I^2PAKFP (TO-281) drawing

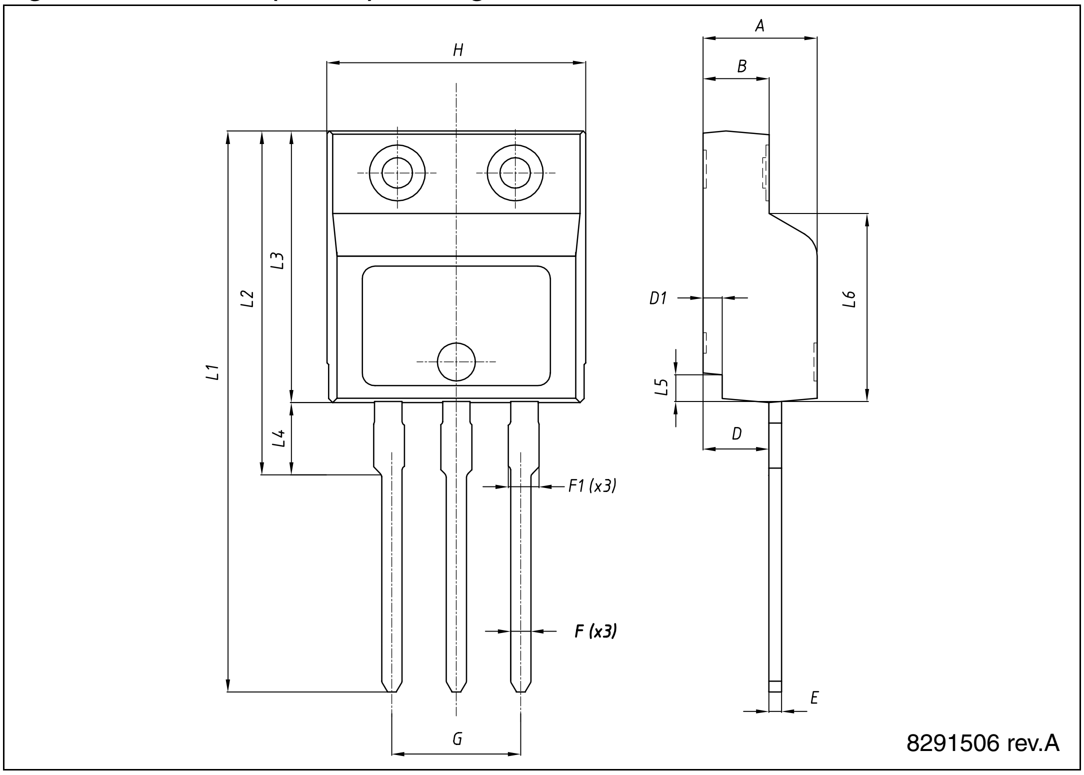

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Table 11. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 27. I²PAK (TO-262) drawing

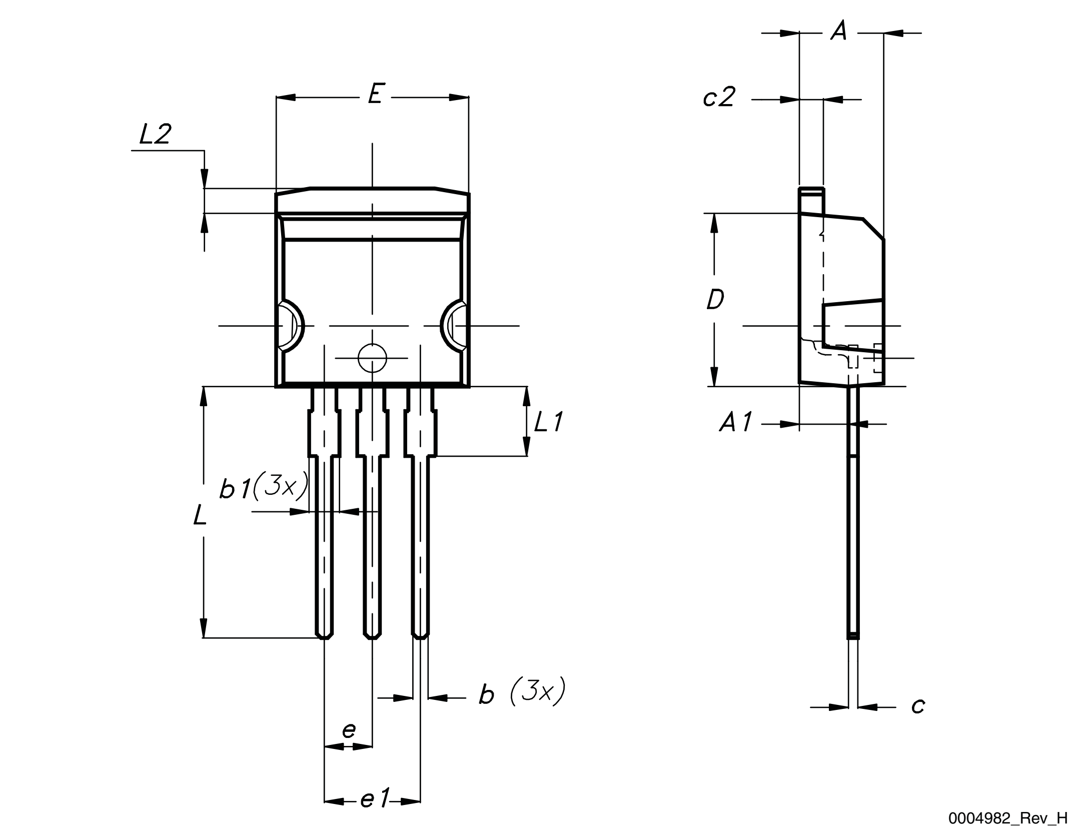

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Table 12. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

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Figure 28. TO-220 type A drawing

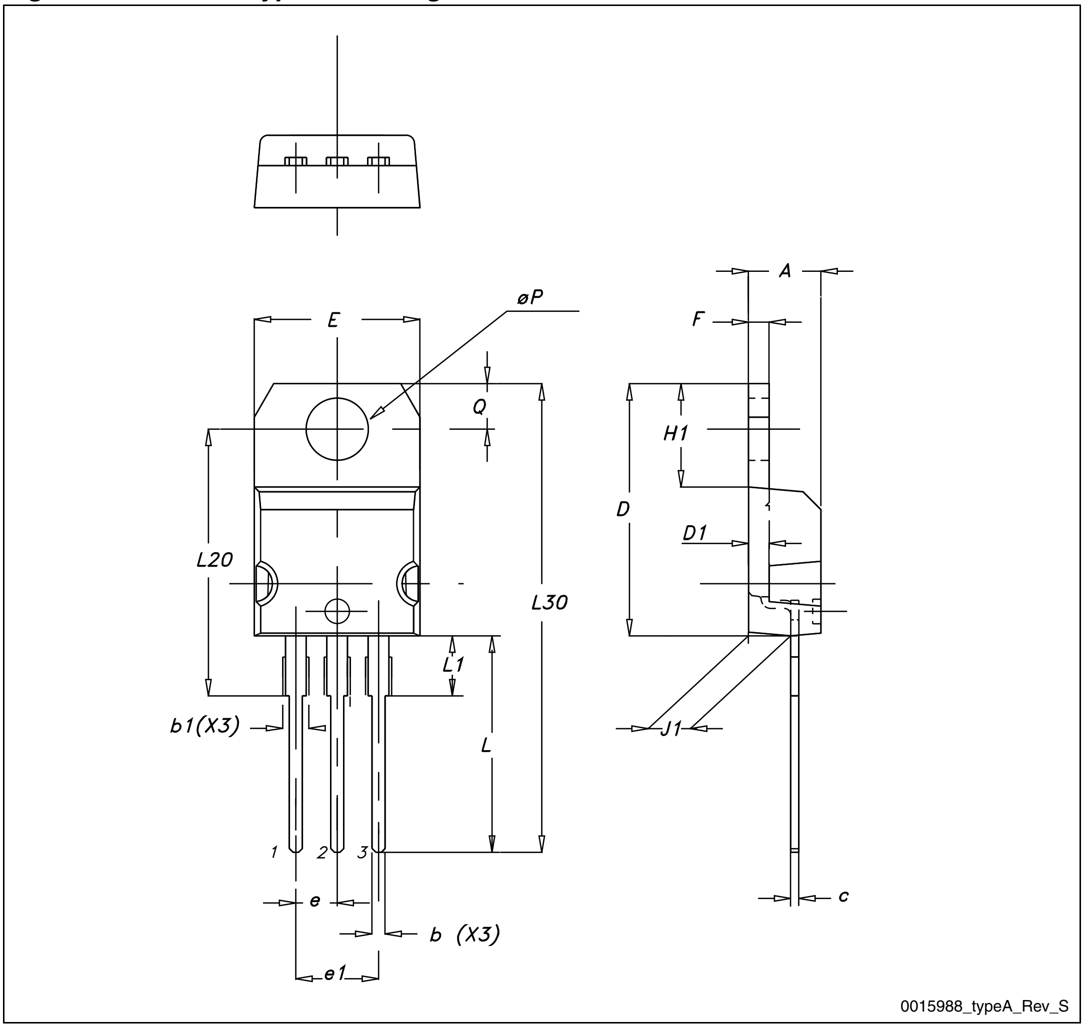

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Table 13. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

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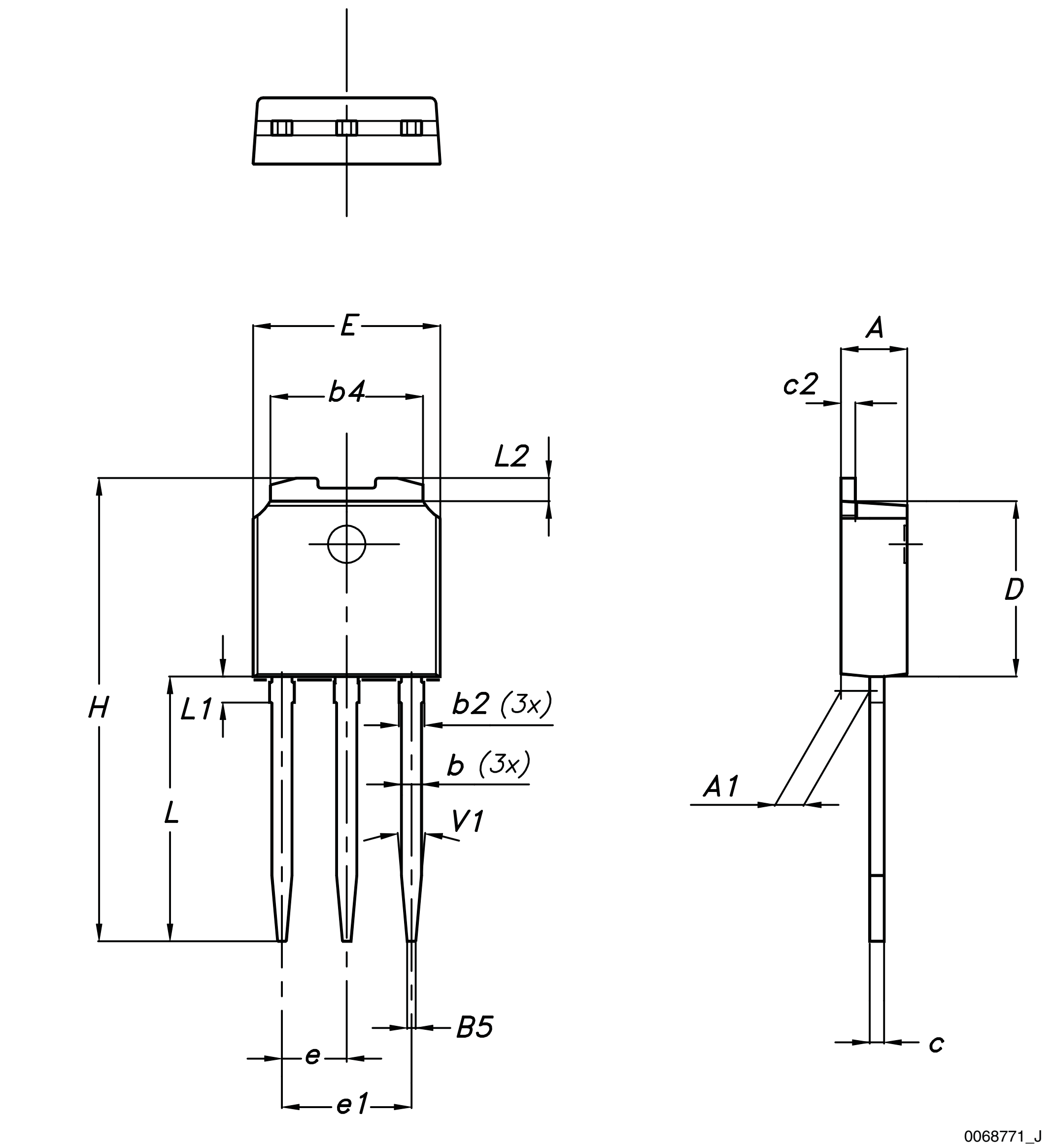
Figure 29. IPAK (TO-251) drawing



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5 Revision history

Table 14. Document revision history

Date	Revision	Changes
19-May-2006	1	First release.
02-May-2011	2	R_G value has been updated.
06-Dec-2011	3	Removed p/n STD6N62K3 in DPAK.
03-Aug-2012	4	Added package, mechanical data: I^2PAKFP Updated *Table 1: Device summary*, *Table 2: Absolute maximum ratings*, *Table 3: Thermal data*, *Table 4: On /off states*, *Table 13: IPAK (TO-251) mechanical data* and *Figure 29: IPAK (TO-251) drawing* Minor text changes.

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