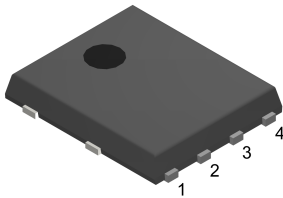
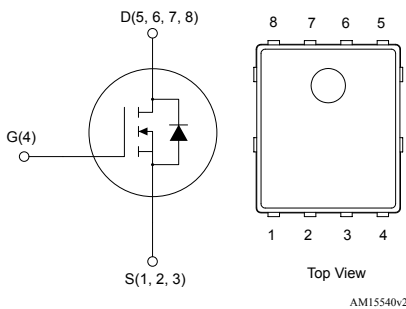


N-channel 80 V, 3.0 mΩ typ., 120 A STripFET F7 Power MOSFET in a PowerFLAT 5x6 package


PowerFLAT 5x6


Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL130N8F7	80 V	3.6 mΩ	120 A	135 W

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rSS}/C_{iSS} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.



Product status link

[STL130N8F7](#)

Product summary

Order code	STL130N8F7
Marking	130N8F7
Package	PowerFLAT 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	±20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	120	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	93	
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ °C}$	26	A
	Drain current (continuous) at $T_{pcb} = 100\text{ °C}$	19	
$I_{DM}^{(1)(3)}$	Drain current (pulsed)	480	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	104	A
$P_{TOT}^{(1)}$	Total power dissipation at $T_C = 25\text{ °C}$	135	W
$P_{TOT}^{(2)}$	Total power dissipation at $T_{pcb} = 25\text{ °C}$	4.8	W
$E_{AS}^{(4)}$	Single pulse avalanche energy	515	mJ
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operating junction temperature range		

1. This value is rated according to $R_{thj-case}$ and is limited by package.
2. This value is rated according to $R_{thj-pcb}$.
3. Pulse width is limited by safe operating area.
4. Starting $T_J = 25\text{ °C}$, $I_D = 18.5\text{ A}$, $V_{DD} = 50\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.1	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	°C/W

1. When mounted on FR-4 board of 1 inch², 2oz Cu, $t < 10\text{ s}$.

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 3. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}, T_J = 125\text{ °C}^{(1)}$			10	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 13\text{ A}$		3.0	3.6	m Ω

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$	-	6340	-	pF
C_{oss}	Output capacitance		-	1195	-	pF
C_{rss}	Reverse transfer capacitance		-	105	-	pF
Q_g	Total gate charge	$V_{DD} = 40\text{ V}, I_D = 26\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	96	-	nC
Q_{gs}	Gate-source charge		-	29	-	nC
Q_{gd}	Gate-drain charge		-	26	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 40\text{ V}, I_D = 13\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	26	-	ns
t_r	Rise time		-	51	-	ns
$t_{d(off)}$	Turn-off delay time		-	82	-	ns
t_f	Fall time		-	44	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 26\text{ A}, V_{GS} = 0\text{ V}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 26\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD} = 60\text{ V}, T_J = 150\text{ °C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	58		ns
Q_{rr}	Reverse recovery charge		-	92		nC
I_{RRM}	Reverse recovery current		-	3.2		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

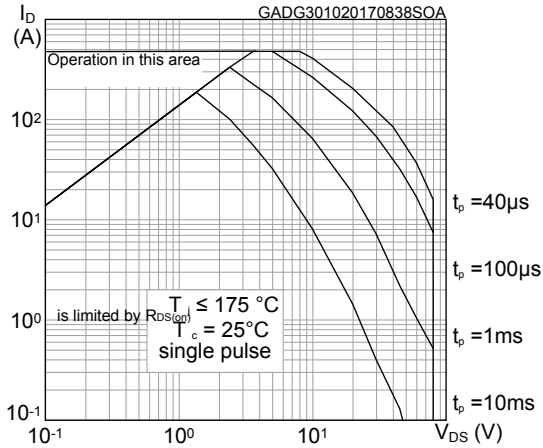


Figure 2. Normalized thermal impedance

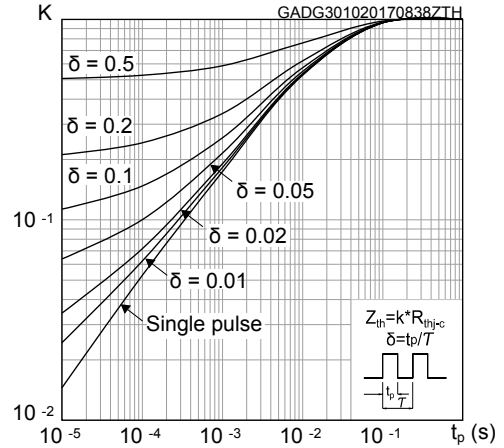


Figure 3. Output characteristics

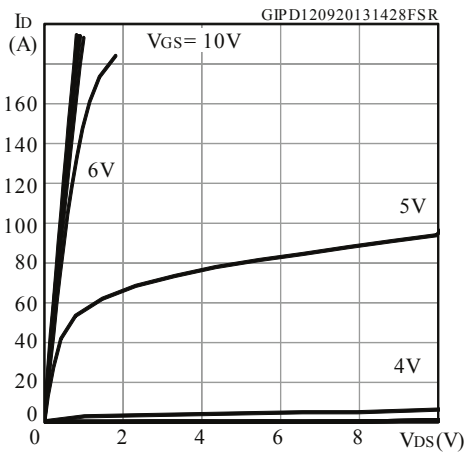


Figure 4. Transfer characteristics

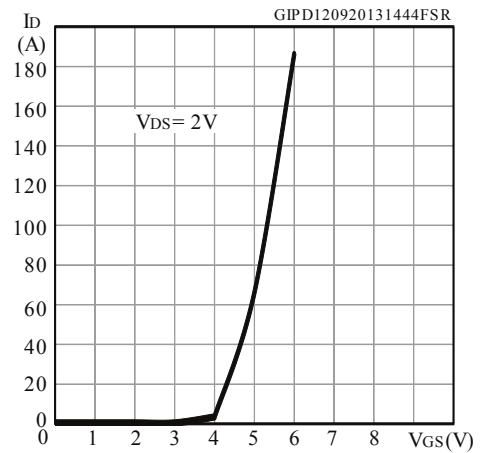


Figure 5. Gate charge vs gate-source voltage

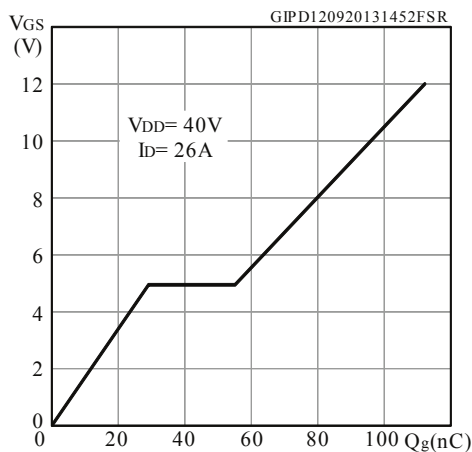


Figure 6. Static drain-source on-resistance

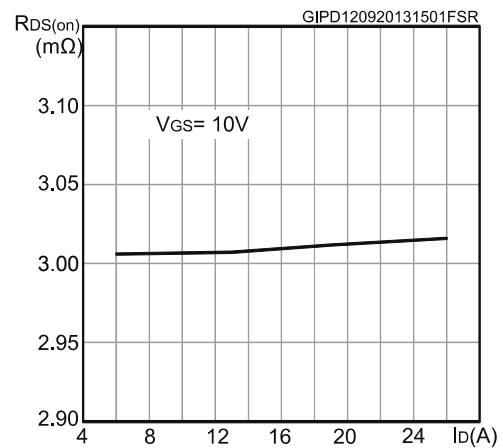


Figure 7. Capacitance variations

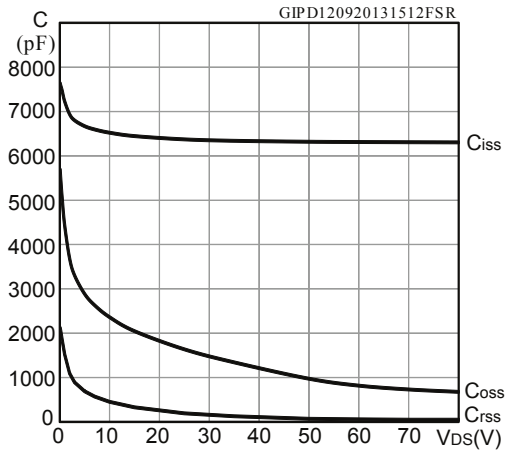


Figure 8. Normalized V_{(BR)DSS} vs temperature

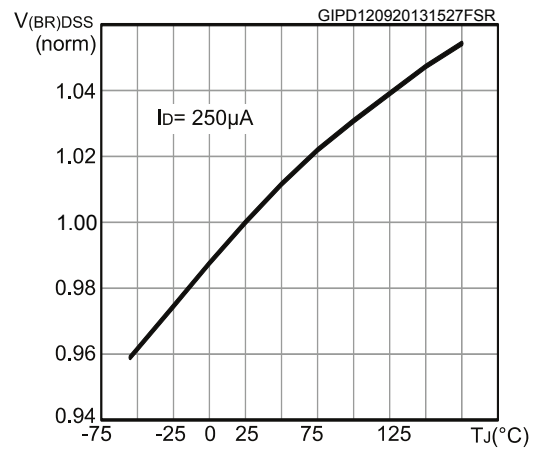


Figure 9. Normalized gate threshold voltage vs temperature

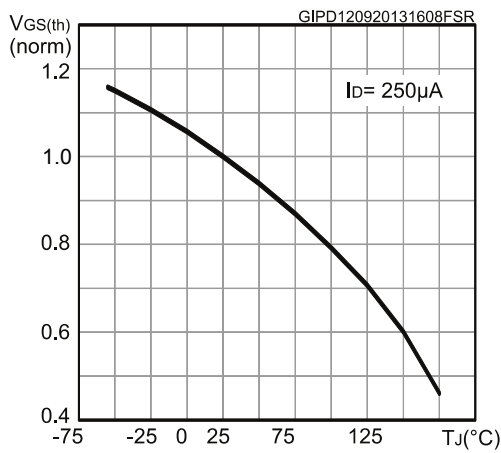


Figure 10. Normalized on-resistance vs temperature

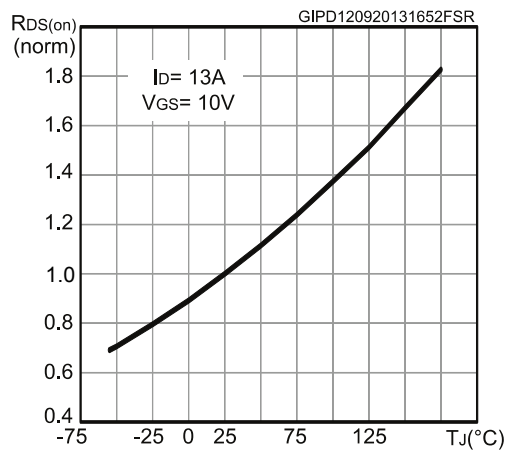
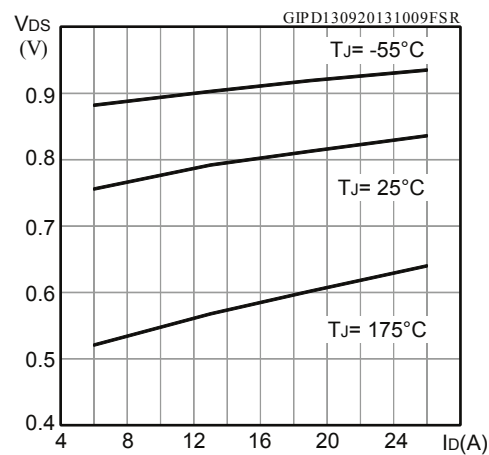
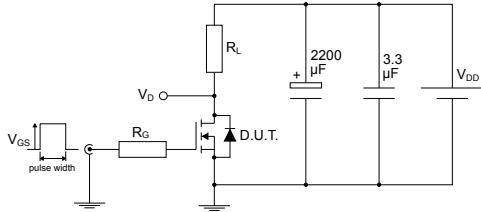


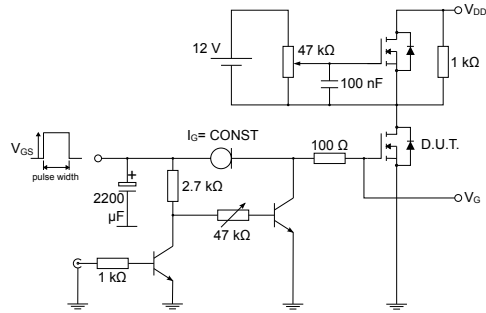
Figure 11. Source-drain diode forward characteristics



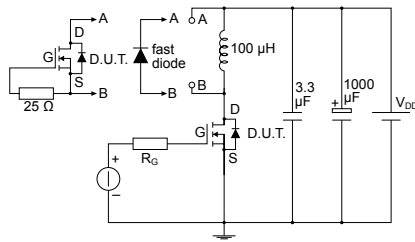
3 Test circuits

Figure 12. Test circuit for resistive load switching times


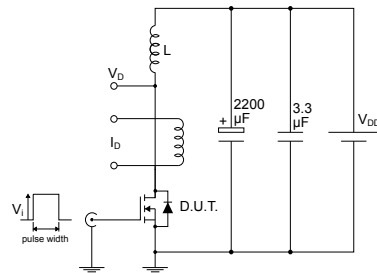
AM01468v1

Figure 13. Test circuit for gate charge behavior


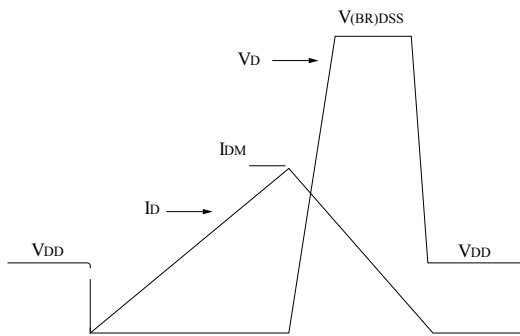
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Figure 14. Test circuit for inductive load switching and diode recovery times


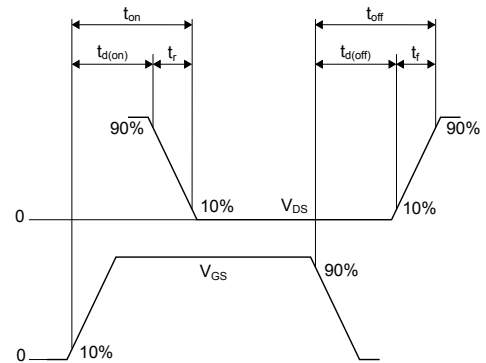
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Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


AM01472v1

Figure 17. Switching time waveform


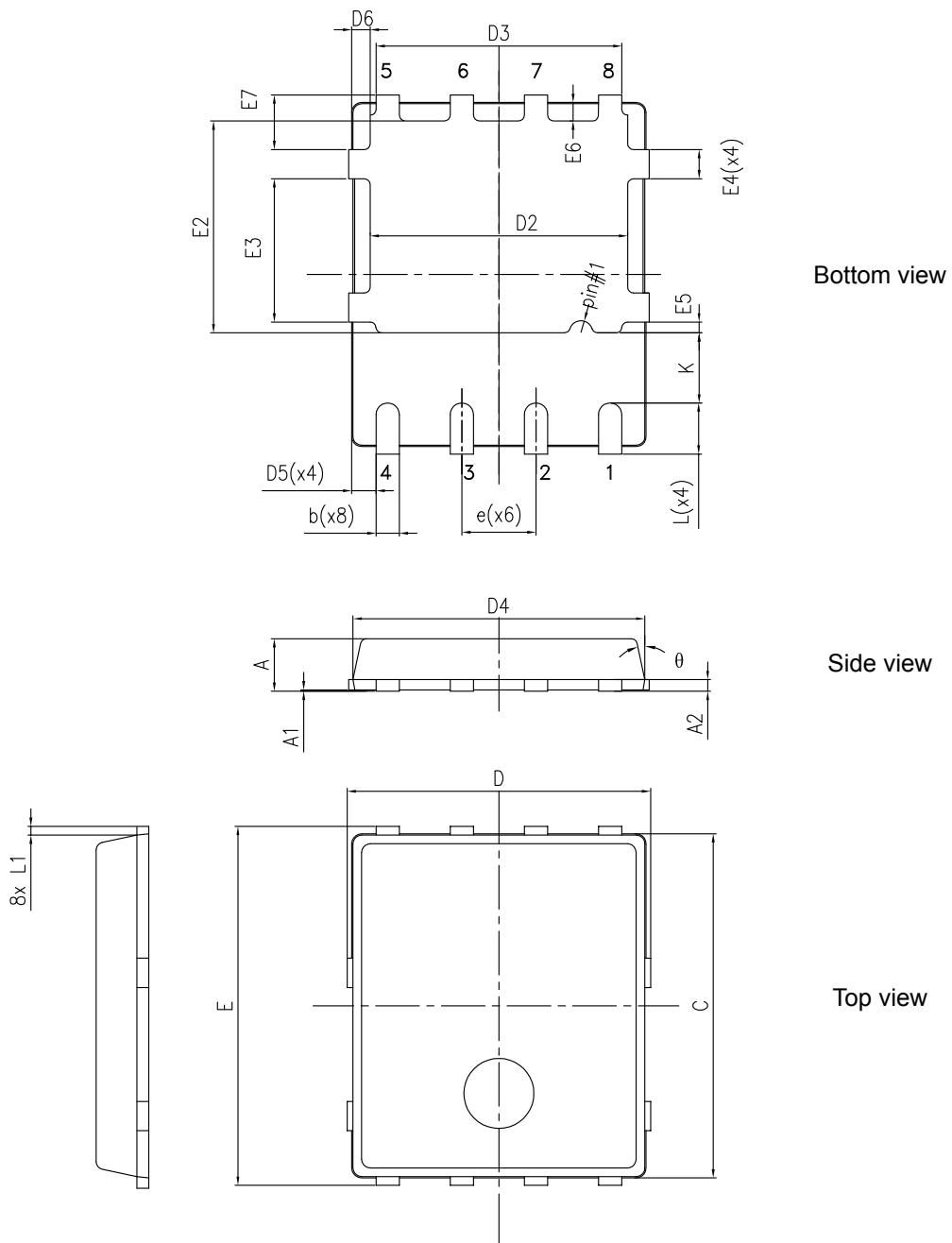
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 type C package information

Figure 18. PowerFLAT 5x6 type C package outline



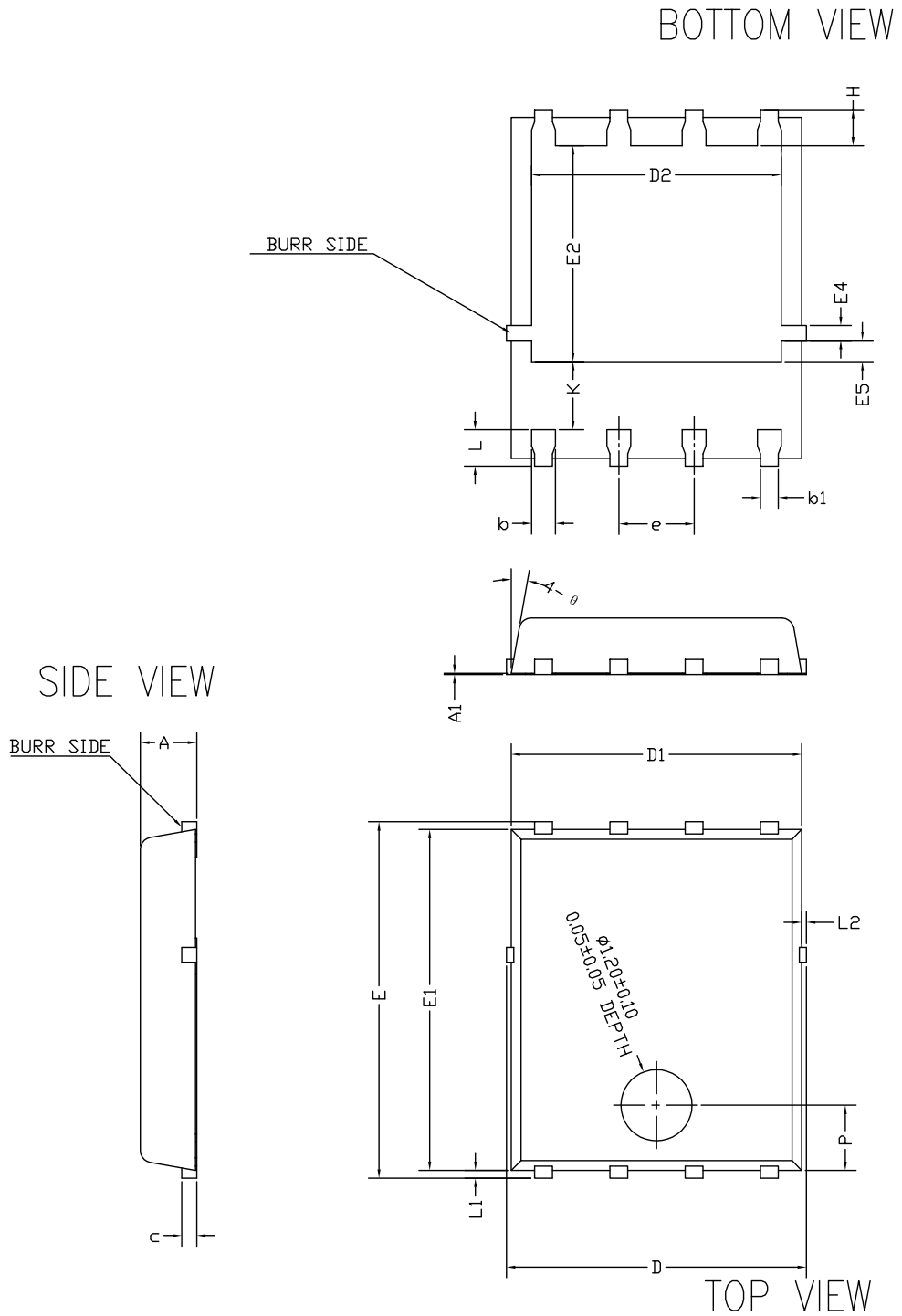
8231817_typeC_Rev20

Table 7. PowerFLAT 5x6 type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.725		1.025
L1	0.05	0.15	0.25
θ	0°		12°

4.2 PowerFLAT 5x6 type C SUBCON package information

Figure 19. PowerFLAT 5x6 type C SUBCON package outline

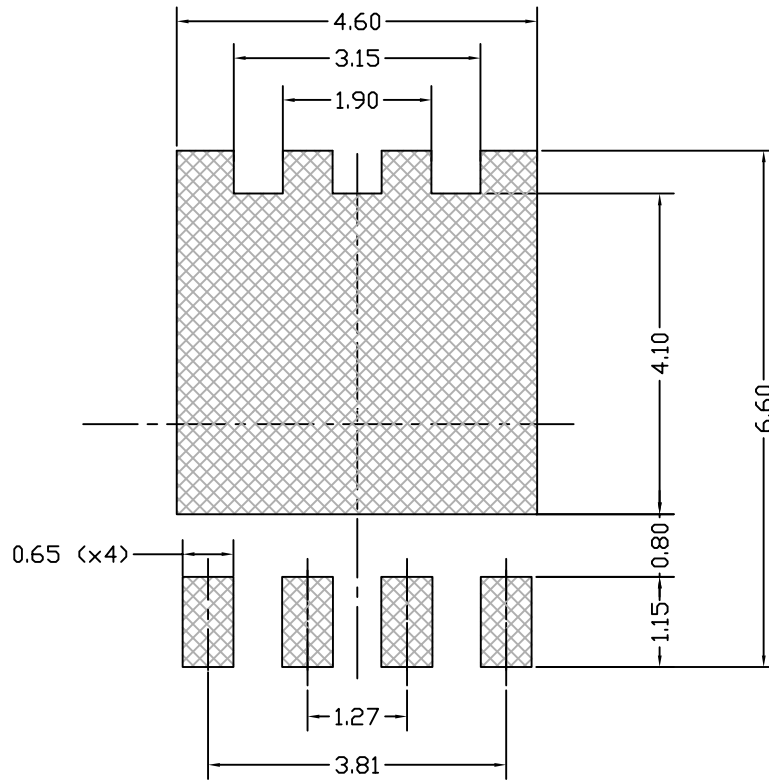


8472137_SUBCON_998G_REV4

Table 8. PowerFLAT 5x6 type C SUBCON package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1		0.02	
b	0.35	0.40	0.45
b1		0.30	
c	0.21	0.25	0.34
D			5.10
D1	4.80	4.90	5.00
D2	4.01	4.21	4.31
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.54	3.64	3.74
E4	0.15	0.25	0.35
E5	0.26	0.36	0.46
H	0.51	0.61	0.71
K	0.95		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
θ	8°	10°	12°

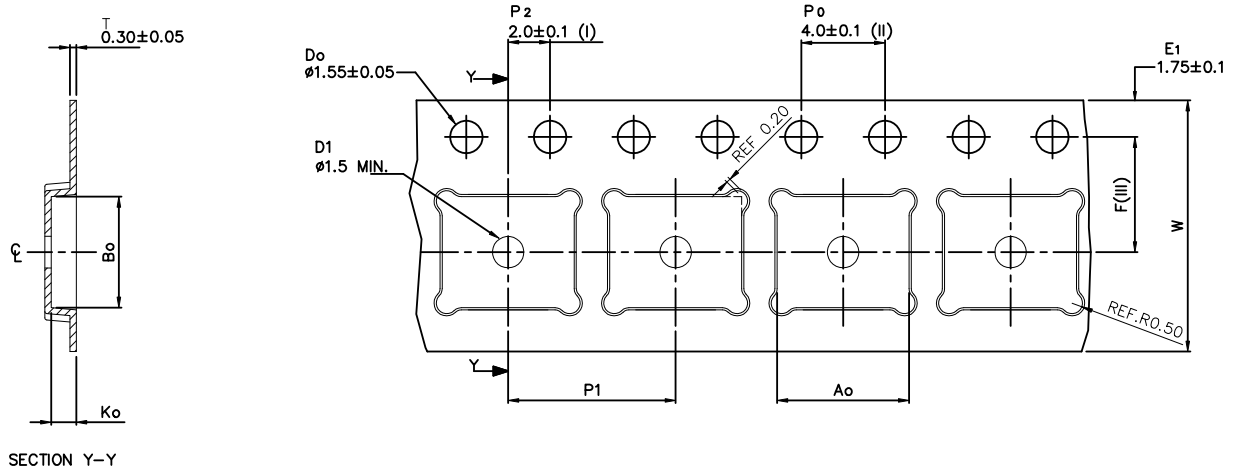
Figure 20. PowerFLAT 5x6 recommended footprint (dimensions are in mm)



8231817_FOOTPRINT_simp_Rev_20

4.3 PowerFLAT 5x6 packing information

Figure 21. PowerFLAT 5x6 tape (dimensions are in mm)



A ₀	6.30 +/- 0.1
B ₀	5.30 +/- 0.1
K ₀	1.20 +/- 0.1
F	5.50 +/- 0.1
P ₁	8.00 +/- 0.1
W	12.00 +/- 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 22. PowerFLAT 5x6 package orientation in carrier tape

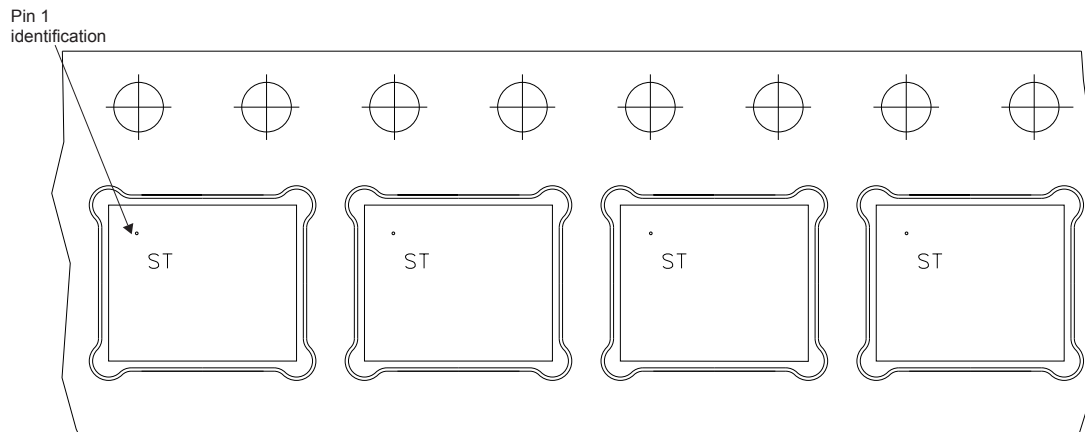
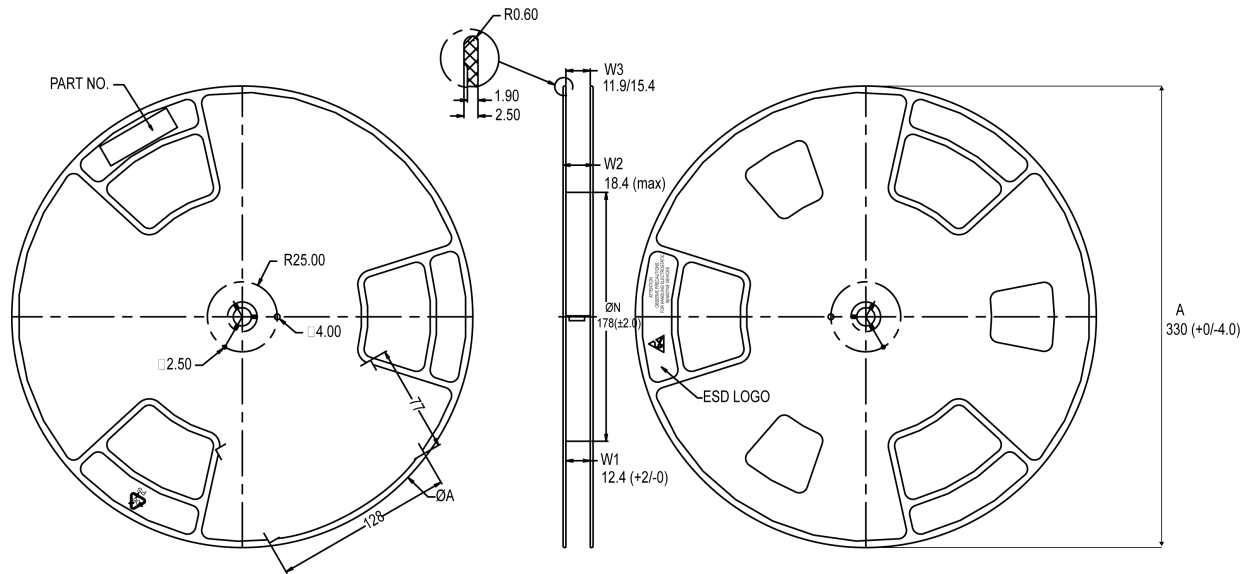


Figure 23. PowerFLAT 5x6 reel



All dimensions are in millimeters

8234350_Reel_rev_C

Revision history

Table 9. Document revision history

Date	Revision	Changes
21-May-2013	1	First release
23-Sep-2013	2	Document status promoted from preliminary to production data. Inserted <i>Section 2.1: Electrical characteristics (curves)</i> .
25-Jul-2014	3	Modified: title and description Modified: ID and PTOT values in cover page Updated: <i>Figure 13, 14, 15 and 16</i> Updated: <i>Section 4: Package mechanical data</i> Minor text changes
03-Nov-2017	4	Updated title and features table on cover page. Updated <i>Table 2: "Absolute maximum ratings"</i> and <i>Table 7: "Source-drain diode"</i> . Updated <i>Figure 2: "Safe operating area"</i> and <i>Figure 3: "Normalized thermal impedance"</i> . Updated <i>Section 4.1: "PowerFLAT™ 5x6 type C package information"</i> . Minor text changes
26-Feb-2020	5	Updated Section 4 Package information . Minor text changes.

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