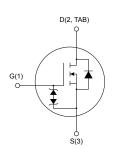


N-channel 800 V, 1.50 Ω typ., 4 A MDmesh K5 Power MOSFET in a DPAK package

Features





Order code	V _{DS}	R _{DS(on)} max.	I _D
STD5N80K5	800 V	1.75 Ω	4 A

- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- · Ultra-low gate charge
- 100% avalanche tested
- · Zener-protected

Applications

· Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.



Product status link STD5N80K5

Product summary			
Order code	STD5N80K5		
Marking	5N80K5		
Package	DPAK		
Packing	Tape and reel		



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	±30	V
I _D	Drain current (continuous) at T _C = 25 °C	4	Α
I _D	Drain current (continuous) at T _C = 100 °C	2.3	А
I _{DM} ⁽¹⁾	Drain current (pulsed)	16	А
P _{TOT}	Total power dissipation at T _C = 25 °C	60	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/IIS
T _J	Operating junction temperature range	- 55 to 150	°C
T _{stg}	Storage temperature range	- 55 (0 150	

- 1. Pulse width limited by safe operating area.
- 2. $I_{SD} \le 4$ A, di/dt = 100 A/ μ s; V_{DS} (peak) $< V_{(BR)DSS}$, $V_{DD} = 640$ V.
- 3. $V_{DS} \le 640 \text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	2.08	°C/W
R _{thj-pcb} (1)	Thermal resistance junction-pcb	50	°C/W

1. When mounted on FR-4 board of 1 inch², 2 oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _J max)	1.2	Α
E _{AS}	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	165	mJ

DS11344 - Rev 4 page 2/18

2 Electrical characteristics

 T_C = 25 °C unless otherwise specified

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	800			V
I	I _{DSS} Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 800 V			1	
IDSS		V _{GS} = 0 V, V _{DS} = 800 V, T _C = 125 °C ⁽¹⁾			50	μΑ
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	$V_{DD} = V_{GS}$, $I_D = 100 \mu A$	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 2 A		1.50	1.75	Ω

^{1.} Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	177	-	pF
Coss	Output capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	15	-	pF
C _{rss}	Reverse transfer capacitance		-	0.3	-	pF
C _{o(tr)} (1)	Equivalent capacitance time related	V _{DS} = 0 to 640 V, V _{GS} = 0 V	-	33	-	nC
C _{o(er)} (2)	Equivalent capacitance energy related		-	12	-	nC
R _g	Intrinsic gate resistance	V _{DD} = 640 V, I _D = 4 A,	-	16	-	nC
Qg	Total gate charge	V _{GS} = 0 to 10 V (see Figure 14. Test circuit for gate	-	5	-	nC
Q _{gs}	Gate-source charge		-	1.7	-	nC
Q _{gd}	Gate-drain charge	charge behavior)	-	2.9	-	nC

^{1.} $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 400 V, I _D = 2 A,	-	12.7	-	ns
t _r	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$	-	11.7	-	ns
t _{d(off)}	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and	-	23	-	ns
t _f	Fall time	Figure 18. Switching time waveform)	-	14.8	-	ns

DS11344 - Rev 4 page 3/18

^{2.} $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .



Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		4	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		16	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 4 A, V _{GS} = 0 V	-		1.5	V
t _{rr}	Reverse recovery time	I _{SD} = 4 A, di/dt = 100 A/μs, V _{DD} = 60 V (see Figure 15. Test circuit for inductive	-	265		ns
Q _{rr}	Reverse recovery charge		-	1.59		μC
I _{RRM}	Reverse recovery current	load switching and diode recovery times)	-	12		Α
t _{rr}	Reverse recovery time	I_{SD} = 4 A, di/dt = 100 A/ μ s, V_{DD} = 60 V,	-	386		ns
Q _{rr}	Reverse recovery charge	T _J = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	2.18		μC
I _{RRM}	Reverse recovery current		-	11.3		Α

- 1. Pulse width limited by safe operating area.
- 2. Pulsed: pulse duration = 300 μs, duty cycle 1.5%.

Table 8. Gate-source Zener diode

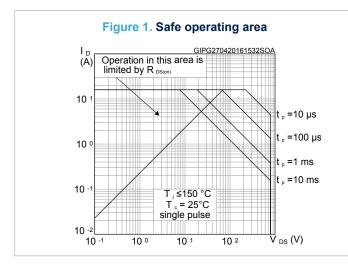
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)GSO}	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}, I_D = 0 \text{ A}$	30	-	-	V

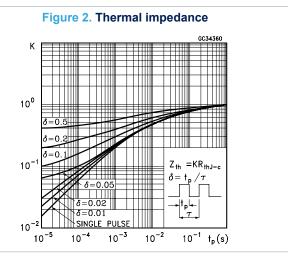
The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

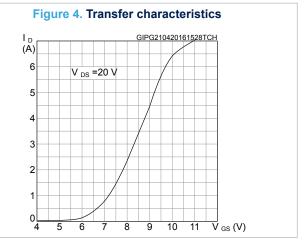
DS11344 - Rev 4 page 4/18

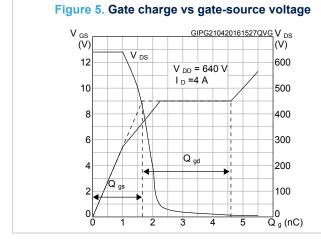


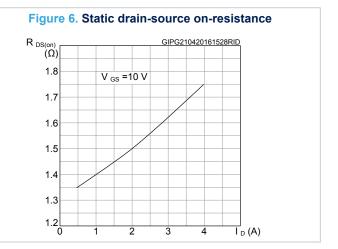
2.1 Electrical characteristics (curves)











DS11344 - Rev 4 page 5/18



Figure 7. Capacitance variations C (pF) GIPG210420161526CVR 10 C _{ISS} 10 2 10 C oss C_{RSS} f = 1 MHz 10 0 10 -1 Ŭ _{DS} (V) 10 -1 10 ¹ 10 º

Figure 8. Normalized gate threshold voltage vs temperature V _{GS(th)} (norm.) GIPG210420161529VTH 1.2 $I_D = 100 \mu A$ 1.0 8.0 0.6 0.4 0.2 -75 -25 25 75 125 T_j (°C)

Figure 9. Normalized on-resistance vs temperature

R DS(on) (norm.)

2.6

V GS = 10 V

1.8

1.4

1.0

0.6

0.2

-75

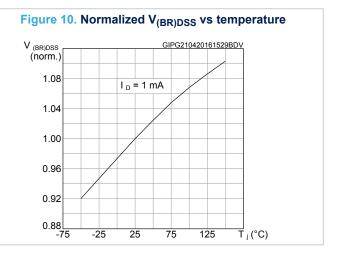
-25

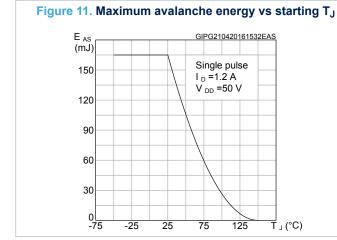
25

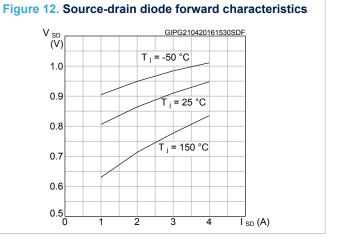
75

125

T j (°C)







DS11344 - Rev 4 page 6/18



3 Test circuits

Figure 13. Test circuit for resistive load switching times

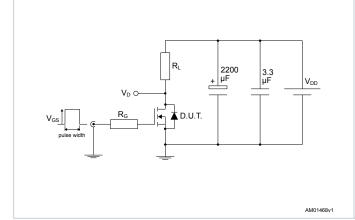


Figure 14. Test circuit for gate charge behavior

VGS

PURCHARACTER

VGS

PURCHARACTER

AMD1469r10

Figure 15. Test circuit for inductive load switching and diode recovery times

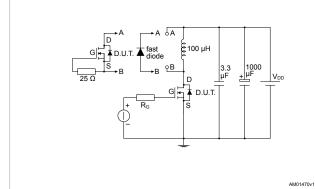


Figure 16. Unclamped inductive load test circuit

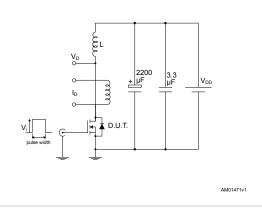


Figure 17. Unclamped inductive waveform

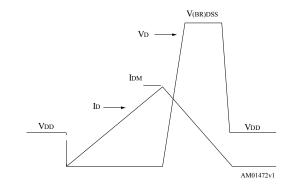
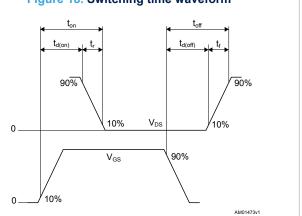


Figure 18. Switching time waveform



DS11344 - Rev 4 page 7/18



4 Package information

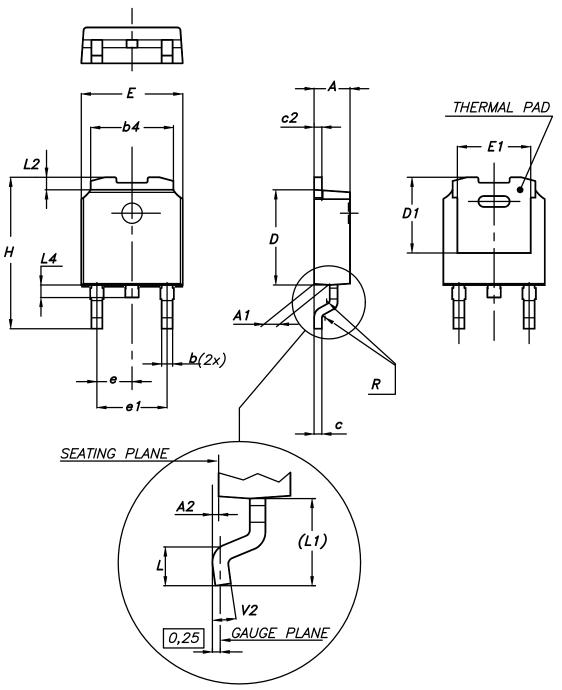
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

DS11344 - Rev 4 page 8/18



4.1 DPAK (TO-252) type A package information

Figure 19. DPAK (TO-252) type A package outline



0068772_A_26



Table 9. DPAK (TO-252) type A mechanical data

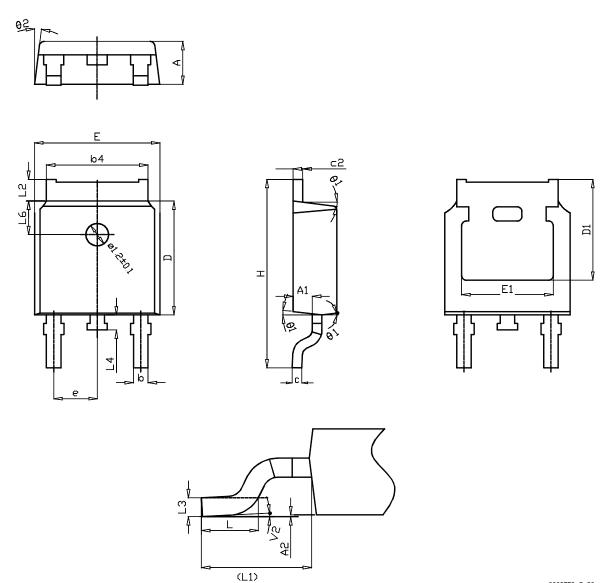
mm					
Min.	Тур.	Max.			
2.20		2.40			
0.90		1.10			
0.03		0.23			
0.64		0.90			
5.20		5.40			
0.45		0.60			
0.48		0.60			
6.00		6.20			
4.95	5.10	5.25			
6.40		6.60			
4.60	4.70	4.80			
2.159	2.286	2.413			
4.445	4.572	4.699			
9.35		10.10			
1.00		1.50			
2.60	2.80	3.00			
0.65	0.80	0.95			
0.60		1.00			
	0.20				
0°		8°			
	2.20 0.90 0.03 0.64 5.20 0.45 0.48 6.00 4.95 6.40 4.60 2.159 4.445 9.35 1.00 2.60 0.65 0.60	Min. Typ. 2.20 0.90 0.03 0.64 5.20 0.45 0.48 6.00 4.95 5.10 6.40 4.70 2.159 2.286 4.445 4.572 9.35 1.00 2.60 2.80 0.65 0.80 0.60 0.20			

DS11344 - Rev 4 page 10/18



4.2 DPAK (TO-252) type C package information

Figure 20. DPAK (TO-252) type C package outline



0068772_C_26



Table 10. DPAK (TO-252) type C mechanical data

Dim.	mm				
Dilli.	Min.	Тур.	Max.		
А	2.20	2.30	2.38		
A1	0.90	1.01	1.10		
A2	0.00		0.10		
b	0.72		0.85		
b4	5.13	5.33	5.46		
С	0.47		0.60		
c2	0.47		0.60		
D	6.00	6.10	6.20		
D1	5.25				
E	6.50	6.60	6.70		
E1	4.70				
е	2.186	2.286	2.386		
Н	9.80	10.10	10.40		
L	1.40	1.50	1.70		
L1		2.90 REF			
L2	0.90		1.25		
L3		0.51 BSC			
L4	0.60	0.80	1.00		
L6	1.80 BSC				
θ1	5°	7°	9°		
θ2	5°	7°	9°		
V2	0°		8°		

DS11344 - Rev 4 page 12/18



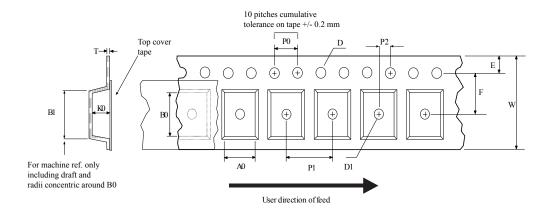
Figure 21. DPAK (TO-252) recommended footprint (dimensions are in mm)

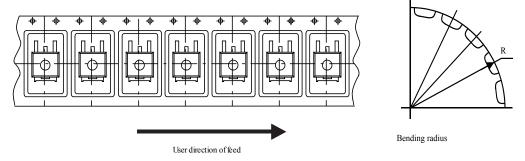
FP_0068772_26



4.3 DPAK (TO-252) packing information

Figure 22. DPAK (TO-252) tape outline



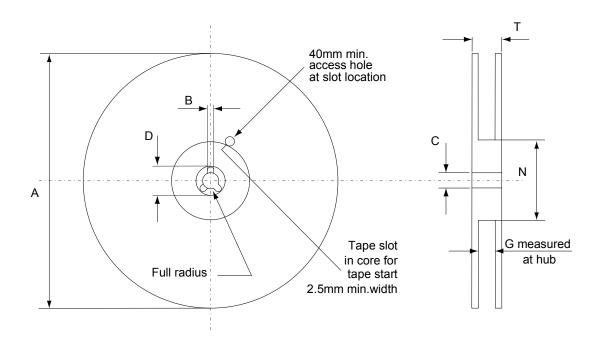


AM08852v1

DS11344 - Rev 4 page 14/18



Figure 23. DPAK (TO-252) reel outline



AM06038v1

Table 11. DPAK (TO-252) tape and reel mechanical data

Таре			Reel		
Dim.	mm		Disc	mm	
Dilli.	Min.	Max.	Dim.	Min.	Max.
A0	6.8	7	А		330
В0	10.4	10.6	В	1.5	
B1		12.1	С	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	Т		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
Т	0.25	0.35			
W	15.7	16.3			

DS11344 - Rev 4 page 15/18



Revision history

Table 12. Document revision history

Date	Revision	Changes
08-Jan-2016	1	First release.
09-May-2016	2	Modified: title
		Modified: Table 1. Absolute maximum ratings, Table 2. Thermal data, Table 4. On/off-state, Table 5. Dynamic, Table 6. Switching times and Table 7. Source-drain diode.
		Added: Section 2.1 Electrical characteristics (curves).
		Modified: Section 3 Test circuits.
		Minor text changes
03-Apr-2019	3	Updated Section 4 Package information.
		Minor text changes.
05-Jul-2019	4	Updated Section 4 Package information.
		Minor text changes.



Contents

1	Elec	trical ratings	2		
2	Electrical characteristics				
		Electrical characteristics (curves)			
3		circuits			
4 Package information					
	4.1	DPAK (TO-252) type A package information	8		
	4.2	DPAK (TO-252) type C package information	10		
	4.3	DPAK (TO-252) packing information	13		
Rev	ision	history	16		



IMPORTANT NOTICE - PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics - All rights reserved

DS11344 - Rev 4 page 18/18