

High voltage fast-switching NPN power transistor

Features

- STK13003 is reverse pin out versus standard SOT-82 package
- High voltage capability
- Low spread of dynamic parameters
- Minimum lot-to-lot spread for reliable operation
- Very high switching speed

Applications

- Electronic ballast for fluorescent lighting (CFL)
- SMPS for battery charger

Description

The device is manufactured using high voltage multi-epitaxial planar technology for high switching speeds and high voltage capability.

It uses a cellular emitter structure with planar edge termination to enhance switching speeds while maintaining the wide RBSOA.

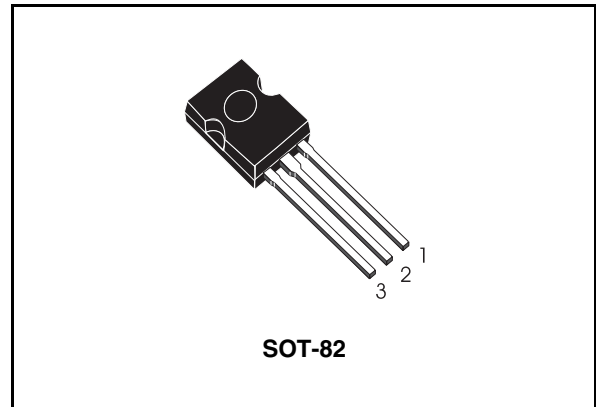


Figure 1. Internal schematic diagram

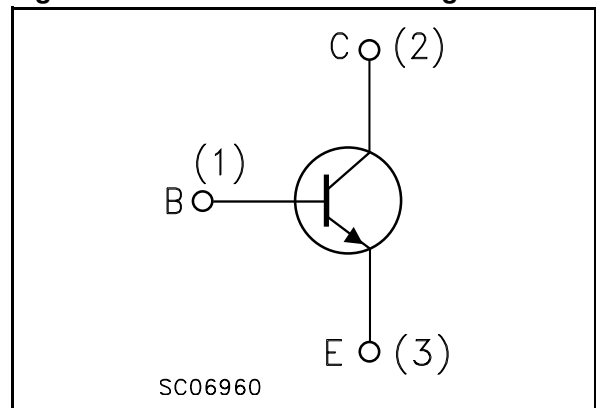


Table 1. Device summary

| Order code | Marking | Package | Packaging |
|------------|---------|---------|-----------|
| STK13003 | K13003 | SOT-82 | Tube |

1 Electrical ratings

Table 2. Absolute maximum rating

| Symbol | Parameter | Value | Unit |
|-----------|--|---------------|------------|
| V_{CES} | Collector-emitter voltage ($V_{BE} = 0$) | 700 | V |
| V_{CEO} | Collector-emitter voltage ($I_B = 0$) | 400 | V |
| V_{EBO} | Emitter-base voltage ($I_C = 0$, $I_B = 0.75A$, $t_p < 10\mu s$) | $V_{(BR)EBO}$ | V |
| I_C | Collector current | 1.5 | A |
| I_{CM} | Collector peak current ($t_p < 5ms$) | 3 | A |
| I_B | Base current | 0.75 | A |
| I_{BM} | Base peak current ($t_p < 5ms$) | 1.5 | A |
| P_{tot} | Total dissipation at $T_c = 25^\circ C$ | 40 | W |
| T_{stg} | Storage temperature | -55 to 150 | $^\circ C$ |
| T_J | Max. operating junction temperature | 150 | $^\circ C$ |

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 3. Electrical characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--|--|--|--------|------|-----------------|---|
| I_{CES} | Collector cut-off current ($V_{\text{BE}} = 0$) | $V_{\text{CE}} = 700\text{V}$ $V_{\text{CE}} = 700\text{V}$ $T_{\text{c}} = 125\text{°C}$ | | | 1 5 | mA mA |
| $V_{(\text{BR})\text{EBO}}$ | Emitter-Base breakdown voltage ($I_{\text{C}} = 0$) | $I_{\text{E}} = 10\text{mA}$ | 9 | | 18 | V |
| $V_{\text{CEO(sus)}}^{(1)}$ | Collector-emitter sustaining voltage ($I_{\text{B}} = 0$) | $I_{\text{C}} = 10\text{mA}$ | 400 | | | V |
| $V_{\text{CE(sat)}}^{(1)}$ | Collector-emitter saturation voltage | $I_{\text{C}} = 0.5\text{A}$ $I_{\text{B}} = 0.1\text{A}$ $I_{\text{C}} = 1\text{A}$ $I_{\text{B}} = 0.25\text{A}$ $I_{\text{C}} = 1.5\text{A}$ $I_{\text{B}} = 0.5\text{A}$ | | | 0.5 1 1.5 | V V V |
| $V_{\text{BE(sat)}}^{(1)}$ | Base-emitter saturation voltage | $I_{\text{C}} = 0.5\text{A}$ $I_{\text{B}} = 0.1\text{A}$ $I_{\text{C}} = 1\text{A}$ $I_{\text{B}} = 0.25\text{A}$ | | | 1 1.2 | V V |
| h_{FE} | DC current gain | $I_{\text{C}} = 0.5\text{A}$ $V_{\text{CE}} = 2\text{V}$ $I_{\text{C}} = 1\text{A}$ $V_{\text{CE}} = 2\text{V}$ | 8 5 | | 20 25 | |
| t_{r} t_{s} t_{f} | Resistive load Rise time Storage time Fall time | $V_{\text{CC}} = 125\text{V}$ $I_{\text{C}} = 1\text{A}$ $I_{\text{B1}} = 0.2\text{A}$ $I_{\text{B2}} = -0.2\text{A}$ $T_{\text{p}} = 25\mu\text{s}$ | | | 1 4 0.7 | μs μs μs |
| t_{s} | Inductive load Storage time | $I_{\text{C}} = 1\text{A}$ $I_{\text{B1}} = 0.2\text{A}$ $V_{\text{BE}} = -5\text{V}$ $L = 50\text{mH}$ $V_{\text{Clamp}} = 300\text{V}$ | | 0.8 | | μs |

1. Pulsed duration = 300 μs , duty cycle $\leq 1.5\%$.

2.1 Electrical characteristics (curves)

2.2

Figure 2. Safe operating areas

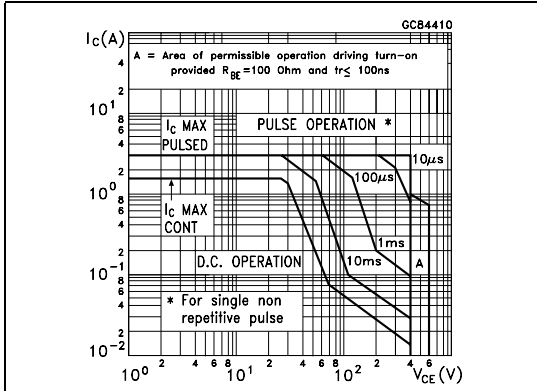


Figure 3. Derating curves

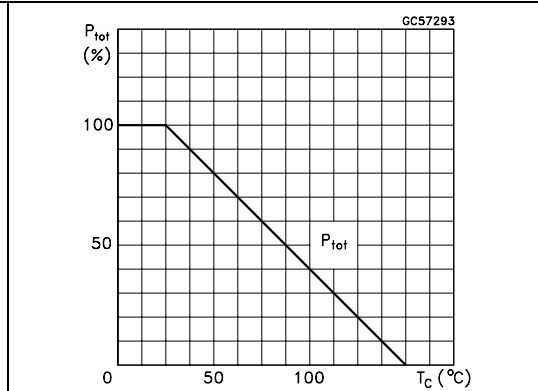


Figure 4. Output characteristics

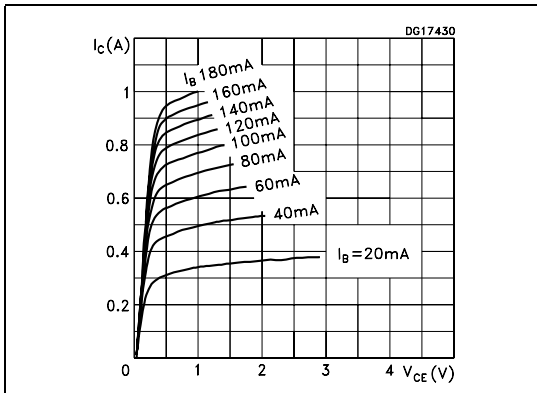


Figure 5. Reverse biased safe operating areas

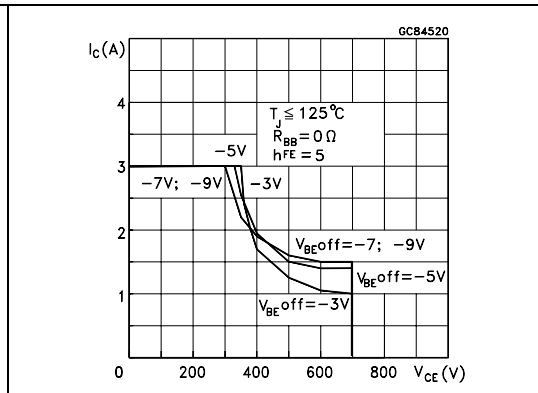


Figure 6. DC current gain

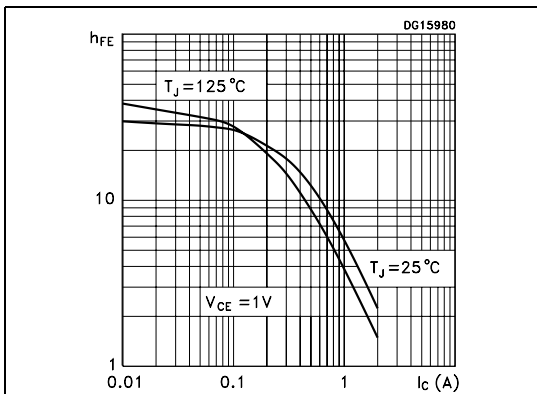


Figure 7. DC current gain

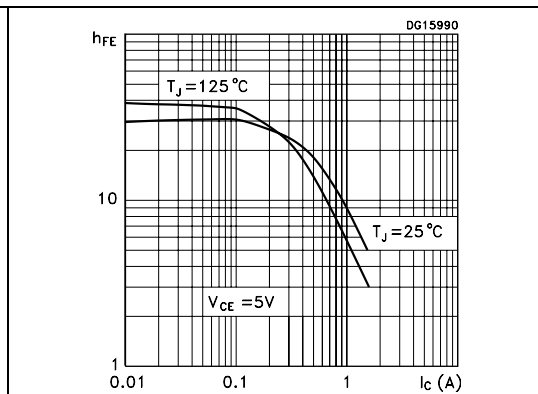


Figure 8. Collector-emitter saturation voltage

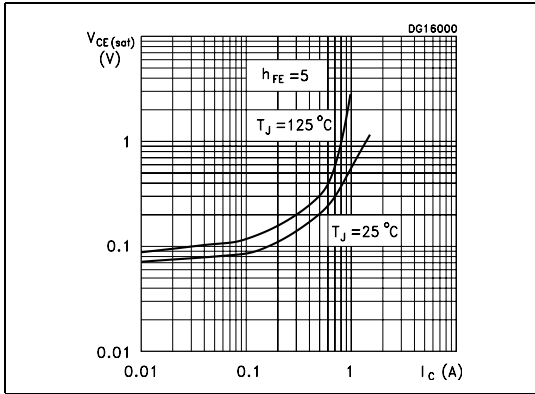


Figure 9. Base-emitter saturation voltage

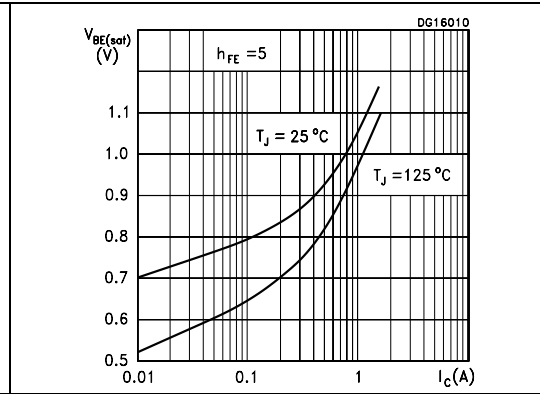
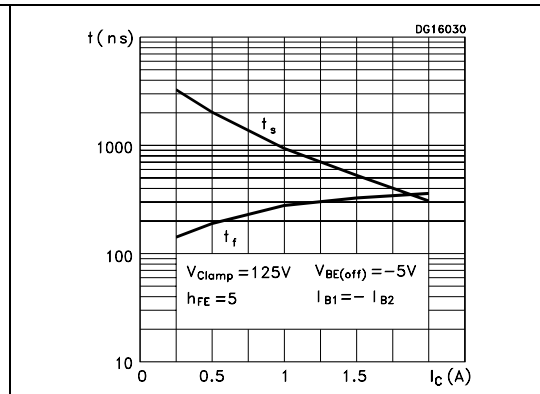
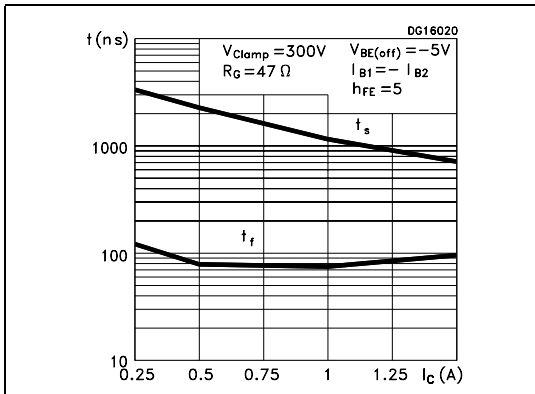


Figure 10. Inductive load switching time **Figure 11. Resistive load switching time**



2.3 Test circuits

Resistive load switching test circuit

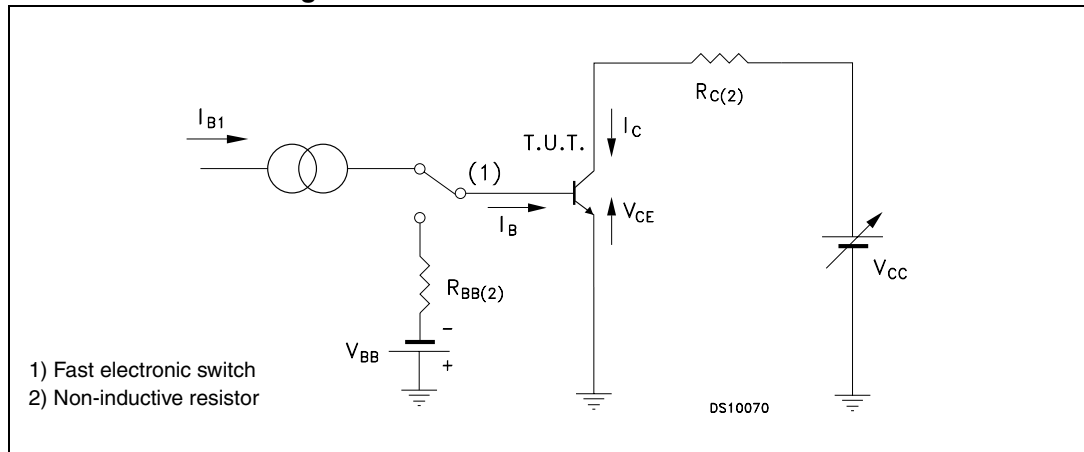
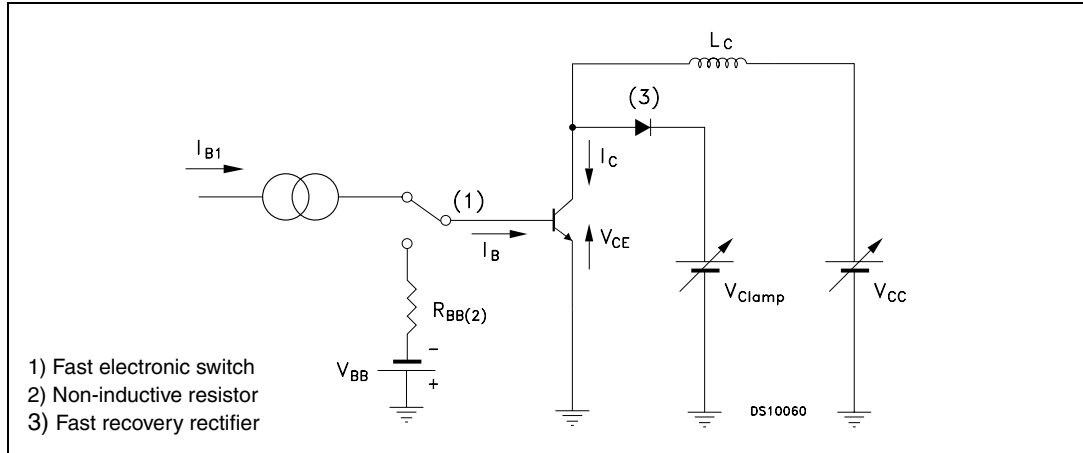


Figure 12. Inductive load switching test circuit

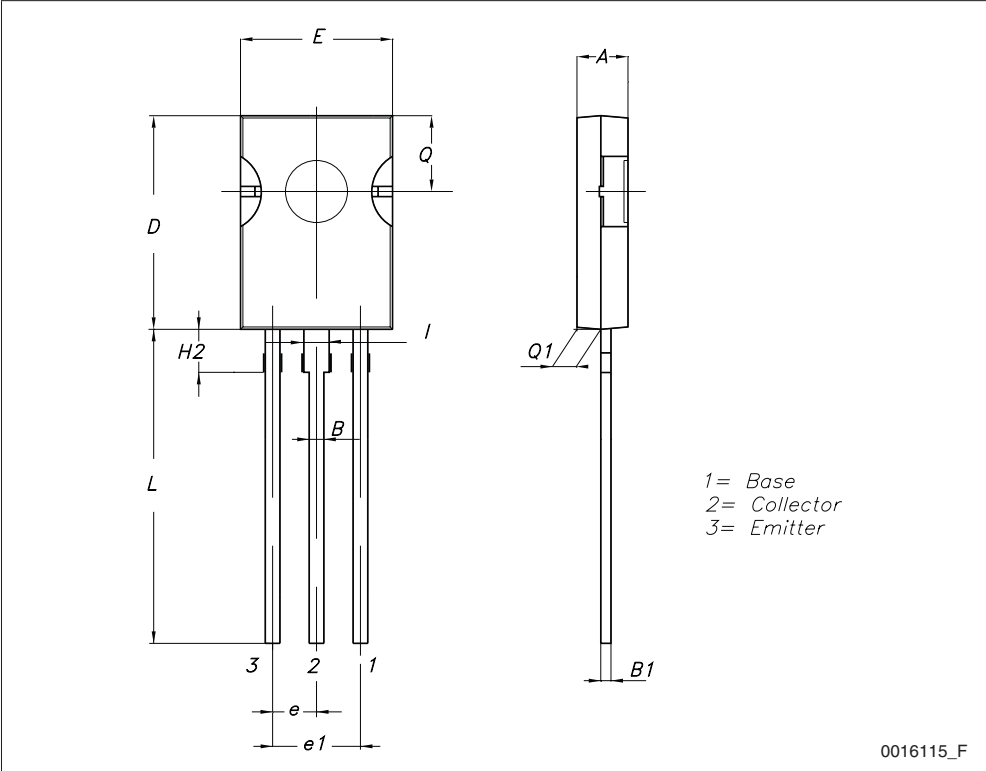


3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SOT-82 mechanical data

| Dim. | mm. | | |
|------|-------|------|-------|
| | Min. | Typ. | Max. |
| A | 2.40 | | 2.70 |
| B | 0.70 | | 0.90 |
| B1 | 0.49 | | 0.75 |
| D | 10.50 | | 10.80 |
| E | 7.40 | | 7.80 |
| e | 2.04 | | 2.54 |
| e1 | 4.07 | | 5.08 |
| L | 15.40 | | 16 |
| Q | | 3.80 | |
| Q1 | 1 | | 1.30 |
| H2 | | 2.07 | |
| I | | 1.27 | |



4 Revision history

Table 4. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 21-Jun-2004 | 3 | |
| 14-Jul-2008 | 4 | Modified mechanical data <i>Figure on page 8.</i> |

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