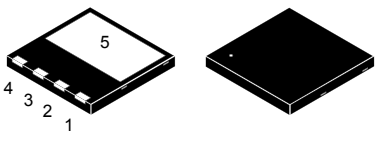
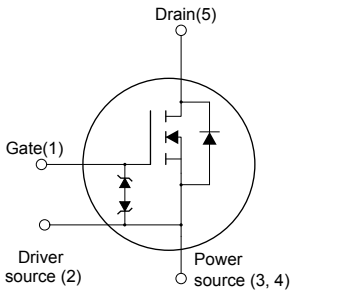
N-channel 600 V, 0.184 Ω typ., 16 A MDmesh™ M2 EP Power MOSFET in a PowerFLAT™ 8x8 HV package



PowerFLAT™ 8x8 HV



NG1DS2PS34D5Z

Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D
STL25N60M2-EP	650 V	0.205 Ω	16 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- Tailored for Very High Frequency Converters (f > 150 kHz)

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 EP enhanced performance technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

Product status
STL25N60M2-EP

Device summary	
Order code	STL25N60M2-EP
Marking	25N60M2EP
Package	PowerFLAT™ 8x8 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	16	A
I_D	Drain current (continuous) at T_C = 100 °C	10	A
I_{DM} (1)	Drain current (pulsed)	64	A
P_{TOT}	Total dissipation at T_C = 25 °C	125	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 16 A, di/dt ≤ 400 A/µs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V.*
3. *V_{DS} ≤ 480 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	45	°C/W

1. *When mounted on FR-4 board of inch², 2oz Cu.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive (pulse width limited by T_{jmax})	3.5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}; V_{DD} = 50 V)	180	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 8 A		0.184	0.205	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	1090	-	pF
C_{oss}	Output capacitance		-	56	-	pF
C_{rss}	Reverse transfer capacitance		-	1.6	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	255	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 18 A, V_{GS} = 0 to 10 V (see Figure 15. Gate charge test circuit)	-	29	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	12	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}*

Table 6. Switching Energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{(off)}$	Turn-off energy (from 90% V_{GS} to 0% I_D)	V_{DD} = 400 V, I_D = 2 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	7	-	µJ
		V_{DD} = 400 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	8	-	µJ

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 9 A R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Switching times test circuit for resistive load and Figure 19. Switching time waveform)	-	15	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off-delay time		-	61	-	ns
t_f	Fall time		-	16	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		16	A
I_{SDM} (1)	Source-drain current (pulsed)		-		64	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 16 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs, V_{DD} = 100 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	360		ns
Q_{rr}	Reverse recovery charge		-	5		µC
I_{RRM}	Reverse recovery current		-	28		A
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	445		ns
Q_{rr}	Reverse recovery charge		-	6.5		µC
I_{RRM}	Reverse recovery current		-	29		A

1. *Pulse width is limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

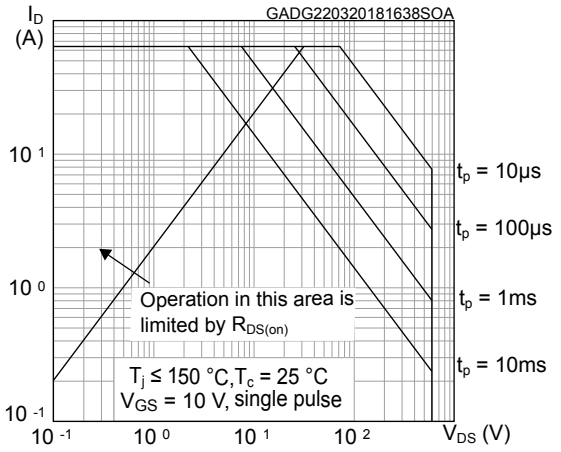


Figure 2. Thermal impedance

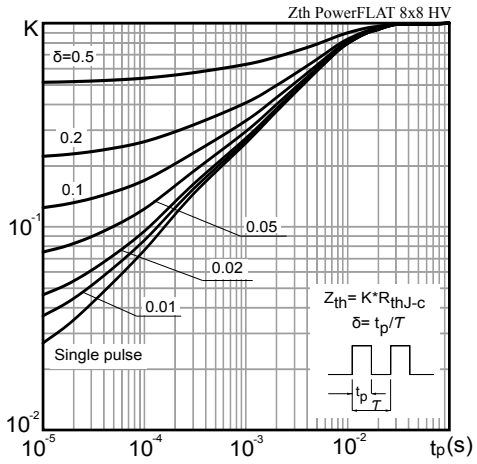


Figure 3. Output characteristics

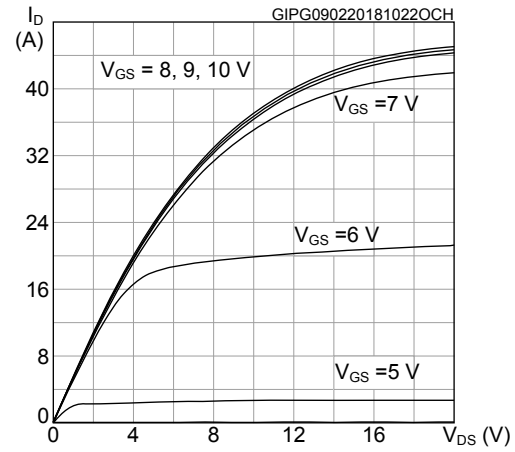


Figure 4. Transfer characteristics

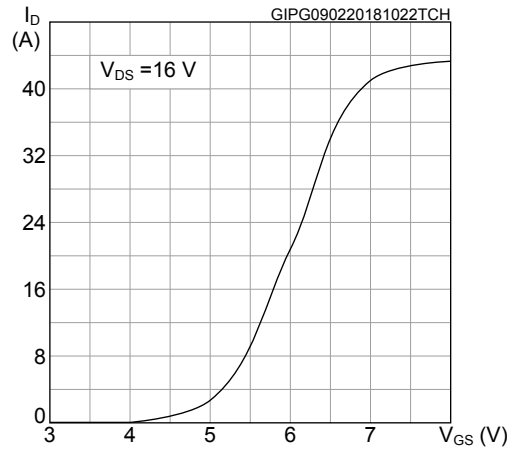


Figure 5. Gate charge vs gate-source voltage

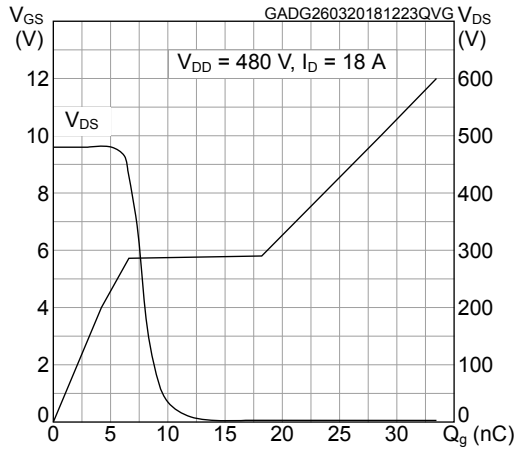


Figure 6. Static drain-source on-resistance

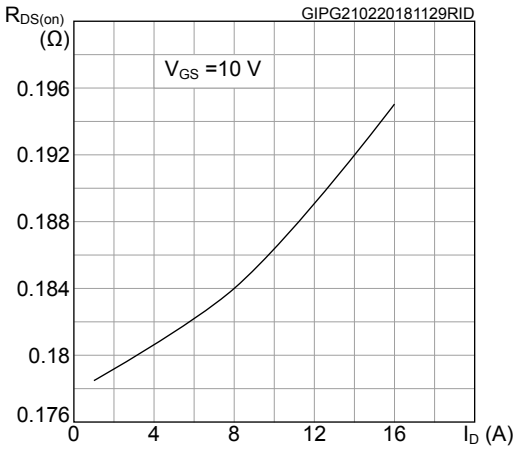


Figure 7. Capacitance variations

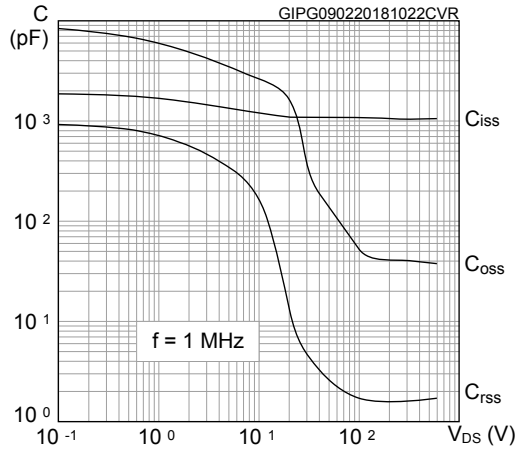


Figure 8. Output capacitance stored energy

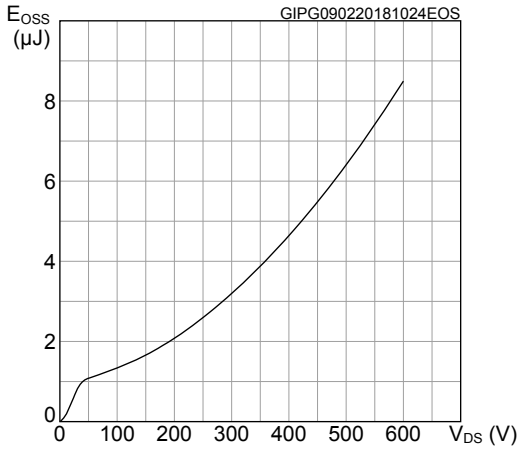


Figure 9. Turn-off switching energy vs drain current

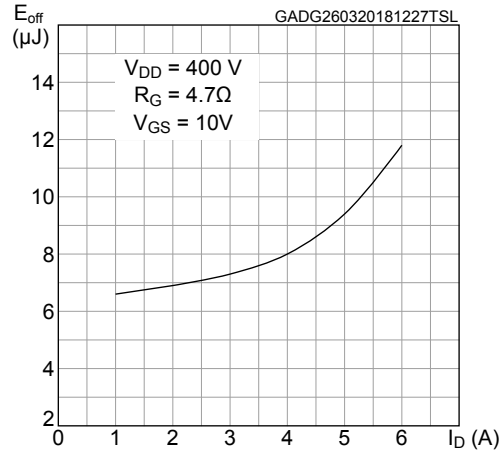


Figure 10. Normalized gate threshold voltage vs temperature

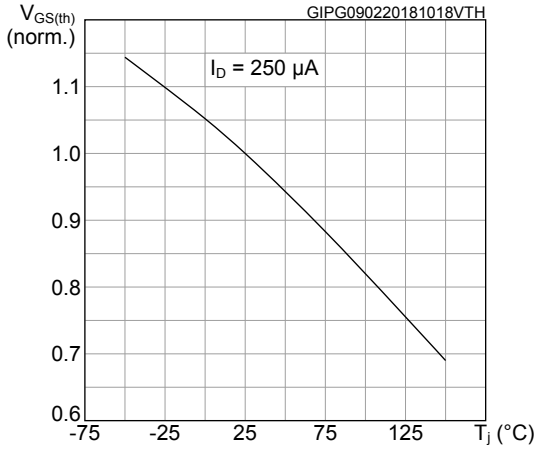


Figure 11. Normalized on-resistance vs temperature

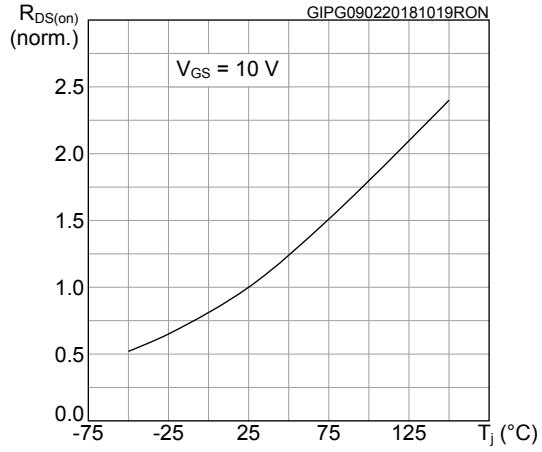


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature

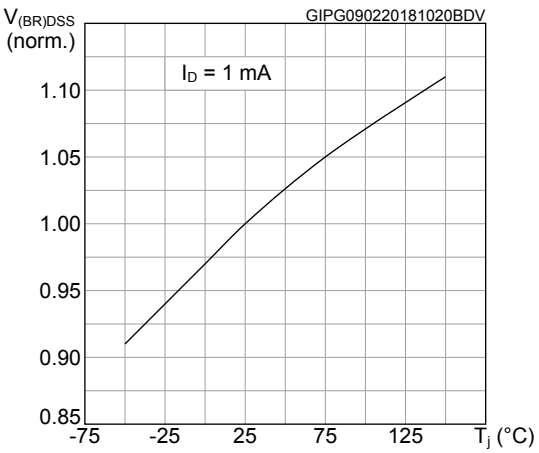
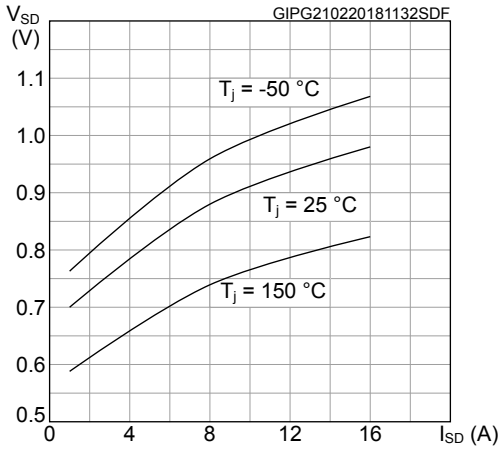


Figure 13. **Source-drain diode forward characteristics**



3 Test circuits

Figure 14. Switching times test circuit for resistive load

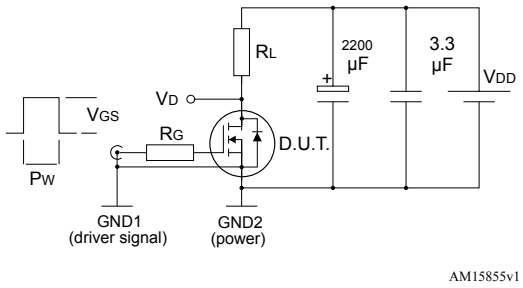


Figure 15. Gate charge test circuit

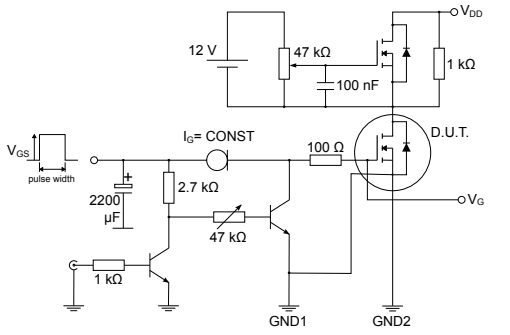


Figure 16. Test circuit for inductive load switching and diode recovery times

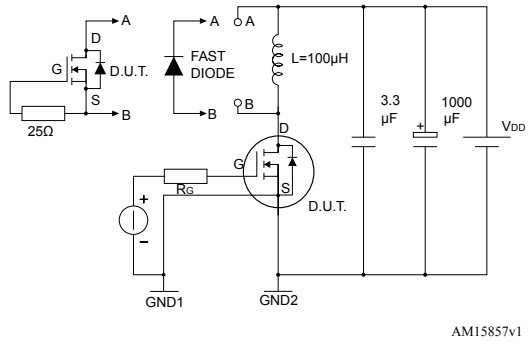


Figure 17. Unclamped inductive load test circuit

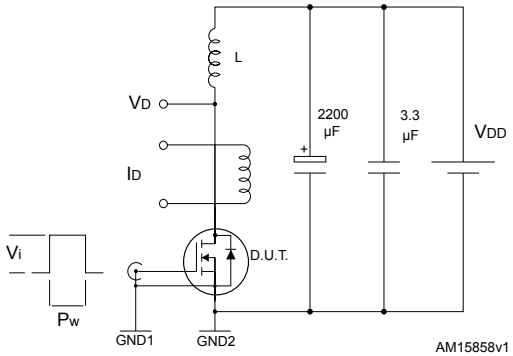


Figure 18. Unclamped inductive waveform

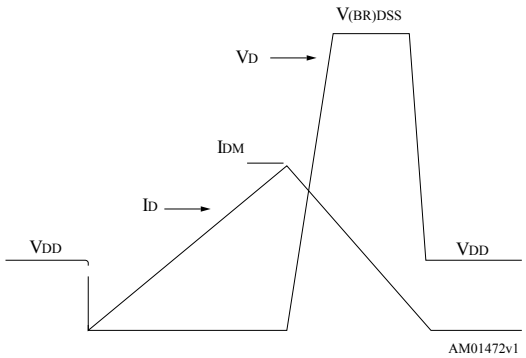
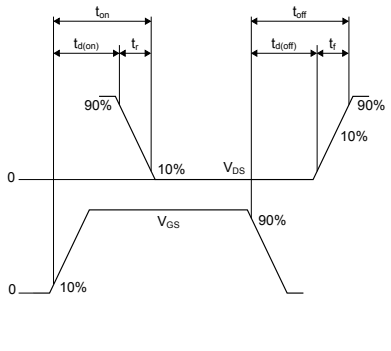


Figure 19. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 8x8 HV package information

Figure 20. **PowerFLAT™ 8x8 HV package outline**

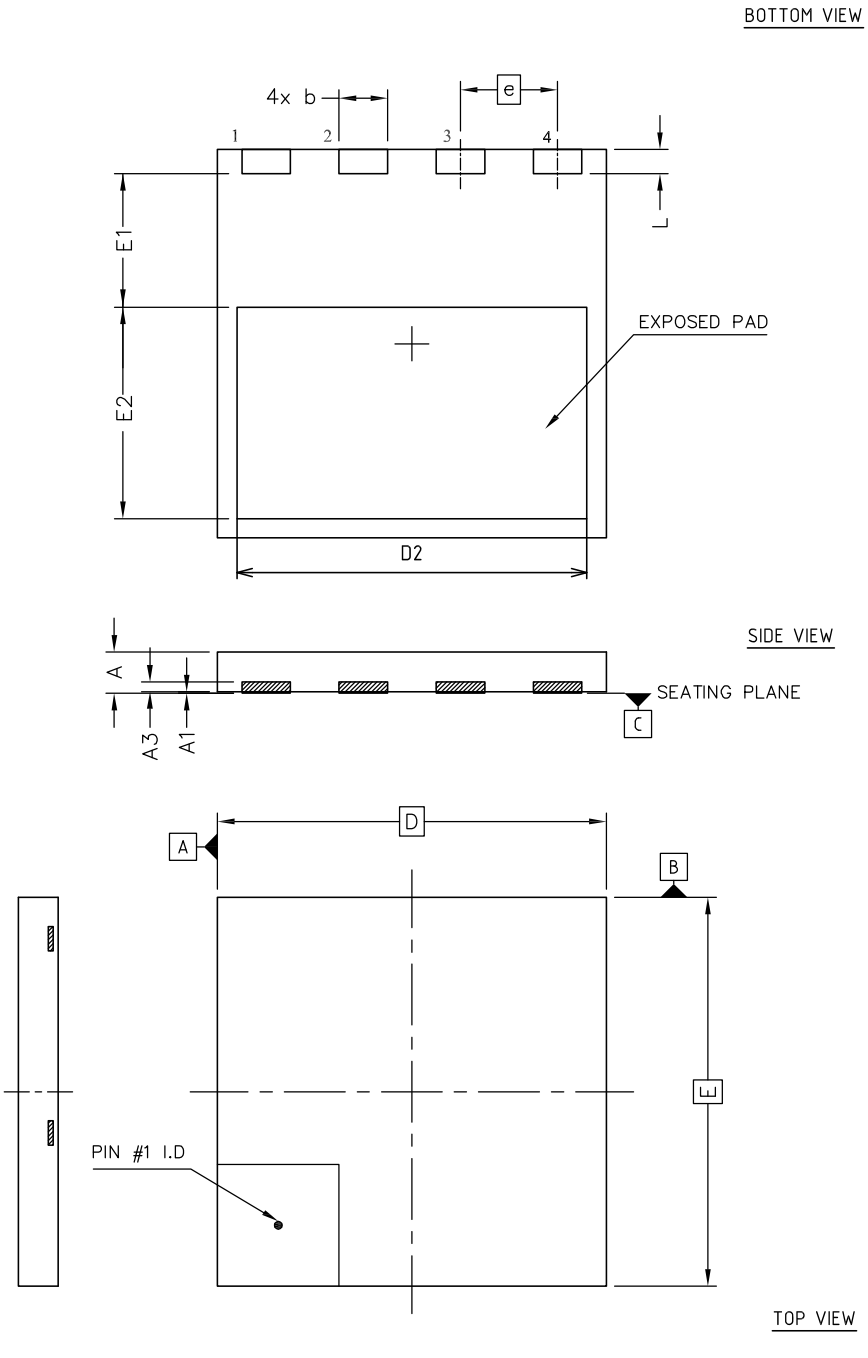
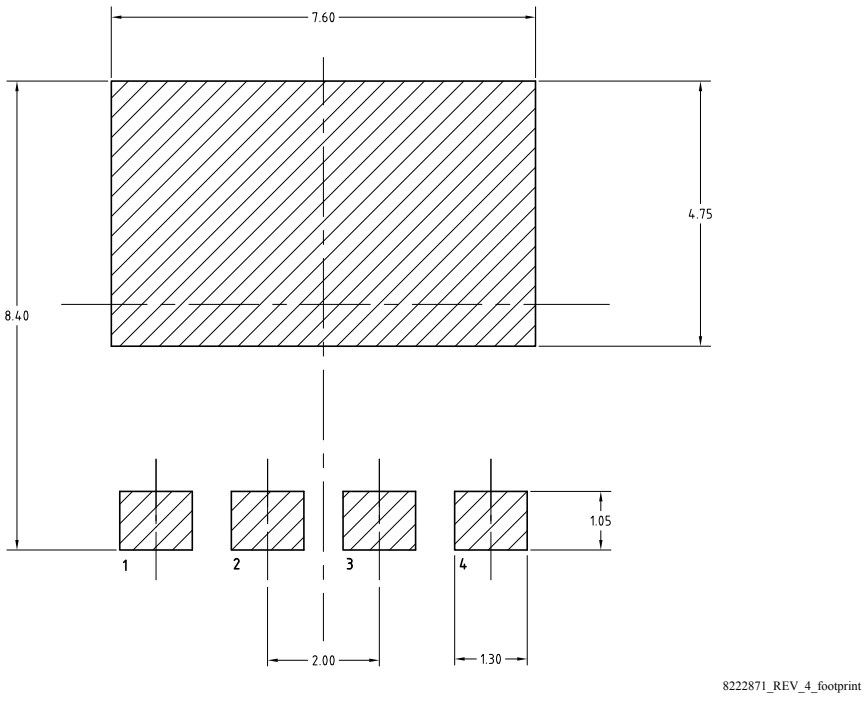


Table 9. **PowerFLAT™ 8x8 HV mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00 BSC	
L	0.40	0.50	0.60

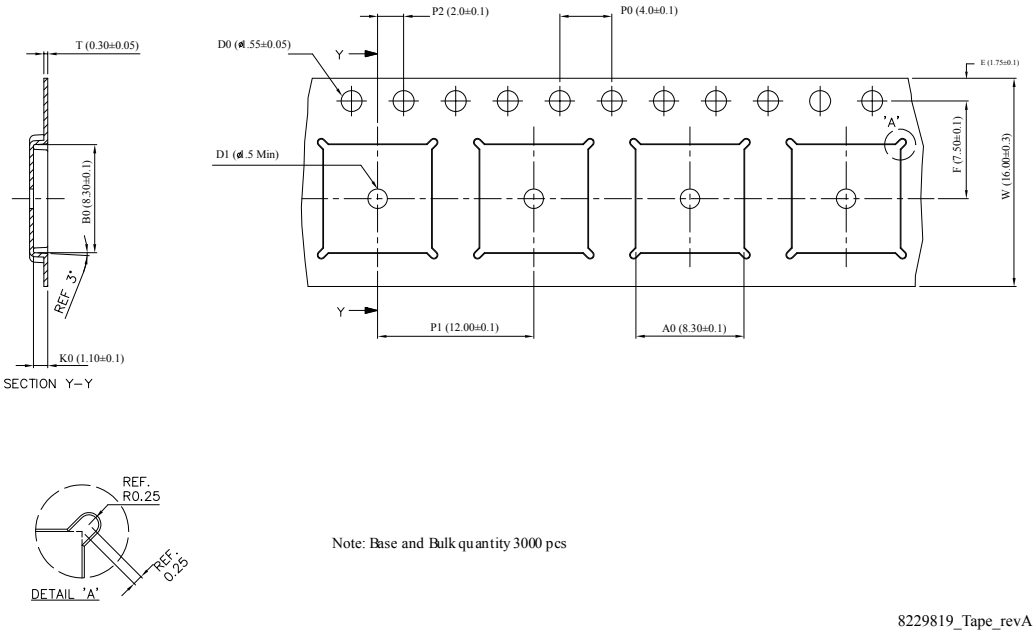
Figure 21. **PowerFLAT™ 8x8 HV footprint**



Note: All dimensions are in millimeters.

5 PowerFLAT™ 8x8 HV packing information

Figure 22. PowerFLAT™ 8x8 HV tape



Note: All dimensions are in millimeters.

Figure 23. PowerFLAT™ 8x8 HV package orientation in carrier tape

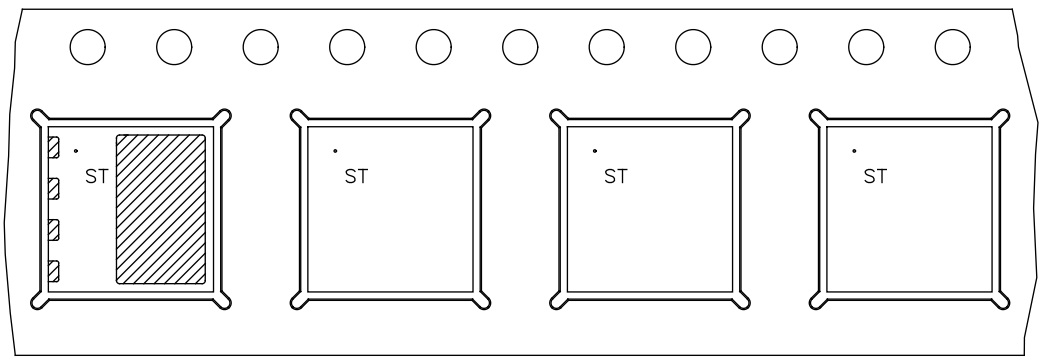
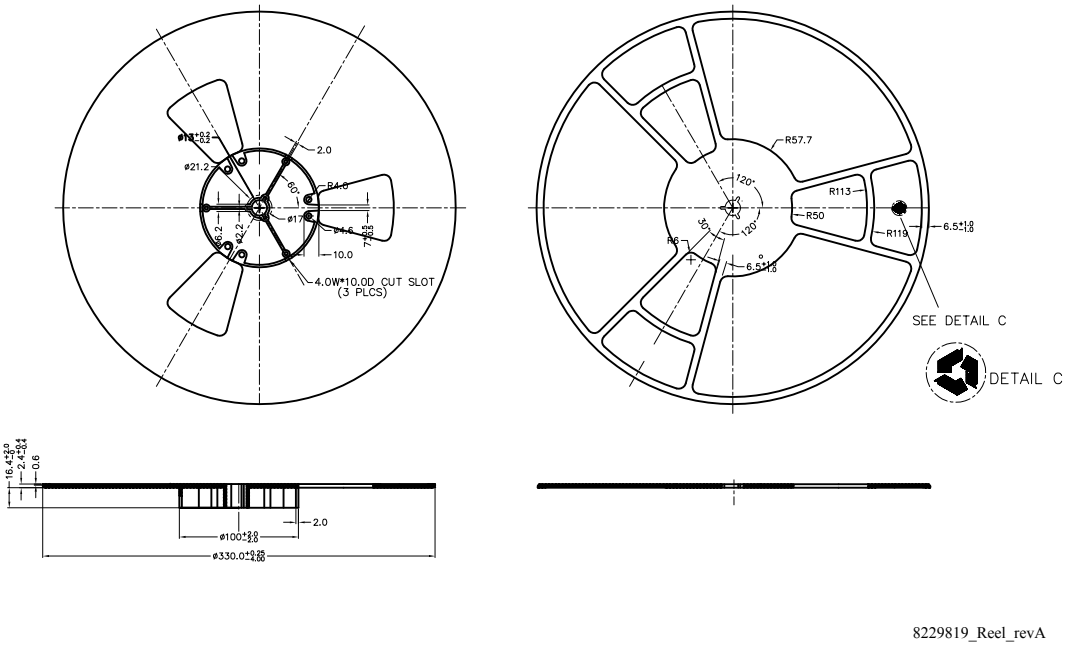


Figure 24. **PowerFLAT™ 8x8 HV reel**



Note: All dimensions are in millimeters.

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
02-Dec-2014	1	First release.
12-Jan-2015	2	Updated product status from “preliminary data” to “production data”.
20-Nov-2015	3	Updated: cover image and *Figure 1: "Internal schematic diagram"* Updated: *Section 3: "Test circuits"* Modified: *Section 4.1: "PowerFLAT 8x8 HV package information"* Minor text changes
21-Feb-2018	4	Removed maturity status indication from cover page. The document status is production data. Modified *Table 1. Absolute maximum ratings*, *Table 4. On/off states*, *Table 5. Dynamic*, *Table 6. Switching Energy*, *Table 7. Switching times* and *Table 8. Source drain diode*. Modified the entire *Section 2.1 Electrical characteristics (curves)*. Minor text changes.
26-Mar-2018	5	Modified Table 1. Absolute maximum ratings, Table 4. On/off states, Table 5. Dynamic, Table 6. Switching Energy, Table 7. Switching times, Table 8. Source drain diode and Section 2.1 Electrical characteristics (curves). Minor text changes.

Contents