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# BUH50G

## Switch-mode NPN Silicon Planar Power Transistor

The BUH50G has an application specific state-of-art die designed for use in 50 W HALOGEN electronic transformers and switch-mode applications.

### Features

- Improved Efficiency Due to Low Base Drive Requirements:  
High and Flat DC Current Gain  $h_{FE}$   
Fast Switching
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproducible Parametric Distributions
- Specified Dynamic Saturation Data
- Full Characterization at 125°C
- These Devices are Pb-Free and are RoHS Compliant\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	500	Vdc
Collector-Base Breakdown Voltage	$V_{CBO}$	800	Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	800	Vdc
Emitter-Base Voltage	$V_{EBO}$	9	Vdc
Collector Current – Continuous	$I_C$	4	Adc
Collector Current – Peak (Note 1)	$I_{CM}$	8	Adc
Base Current – Continuous	$I_B$	2	Adc
Base Current – Peak (Note 1)	$I_{BM}$	4	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_D$	50 0.4	W W/°C
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq$  10%.

### THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	$T_L$	260	°C

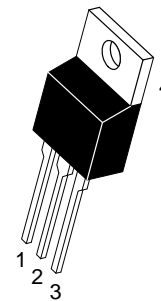
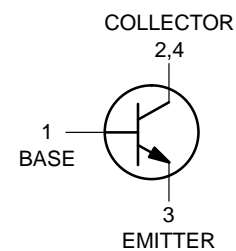
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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**POWER TRANSISTOR  
4 AMPERES  
800 VOLTS, 50 WATTS**



TO-220  
CASE 221A  
STYLE 1

### MARKING DIAGRAM



BUH50 = Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping
BUH50G	TO-220 (Pb-Free)	50 Units / Rail

# BUH50G

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (I <sub>C</sub> = 100 mA, L = 25 mH)	V <sub>CEO(sus)</sub>	500			Vdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEO</sub> , I <sub>B</sub> = 0)	I <sub>CEO</sub>			100	μAdc
Collector Cutoff Current @ T <sub>C</sub> = 25°C (V <sub>CE</sub> = Rated V <sub>CES</sub> , V <sub>EB</sub> = 0) @ T <sub>C</sub> = 125°C	I <sub>CES</sub>			100 1000	μAdc
Emitter-Cutoff Current (V <sub>EB</sub> = 9 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>			100	μAdc

### ON CHARACTERISTICS

Base-Emitter Saturation Voltage (I <sub>C</sub> = 1 Adc, I <sub>B</sub> = 0.33 Adc) (I <sub>C</sub> = 2 Adc, I <sub>B</sub> = 0.66 Adc) 25°C (I <sub>C</sub> = 2 Adc, I <sub>B</sub> = 0.66 Adc) 100°C	V <sub>BE(sat)</sub>		0.86 0.94 0.85	1.2 1.6 1.5	Vdc
Collector-Emitter Saturation Voltage (I <sub>C</sub> = 1 Adc, I <sub>B</sub> = 0.33 Adc)  (I <sub>C</sub> = 2 Adc, I <sub>B</sub> = 0.66 Adc)  (I <sub>C</sub> = 3 Adc, I <sub>B</sub> = 1 Adc)	V <sub>CE(sat)</sub>	@ T <sub>C</sub> = 25°C  @ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C  @ T <sub>C</sub> = 25°C	0.2  0.32 0.29  0.5	0.5  0.6 0.7  1	Vdc
DC Current Gain (I <sub>C</sub> = 1 Adc, V <sub>CE</sub> = 5 Vdc)  (I <sub>C</sub> = 2 Adc, V <sub>CE</sub> = 5 Vdc)	h <sub>FE</sub>	@ T <sub>C</sub> = 25°C  @ T <sub>C</sub> = 25°C	7  5	13  10	-  -

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 1 MHz)	f <sub>T</sub>	4			MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 1 MHz)	C <sub>ob</sub>		50	100	pF
Input Capacitance (V <sub>EB</sub> = 8 Vdc)	C <sub>ib</sub>		850	1200	pF

### DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I <sub>B1</sub> reaches 90% of final I <sub>B1</sub>	I <sub>C</sub> = 1 A I <sub>B1</sub> = 0.33 A V <sub>CC</sub> = 300 V	@ 1 μs	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	V <sub>CE(dsat)</sub>	1.75 5		V
		@ 3 μs	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C		0.3 0.5		V
	I <sub>C</sub> = 2 A I <sub>B1</sub> = 0.66 A V <sub>CC</sub> = 300 V	@ 1 μs	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	6 14		V	
		@ 3 μs	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	0.75 4		V	

### SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn-on Time	I <sub>C</sub> = 2 Adc, I <sub>B1</sub> = 0.4 Adc I <sub>B2</sub> = 0.4 Adc V <sub>CC</sub> = 125 Vdc	@ T <sub>C</sub> = 25°C	t <sub>on</sub>	95	250	ns
Turn-off Time		@ T <sub>C</sub> = 25°C	t <sub>off</sub>	2.5	3.5	μs
Turn-on Time	I <sub>C</sub> = 2 Adc, I <sub>B1</sub> = 0.4 Adc I <sub>B2</sub> = 1 Adc V <sub>CC</sub> = 125 Vdc	@ T <sub>C</sub> = 25°C	t <sub>on</sub>	110	250	ns
Turn-off Time		@ T <sub>C</sub> = 25°C	t <sub>off</sub>	0.95	2	μs
Turn-on Time	I <sub>C</sub> = 1 Adc, I <sub>B1</sub> = 0.3 Adc I <sub>B2</sub> = 0.3 Adc V <sub>CC</sub> = 125 Vdc	@ T <sub>C</sub> = 25°C	t <sub>on</sub>	100	200	ns
Turn-off Time		@ T <sub>C</sub> = 25°C	t <sub>off</sub>	2.9	3.5	μs

### SWITCHING CHARACTERISTICS: Inductive Load (V<sub>clamp</sub> = 300 V, V<sub>CC</sub> = 15 V, L = 200 μH)

Fall Time	I <sub>C</sub> = 2 Adc I <sub>B1</sub> = 0.4 Adc I <sub>B2</sub> = 1 Adc	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>f</sub>	80 95	150	ns
Storage Time		@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>s</sub>	1.2 1.7	2.5	μs
Crossover Time		@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>c</sub>	150 180	300	ns
Fall Time	I <sub>C</sub> = 2 Adc I <sub>B1</sub> = 0.66 Adc I <sub>B2</sub> = 1 Adc	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>f</sub>	90 100	150	ns
Storage Time		@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>s</sub>	1.7 2.5	2.75	μs
Crossover Time		@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>c</sub>	190 220	350	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL STATIC CHARACTERISTICS

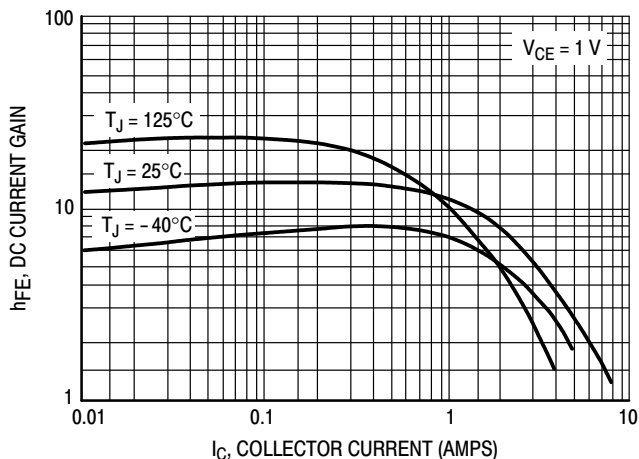


Figure 1. DC Current Gain @ 1 Volt

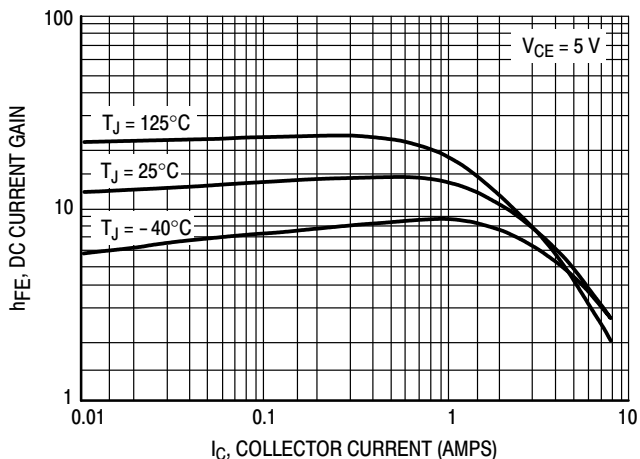


Figure 2. DC Current Gain @ 5 Volt

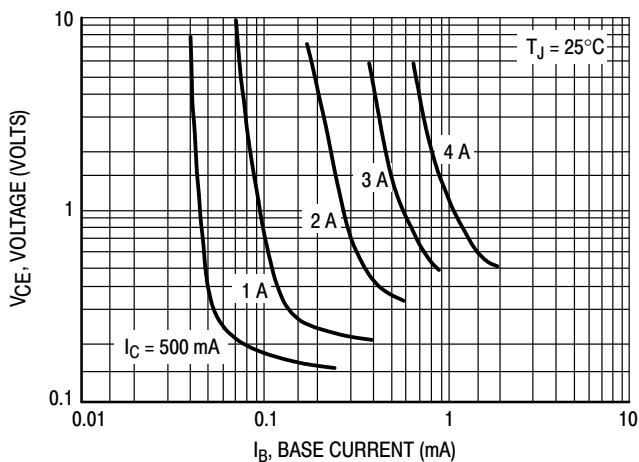


Figure 3. Collector Saturation Region

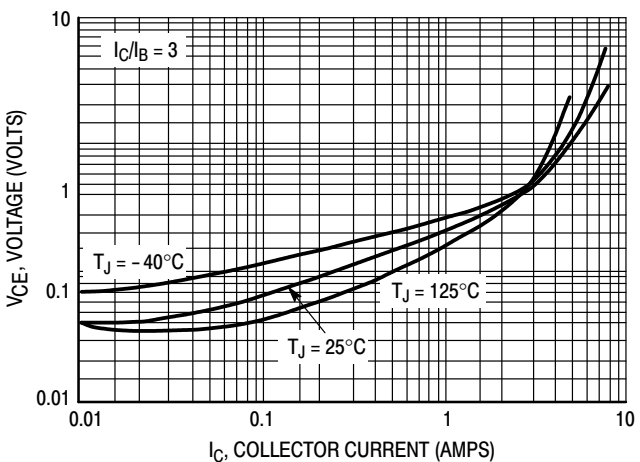


Figure 4. Collector-Emmitter Saturation Voltage

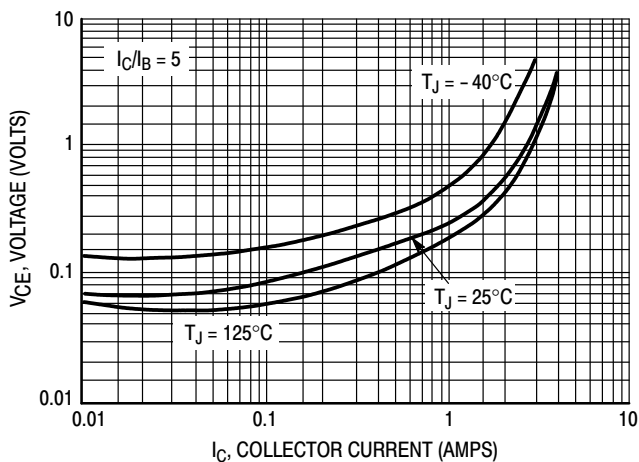


Figure 5. Collector-Emmitter Saturation Voltage

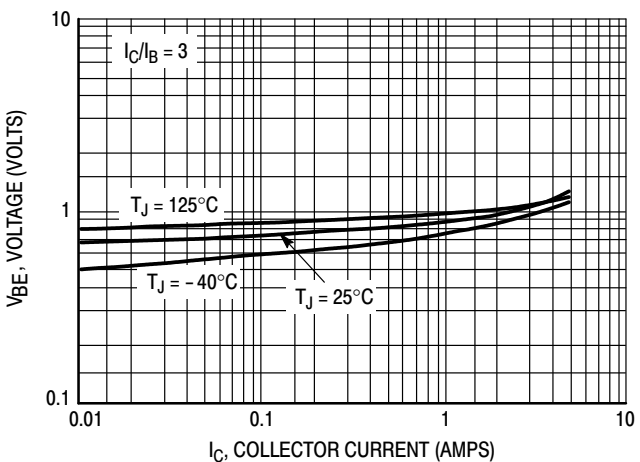


Figure 6. Base-Emmitter Saturation Region

# BUH50G

## TYPICAL STATIC CHARACTERISTICS

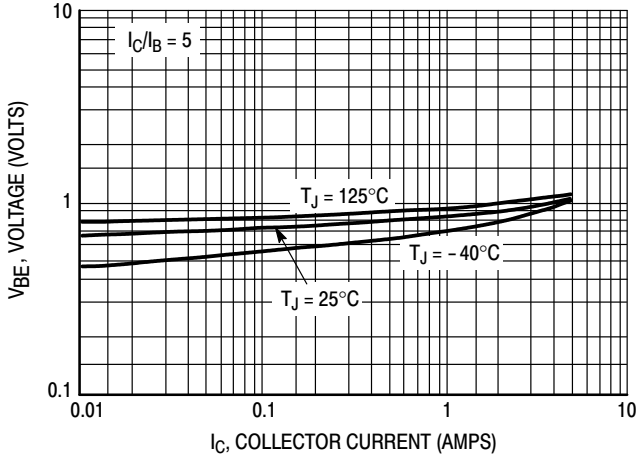


Figure 7. Base-Emitter Saturation Region

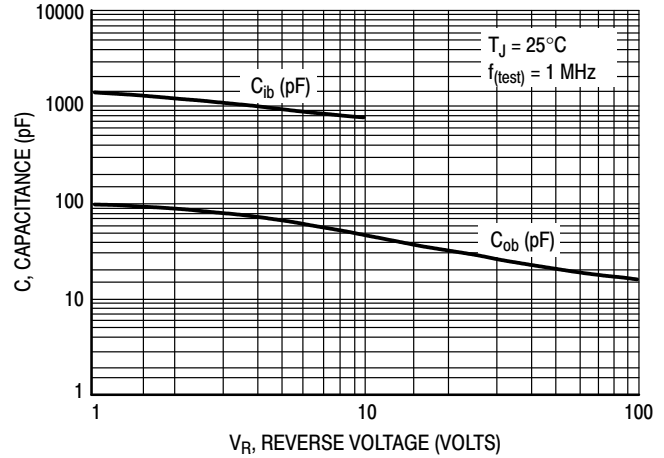


Figure 8. Capacitance

## TYPICAL SWITCHING CHARACTERISTICS

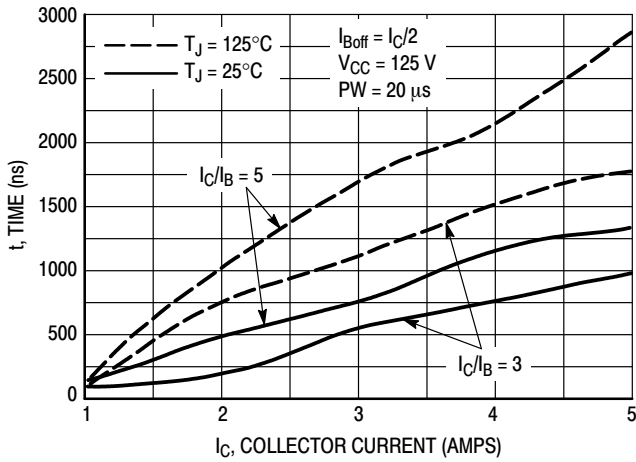


Figure 9. Resistive Switching,  $t_{on}$

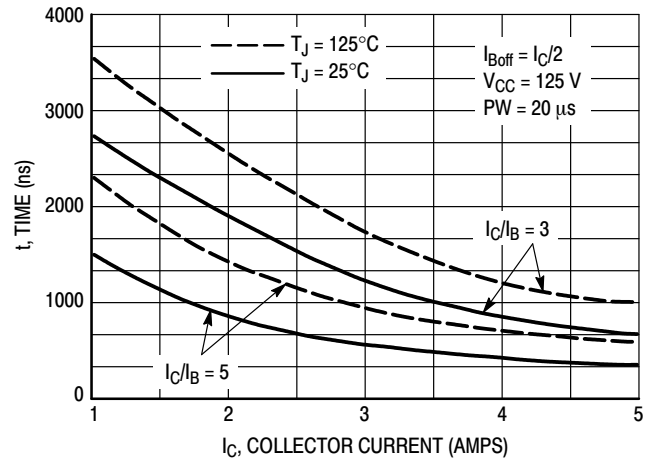


Figure 10. Resistive Switch Time,  $t_{off}$

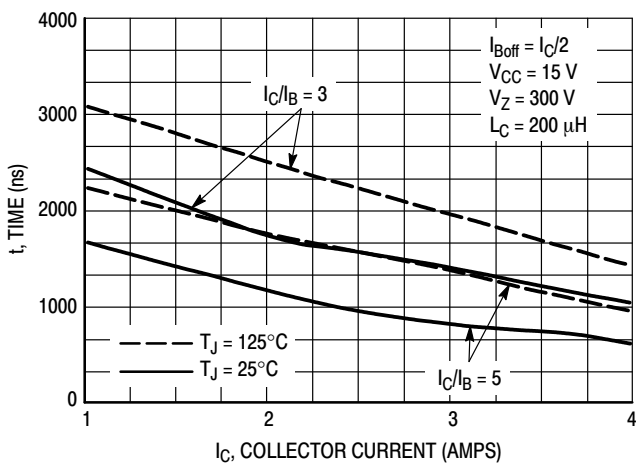


Figure 11. Inductive Storage Time,  $t_{si}$

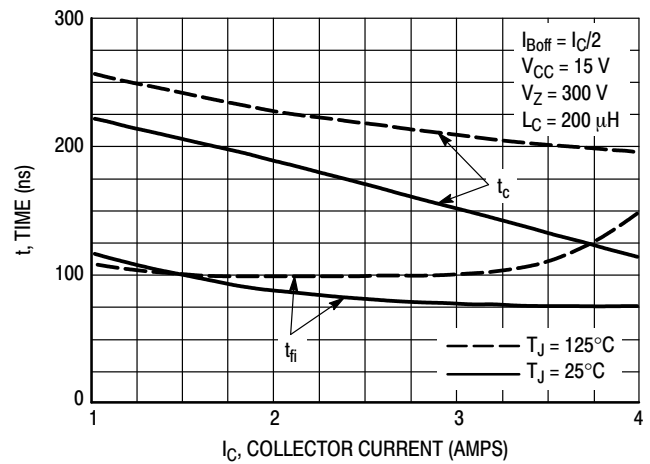


Figure 12. Inductive Storage Time,  $t_c$  &  $t_{fi}$  @  $I_C/I_B = 3$

# BUH50G

## TYPICAL CHARACTERISTICS

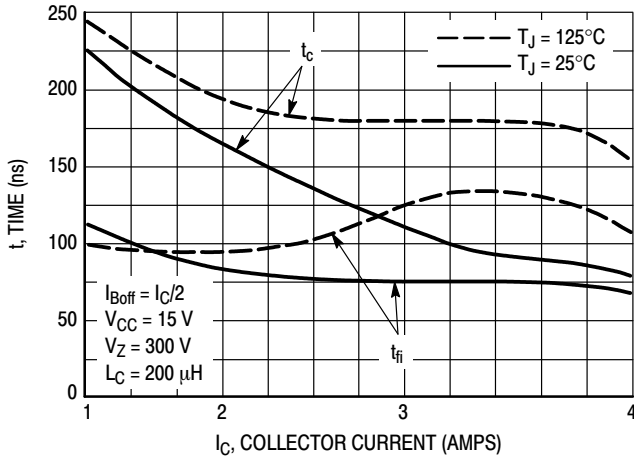


Figure 13. Inductive Switching,  $t_c$  &  $t_{fi}$  @  $I_C/I_B = 5$

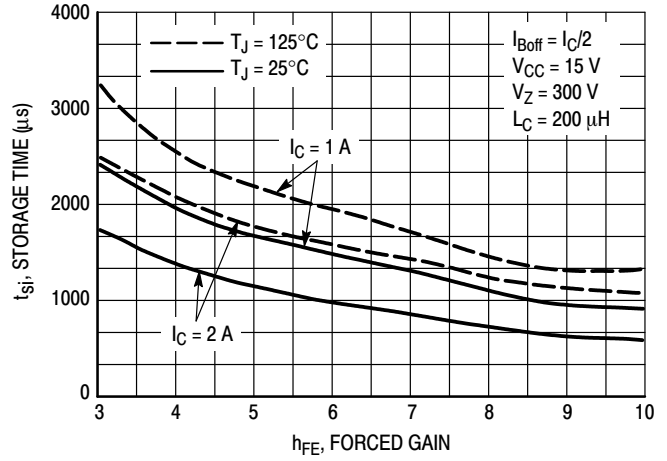


Figure 14. Inductive Storage Time

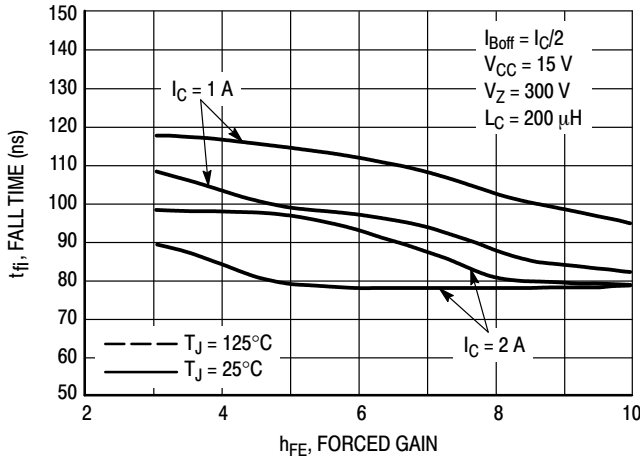


Figure 15. Inductive Fall Time

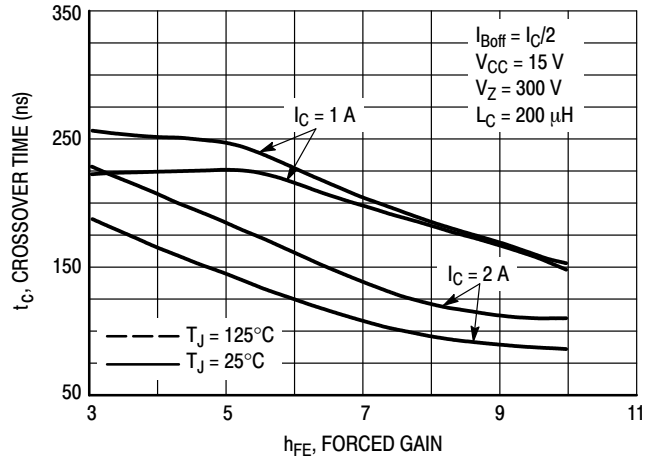


Figure 16. Inductive Crossover Time

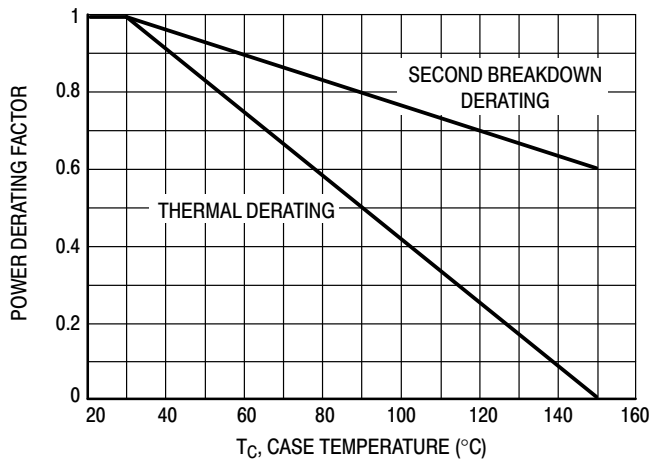


Figure 17. Forward Power Derating

# BUH50G

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 20 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be de-rated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not de-rate the same as thermal limitations. Allowable current at the voltages shown on Figure 20 may be found at any case temperature by using the appropriate curve on Figure 17.

$T_{J(pk)}$  may be calculated from the data in Figure 22. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 21). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

## TYPICAL CHARACTERISTICS

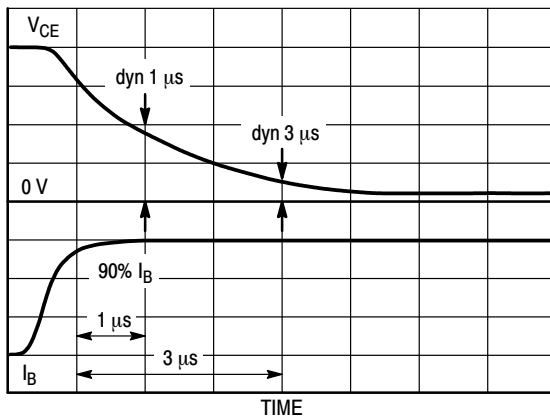


Figure 18. Dynamic Saturation Voltage

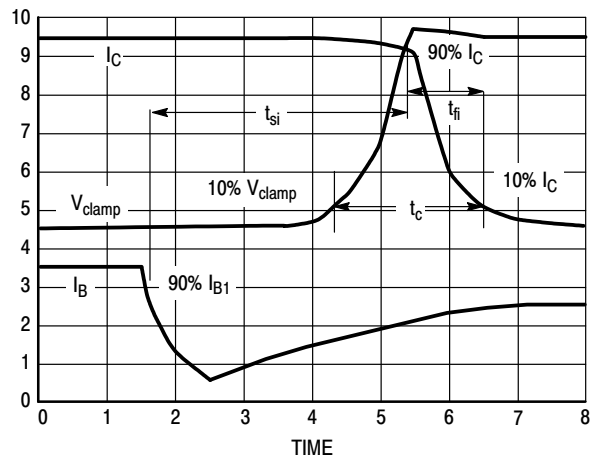


Figure 19. Inductive Switching Measurements

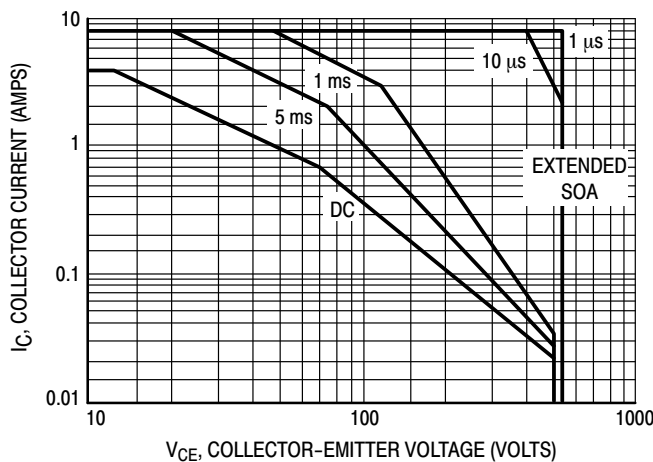


Figure 20. Forward Bias Safe Operating Area

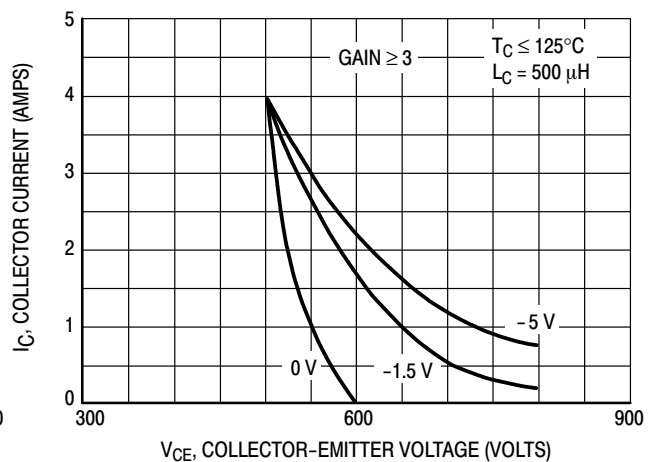
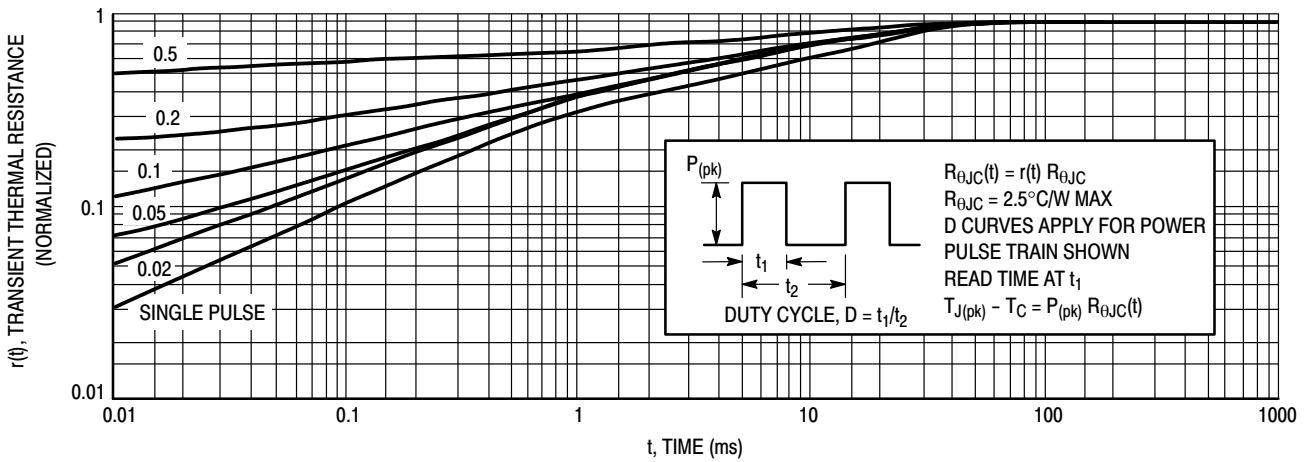
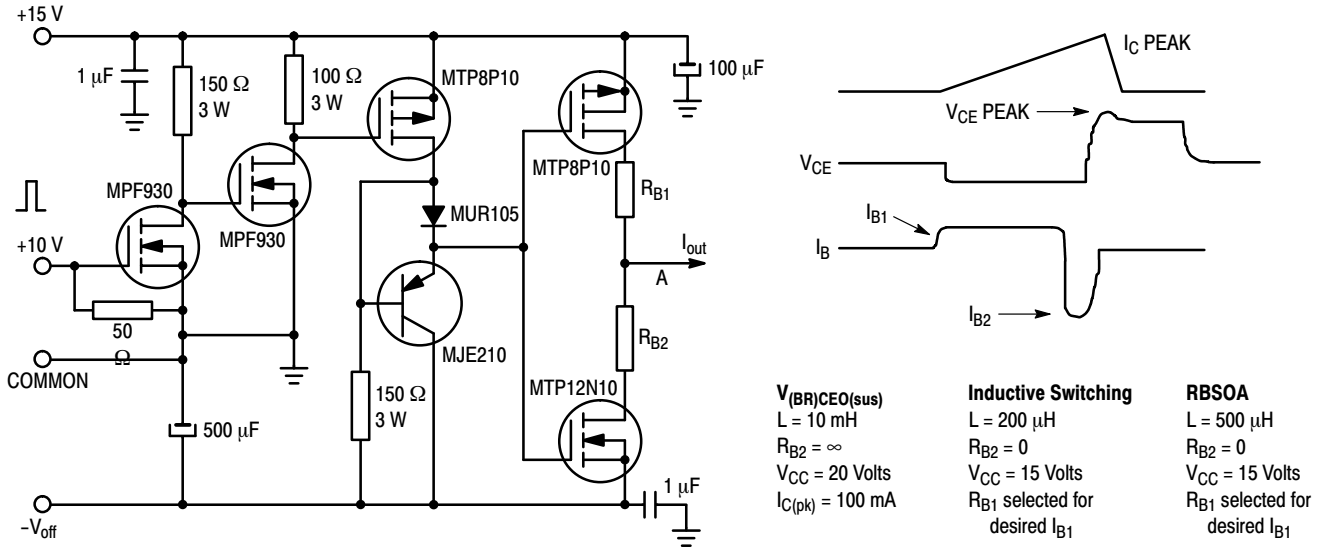


Figure 21. Reverse Bias Safe Operating Area

# BUH50G

## TYPICAL CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit

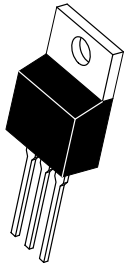




# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

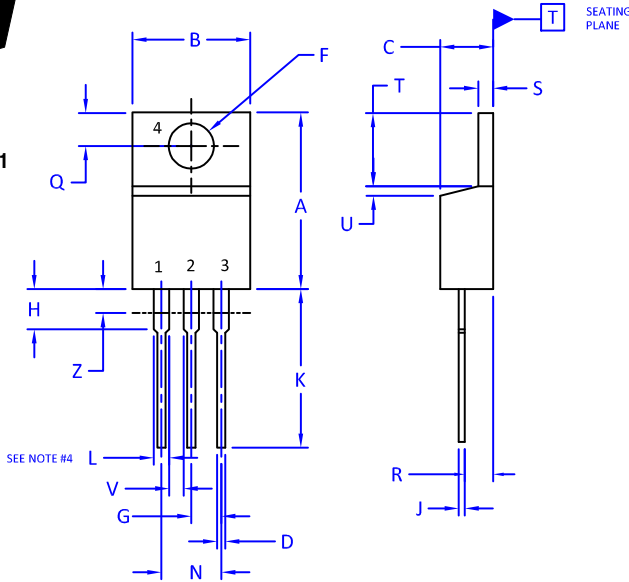
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SCALE 1:1

### TO-220 CASE 221A-09 ISSUE AJ

DATE 05 NOV 2019



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

STYLE 3:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 6:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 8:

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

STYLE 9:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 10:

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

STYLE 11:

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

STYLE 12:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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