

STB80N4F6AG

Automotive-grade N-Channel 40 V, 5.5 mΩ typ.,80 A STripFET™ F6 Power MOSFET in a D²PAK package

Datasheet - production data

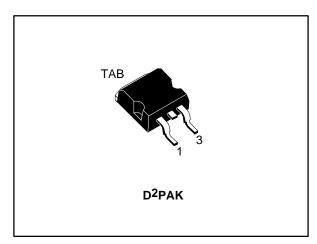
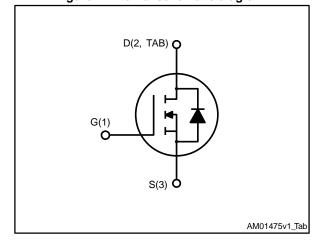


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	l _D
STB80N4F6AG	40 V	6 mΩ	80 A

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET $^{\text{TM}}$ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{\text{DS(on)}}$ in all packages.

Table 1: Device summary

Order code	Marking	Package Packaging	
STB80N4F6AG	80N4F6	D²PAK	Tape and Reel

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STB80N4F6AG Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
ΙD	Drain current (continuous) at T _C = 25 °C	80	Α
ΙD	Drain current (continuous) at Tc= 100 °C	56	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	320	Α
Ртот	Total dissipation at T _C = 25 °C	70	W
l _{AV}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J max)	40	Α
E _{AS}	Single pulse avalanche energy(Starting T_{J} = 25 °C, = I_{D} = I_{AV} , V_{DD} = 25 V)	149	mJ
T _{stg}	Storage temperature	- 55 to 175	°C
Tj	Max. operating junction temperature	175	°C

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max.	2.14	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-ambient max.	35	°C/W

Notes:

⁽¹⁾ Pulse width limited by safe operating area.

⁽¹⁾When mounted on FR-4 board of inch2, 2 oz Cu

Electrical characteristics STB80N4F6AG

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4: On/Off States

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	40			V
		V _{DS} = 40 V			1	μA
IDSS	Zero gate voltage drain current (V _{GS} = 0V)	V _{DS} = 40 V Tj = 125 °C			100	μΑ
Igss	Gate-body leakage current (V _{DS} = 0 V)	V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 40 A		5.5	6	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	2150	-	pF
Coss	Output capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz},$	-	335	-	pF
Crss	Reverse transfer capacitance	$V_{GS} = 0 V$	-	160	-	pF
Qg	Total gate charge	$V_{DD} = 20 \text{ V}, I_D = 80 \text{ A},$	-	36	-	nC
Qgs	Gate-source charge	V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge	-	11	ı	nC
Q_{gd}	Gate-drain charge	behavior")	-	9	1	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 20 \text{ V}, I_D = 40 \text{ A R}_G = 4.7 \Omega,$	-	10.5	-	ns
t _r	Rise time	$V_{GS} = 20 \text{ V, } I_{GS} = 40 \text{ A K}_{GS} = 4.7 \Omega$, $V_{GS} = 10 \text{ V(see } Figure 15: "Test")$	-	7.6	-	ns
t _{d(off)}	Turn-off-delay time	circuit for inductive load switching	-	46.1	-	ns
t _f	Fall time	and diode recovery times")	-	11.9	-	ns

Table 7: Source-drain diode

Symbol	bol Parameter Test conditions		Min.	Тур.	Max.	Unit
I _{SD}	Source drain current				80	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				320	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 40 A, V _{GS} = 0 V			1.3	V
t _{rr}	Reverse recovery time	I _{SD} = 80 A, di/dt = 100 A/μs,		41.1		ns
Q _{RR}	Reverse recovery charge	V _{DD} = 32 V (See <i>Figure 17: "Unclamped</i>		43.6		nC
I _{RRM}	Reverse recovery current	inductive waveform")		2.1		Α

Notes:

 $[\]ensuremath{^{(1)}}\mbox{Pulse}$ width limited by safe operating area.

 $^{^{(2)}}$ Pulsed: pulse duration = 300 μ s, duty cycle 1.5%

2.1 Electrical characteristics (curves)

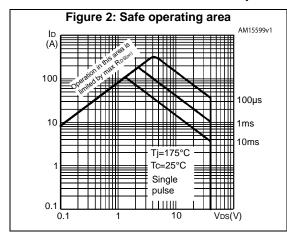
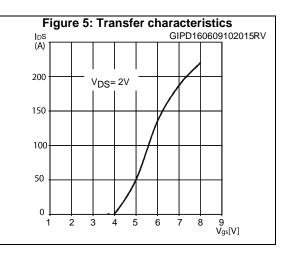
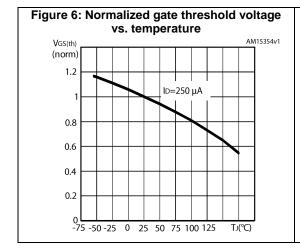
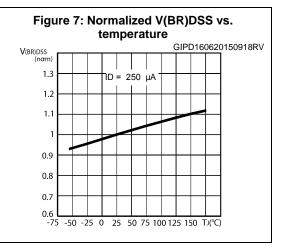


Figure 3: Thermal impedance $\frac{2800 PC}{0.2}$ 0.2 0.05 0.02 0.02 0.02 0.02 0.01 0.05 0.02 0.01







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STB80N4F6AG Electrical characteristics

Figure 8: Static drain-source on-resistance

RDS(on) (mΩ)

6.5

RDS(on)

RDS(on)

10

RDS(on)

10

RDS(on)

10

RDS(on)

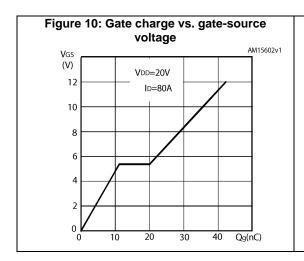
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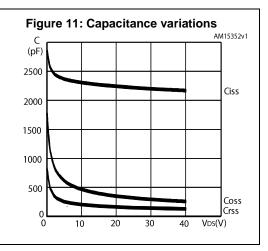
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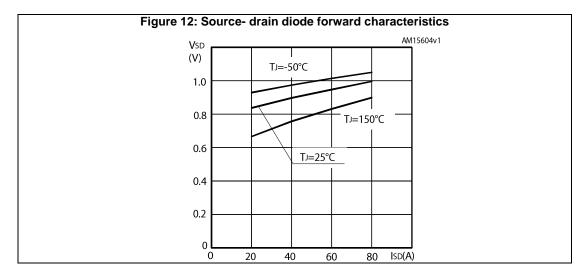
60

80

RDS(on)







Test circuits STB80N4F6AG

3 Test circuits

Figure 13: Test circuit for resistive load switching times

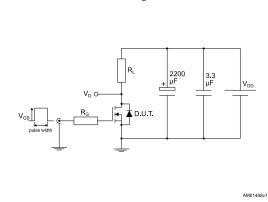


Figure 14: Test circuit for gate charge behavior

12 V 47 KΩ 100 NF D.U.T.

Vos 1 1 KΩ

Vos 1 1 KΩ

AM01469v1

Figure 15: Test circuit for inductive load switching and diode recovery times

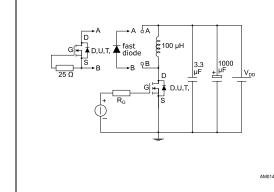


Figure 16: Unclamped inductive load test circuit

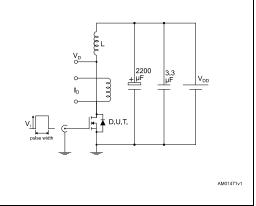


Figure 17: Unclamped inductive waveform

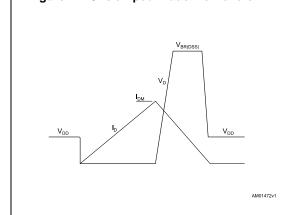
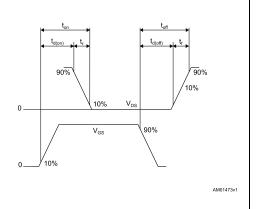


Figure 18: Switching time waveform



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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 D²PAK package information

E1 c2-L1 THERMAL PAD SEATING PLANE COPLANARITY A1 0.25 GAUGE PLANE V2_ 0079457_A_rev22

Figure 19: D²PAK (TO-263) type A package outline

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Table 8: D²PAK (TO-263) type A package mechanical data

	ble 6. D-FAR (10-203) tyl	mm	
Dim.	Min.	Тур.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
С	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
е		2.54	
e1	4.88		5.28
Н	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

9.75

16.9

2.54

Feotprint

Figure 20: D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 D²PAK packing information

Figure 21: Tape outline

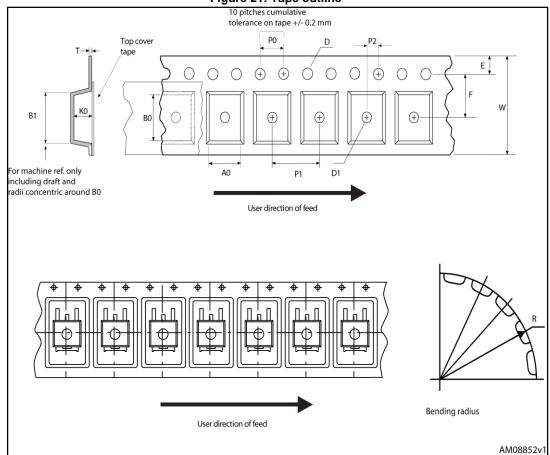


Figure 22: Reel outline

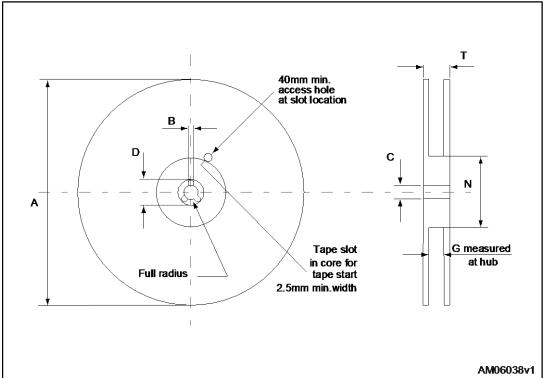


Table 9: D2PAK tape and reel mechanical data

	Таре			Reel	
Dim	mn mr		Dim	m	m
Dim.	Min.	Max.	Dim.	Min.	Max.
A0	10.5	10.7	А		330
В0	15.7	15.9	В	1.5	
D	1.5	1.6	С	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	Т		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base q	uantity	1000
P2	1.9	2.1	Bulk qu	uantity	1000
R	50				
Т	0.25	0.35			
W	23.7	24.3			

Revision history STB80N4F6AG

5 Revision history

Table 10: Document revision history

Date	Revision	Changes	
16-Jun-2015	1	Initial release	
18-Nov-2015	2	Document status promoted from preliminary to production data. Updated title and features in cover page.	

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