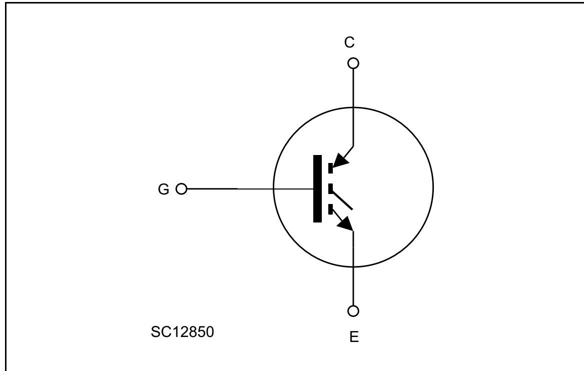
STG80V60FD7

600 V, 80 A trench gate field-stop V series IGBT die in D7 packing

Datasheet - preliminary data



Description

This die is an IGBT developed using an advanced propriety trench gate and field-stop structure. The device is a part of the V series IGBTs.

Features

- Maximum junction temperature: T_J = 175 °C
- Very high speed switching series
- Tail-less switching off
- $V_{CE(sat)}$ = 1.85 V (typ.)@ I_C = 80A
- Tight parameters distribution
- Safer paralleling

Applications

- Solar
- UPS
- Welding
- High frequency converter
- PFC

Table 1. Device summary

Order code	V_{CE}	I_{CN}	Die size	Packing
STG80V60FD7	600V	80 A	6.50 x 6.30 mm^2	D7

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Mechanical parameters

Table 2. Mechanical parameters

Parameter		Value	Unit
Die size		6.50 x 6.30	mm^2
Wafer size		200	mm
Die thickness		70	µm
Maximum possible dice per wafer		654	dice
Front side passivation		Silicone nitride	
Emitter pad size (x2)		5.84 x 1.65	mm^2
Gate pad size		0.36 x 0.50	mm^2
Front side metallization	composition	AlSiCu	
	thickness	4.5	µm
Back side metallization	composition	Al/Ti/NiV/Ag	
	thickness	0.65	µm
Die bond		Electrically conductive glue or soft solder	
Recommended wire bonding		≤ 500	µm

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2 Electrical ratings

Table 3. Absolute maximum ratings (T_J = 25 °C, unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0)	600	V
V_{GE}	Gate-emitter voltage	±20	V
I_C	Continuous collector current limited by T_{Jmax}	80(1)	A
I_{CP}(1)	Pulsed collector current, T_p limited by T_{Jmax}	240	A
T_j	Operating junction temperature	- 55 to 175	°C

1. Depending on thermal properties of assembly

Table 4. Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	I_C = 2 mA, V_{GE} = 0 V	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C= 15 A			2.2	V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = $V_{GE,}$ I_C = 1 mA	5	6	7	V
I_{GES}	Gate-emitter leakage current	V_{GE} = ± 20V, V_{CE} = 0 V			± 250	nA
I_{CES}	Collector cut-off current	V_{CE} = 650 V, V_{GE} = 0 V			25	µA

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Table 5. Electrical characteristics (1)
(not tested at chip level, verified by design/characterization)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15V, I_C = 80 A	-	1.85	2.3	V
		V_{GE} = 15V, I_C = 80 A T_J = 175°C	-	2.4		V
C_{ies}	Input capacitance	V_{CE}= 25 V, f = 1 Mhz V_{GE}= 0 V	-	10800		pF
C_{oes}	Output capacitance		-	390		pF
C_{res}	Reverse transfer capacitive		-	220		pF
Q_g	Total gate charge	V_{CC} = 480 V, I_C = 80 A, V_{GE} = 15V	-	448		nC
Q_{ge}	Gate emitter charge		-	76		nC
Q_{gc}	Gate collector charge		-	184		nC

1. Value are referred to packaged device STGW80V60DF with specific circuit test

Table 6. Switching characteristics(1) on inductive load
(not tested at chip level, verified by design/characterization)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{cc} = 400 V, I_c = 80 A, V_{GE} = 15 V, R_G= 10 Ω T_J = 25 °C	-	60	-	ns
t_r	Current rise time		-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	220	-	ns
t_f	Fall time		-	17	-	ns
E_{off}	Switching off energy		-	1	-	mJ
$t_{d(on)}$	Turn-on delay time	V_{cc} = 400 V, I_c = 80 A, V_{GE} = 15 V, R_G= 10 Ω T_J = 175 °C	-	60	-	ns
t_f	Current rise time		-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	240	-	ns
t_f	Fall time		-	22	-	ns
E_{off}	Switching off energy		-	1.25	-	mJ

1. Values are strongly dependent on package/module design and mounting technology. These value are referred to the characterization for the device STGW80V60DFwith specific test circuit. Refer to STGW80V60DF datasheet for more information

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3 Chip layout

Figure 1. Die drawing and dimensions[a]

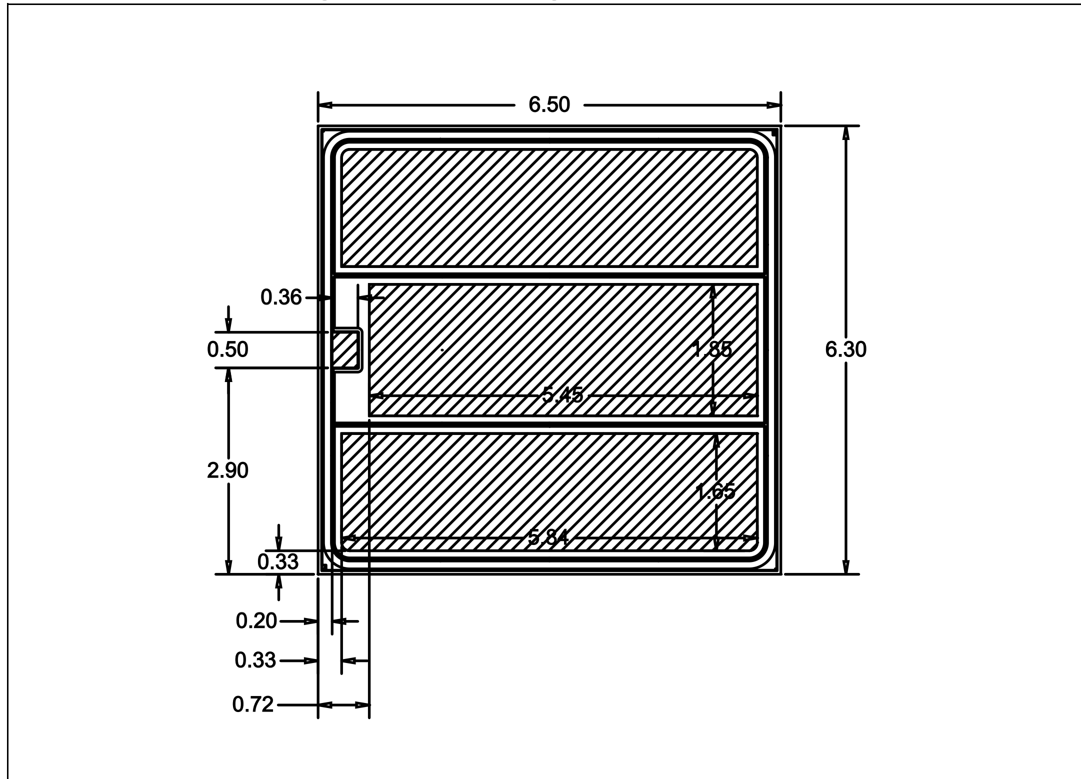

Table 7. Die delivery

Package option	Description	Details
D7	Wafer (8 inches) tested, inked, cut on sticky foil on 10.8" (276 mm) ring (see *Figure 2*)	Wafer (8 inches) is held by ring protected by two carton shells, inside a plastic envelope sealed under vacuum Maximum number of wafers for each package is 5, weight is about 3.7 Kg

a. Dimensions are in mm.

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Figure 2. D7 drawing

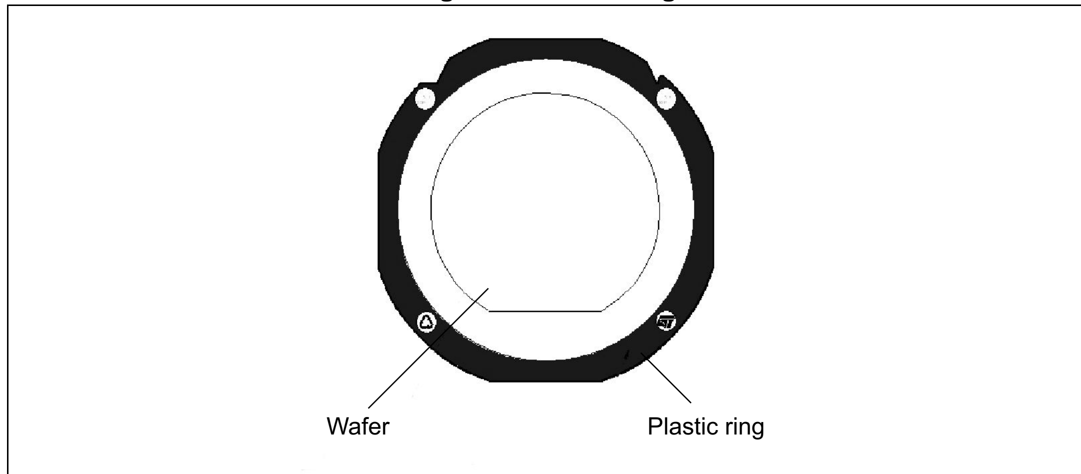
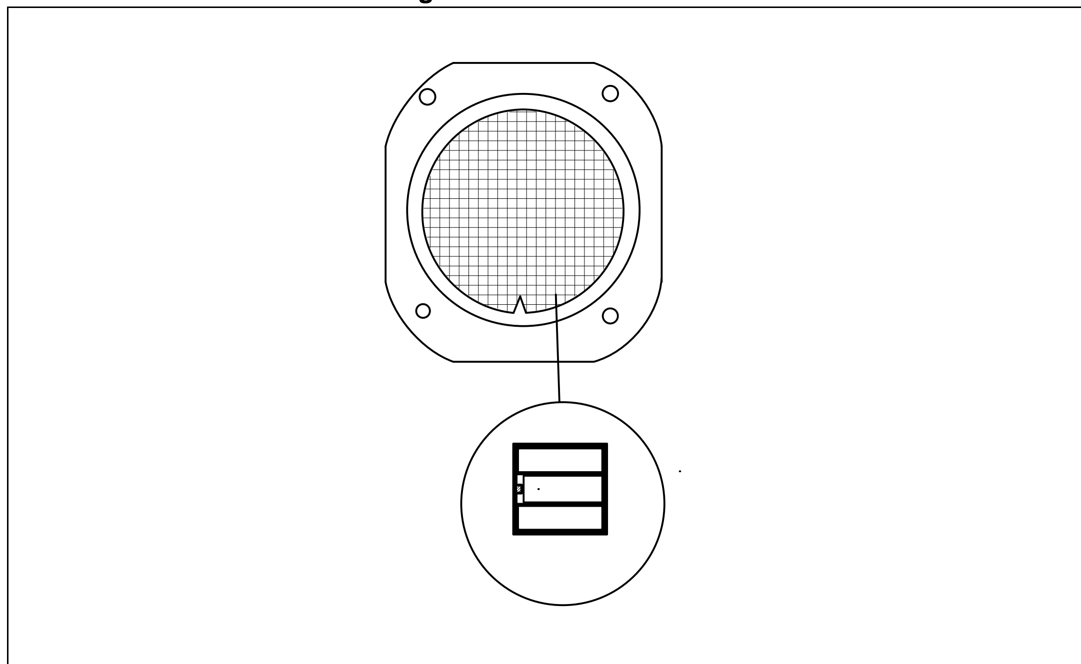


Figure 3. Die orientation



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4 Additional information

4.1 Additional testing and screening

For customers requiring products supplied as known good die (KGD) or requiring specific die level testing, please contact the local ST sales office.

4.2 Shipping

Several shipping options are offered, consult the local ST sales office for availability:

- Die on film sticky foil - suffix on sales type D7
- Carrier tape - suffix on sales type D8+KGD

4.3 Handling

- Products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Products must be handled only in a class 1000 or better-designated clean room environment.
- Singular dice are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

4.4 Wafer/die storage

Once opened, the wafer must be stored in a dry, inert atmosphere, such as nitrogen. Optimum temperature for storage is 18 °C ± 2 °C with as few variations as possible to avoid parasitic polymerization of the adhesive. Sawn wafers must be processed within 12 weeks after receipt by customer.

After the customer opens the package, the customer is responsible for the products.

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5 Revision history

Table 8. Document revision history

Date	Revision	Changes
21-Apr-2015	1	Initial release.

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