ON Semiconductor

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MJE18008, MJF18008

Switch-mode NPN Bipolar Power Transistor

For Switching Power Supply Applications

The MJE/MJF18008 have an applications specific state−of−the−art die designed for use in 220 V line−operated switch−mode Power supplies and electronic light ballasts.

Features

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain h_{FE}
  - Fast Switching
  - No Coil Required in Base Circuit for Turn−Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot−to−Lot
- Two Package Choices: Standard TO−220 or Isolated TO−220
- MJF18008, Case 221D, is UL Recognized at 3500 V_{RMS}: File #E69369
- These Devices are Pb−Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector−Base Breakdown Voltage	V_{CES}	1000	Vdc
Emitter−Base Voltage	V_{EBO}	9.0	Vdc
Collector Current − Continuous	I_C	8.0	Adc
Collector Current − Peak (Note 1)	I_{CM}	16	Adc
Base Current − Continuous	I_B	4.0	Adc
Base Current − Peak (Note 1)	I_{BM}	8.0	Adc
RMS Isolation Voltage (Note 2) Test No. 1 Per Figure 22a Test No. 1 Per Figure 22b Test No. 1 Per Figure 22c (for 1 sec, R.H. < 30%, T_A = 25°C)	V_{ISOL}	**MJF18008** 4500 3500 1500	V
Total Device Dissipation @ T_C = 25°C MJE18008 MJF18008 Derate above 25°C MJE18008 MJF18008	P_D	 125 45 1.0 0.36	 W W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case MJE18008 MJF18008	$R_{\theta JC}$	 1.0 2.78	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.
2. Proper strike and creepage distance must be provided.

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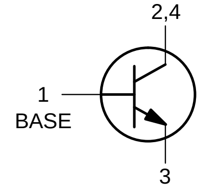
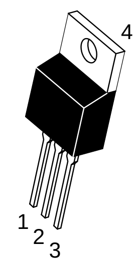
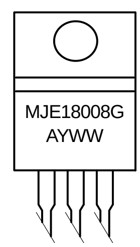
POWER TRANSISTOR
8.0 AMPERES
1000 VOLTS
45 and 125 WATTS

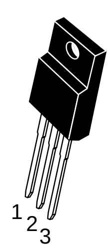


MARKING DIAGRAMS

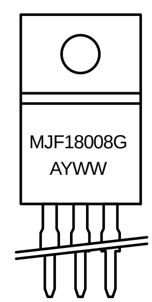


TO−220AB
CASE 221A−09
STYLE 1





TO−220 FULLPACK
CASE 221D
STYLE 2
UL RECOGNIZED



G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

January, 2015 − Rev. 10

Publication Order Number:
MJE18008/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	450	–	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	–	–	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	–	–	100	μAdc
(T_C = 125°C)		–	–	500	
(V_{CE} = 800 V, V_{EB} = 0) (T_C = 125°C)		–	–	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	–	–	100	μAdc
ON CHARACTERISTICS					
Base−Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)	$V_{BE(sat)}$	–	0.82	1.1	Vdc
(I_C = 4.5 Adc, I_B = 0.9 Adc)		–	0.92	1.25	
Collector−Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$	–	0.3	0.6	Vdc
(T_C = 125°C)		–	0.3	0.65	
(I_C = 4.5 Adc, I_B = 0.9 Adc)		–	0.35	0.7	
(T_C = 125°C)		–	0.4	0.8	
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	14	–	34	–
(T_C = 125°C)		–	28	–	
(I_C = 4.5 Adc, V_{CE} = 1.0 Vdc)		6.0	9.0	–	
(T_C = 125°C)		5.0	8.0	–	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)		11	15	–	
(T_C = 125°C)		11	16	–	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		10	20	–	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	–	13	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	100	150	pF
Input Capacitance (V_{EB} = 8.0 V)	C_{ib}	–	1750	2500	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18); (I_C = 2.0 Adc, I_{B1} = 200 mAdc, V_{CC} = 300 V) 1.0 μs	$V_{CE(dsat)}$	–	5.5	–	Vdc
(T_C = 125°C)		–	11.5	–	
3.0 μs		–	3.5	–	
(T_C = 125°C)		–	6.5	–	
(I_C = 5.0 Adc, I_{B1} = 1.0 Adc, V_{CC} = 300 V) 1.0 μs		–	11.5	–	
(T_C = 125°C)		–	14.5	–	
3.0 μs		–	2.4	–	
(T_C = 125°C)		–	9.0	–	
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)					
Turn−On Time (I_C = 2.0 Adc, I_{B1} = 0.2 Adc, I_{B2} = 1.0 Adc, V_{CC} = 300 V)	t_{on}	–	200	300	ns
(T_C = 125°C)		–	190	–	
Turn−Off Time	t_{off}	–	1.2	2.5	μs
(T_C = 125°C)		–	1.5	–	
Turn−On Time (I_C = 4.5 Adc, I_{B1} = 0.9 Adc, I_{B2} = 2.25 Adc, V_{CC} = 300 V)	t_{on}	–	100	180	ns
(T_C = 125°C)		–	250	–	
Turn−Off Time	t_{off}	–	1.6	2.5	μs
(T_C = 125°C)		–	2.0	–	
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)					
Fall Time (I_C = 2.0 Adc, I_{B1} = 0.2 Adc, I_{B2} = 1.0 Adc)	t_{fi}	–	100	180	ns
(T_C = 125°C)		–	120	–	
Storage Time	t_{si}	–	1.5	2.75	μs
(T_C = 125°C)		–	1.9	–	
Crossover Time	t_c	–	250	350	ns
(T_C = 125°C)		–	230	–	
Fall Time (I_C = 4.5 Adc, I_{B1} = 0.9 Adc, I_{B2} = 2.25 Adc)	t_{fi}	–	85	150	ns
(T_C = 125°C)		–	135	–	
Storage Time	t_{si}	–	2.0	3.2	μs
(T_C = 125°C)		–	2.6	–	
Crossover Time	t_c	–	210	300	ns
(T_C = 125°C)		–	250	–	

3. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
4. Proper strike and creepage distance must be provided.

TYPICAL STATIC CHARACTERISTICS

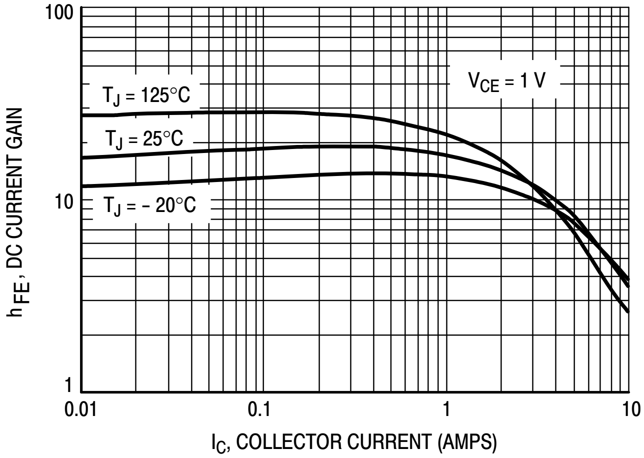


Figure 1. DC Current Gain @ 1 Volt

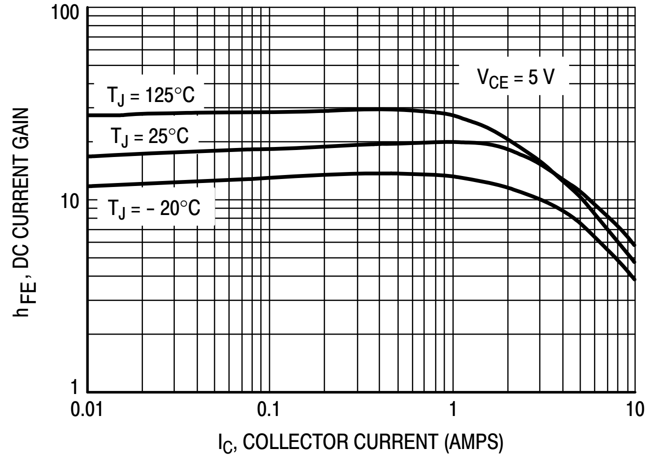


Figure 2. DC Current Gain @ 5 Volts

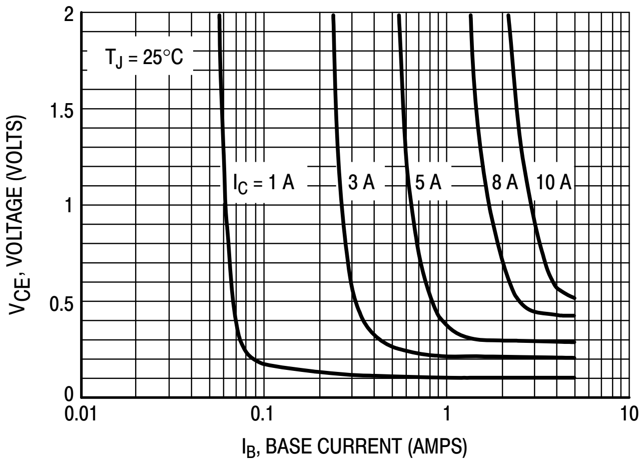


Figure 3. Collector Saturation Region

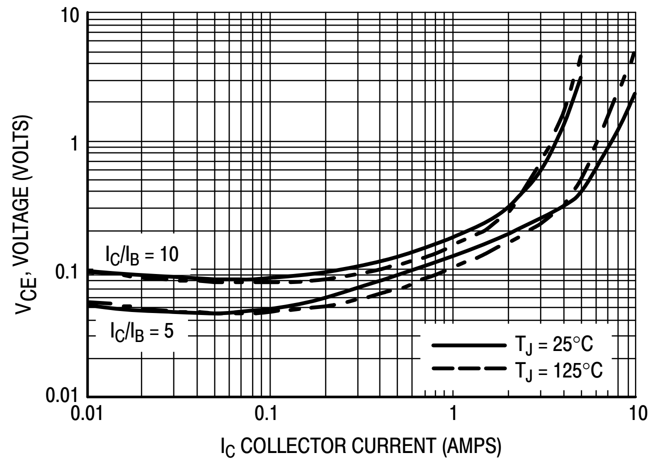


Figure 4. Collector−Emitter Saturation Voltage

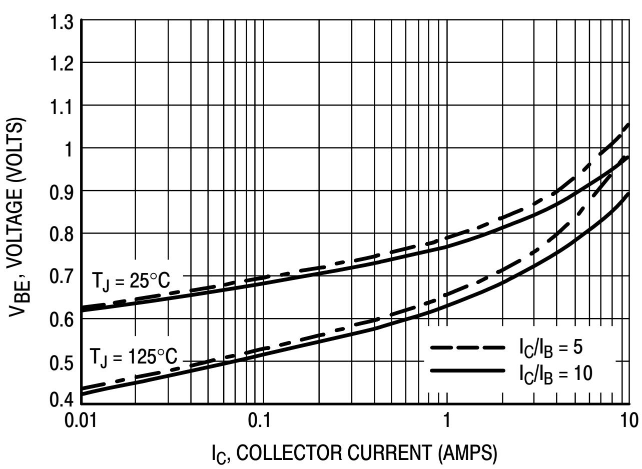


Figure 5. Base−Emitter Saturation Region

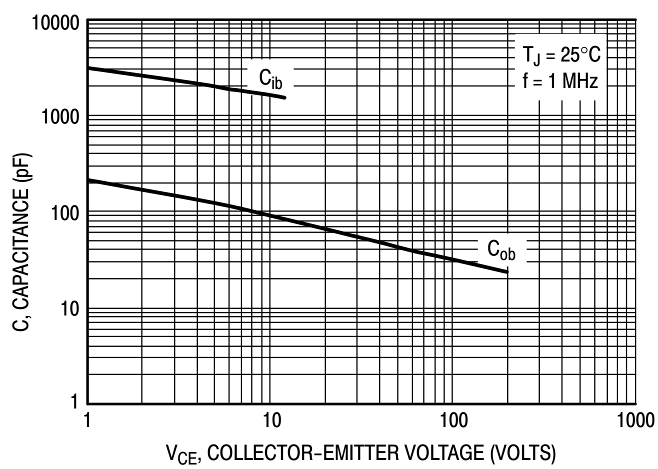


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

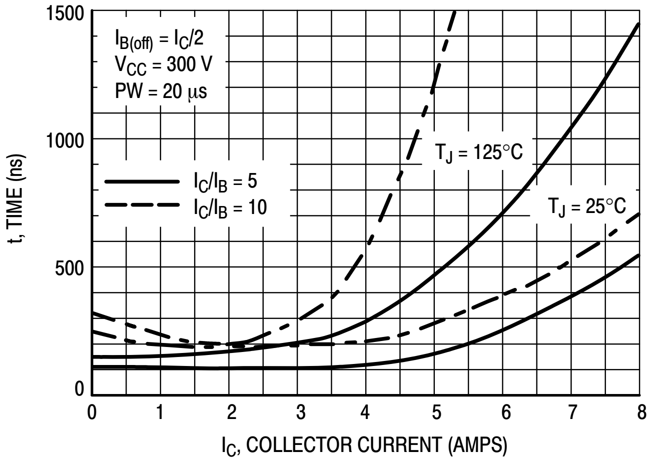


Figure 7. Resistive Switching, t_{on}

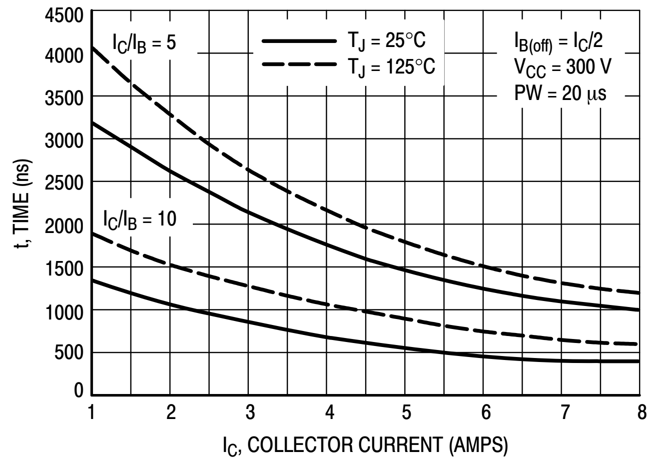


Figure 8. Resistive Switching, t_{off}

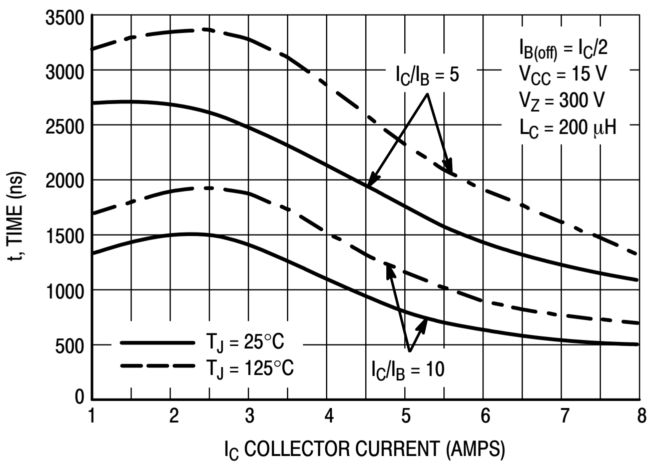


Figure 9. Inductive Storage Time, t_{si}

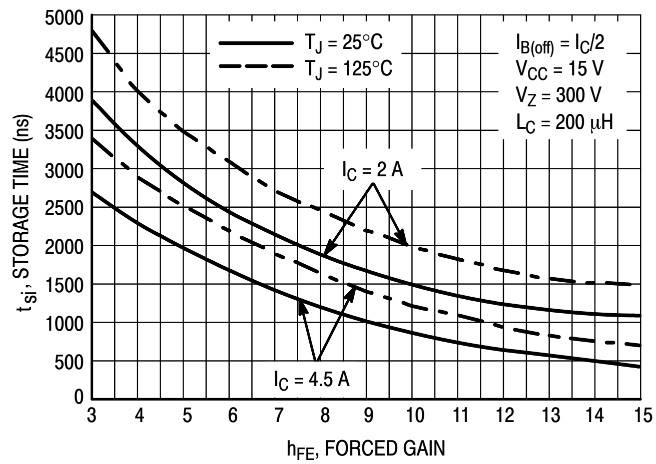


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

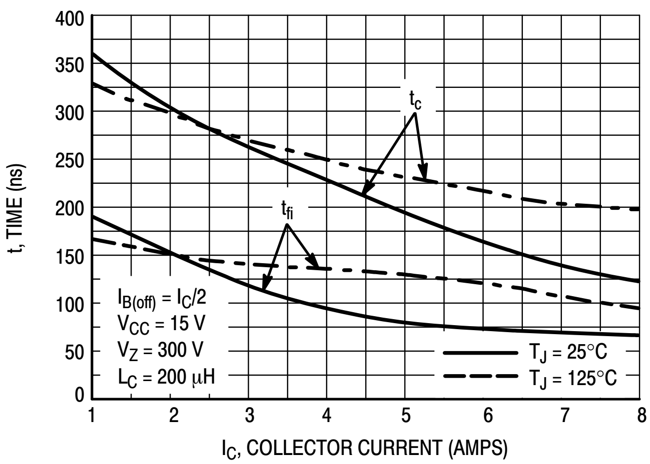


Figure 11. Inductive Switching, t_c and t_{fi}
I_C/I_B = 5

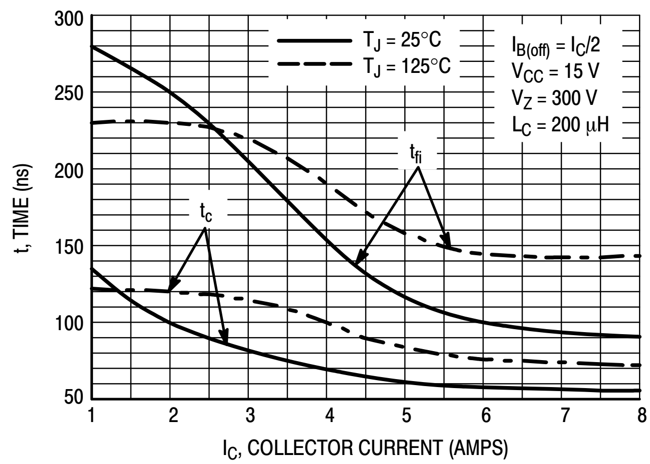


Figure 12. Inductive Switching, t_c and t_{fi}
I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

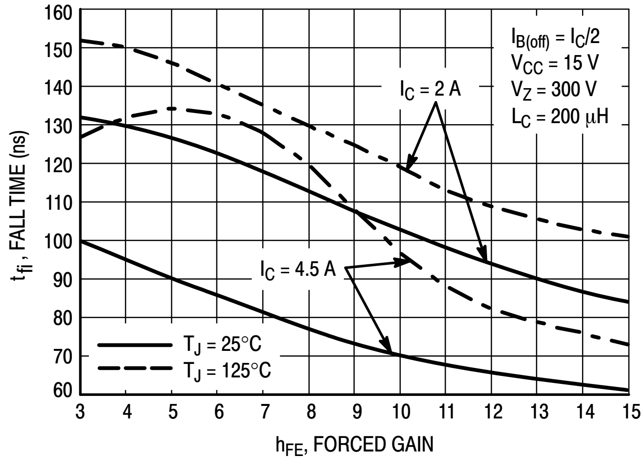


Figure 13. Inductive Fall Time

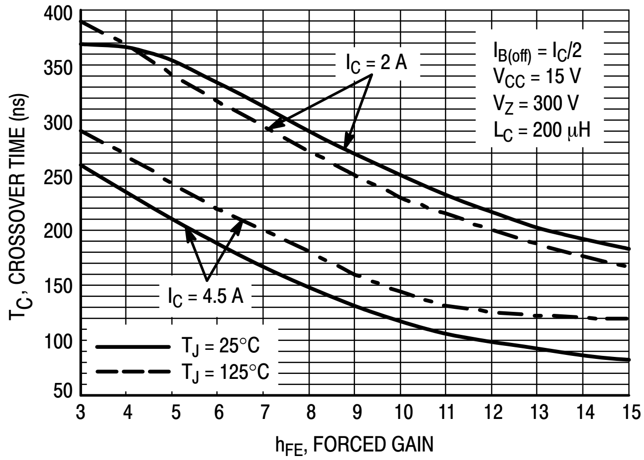


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

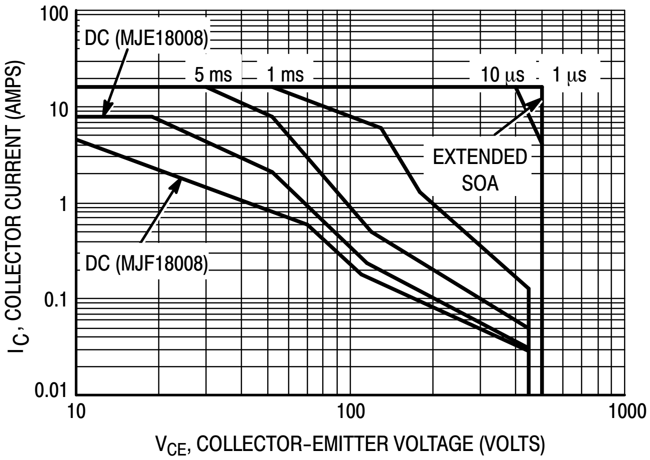


Figure 15. Forward Bias Safe Operating Area

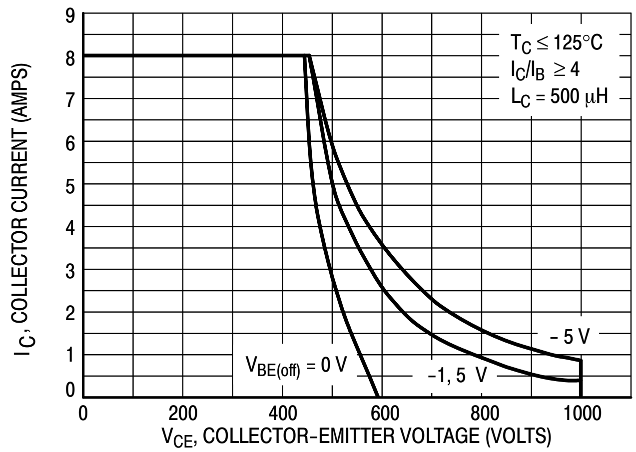


Figure 16. Reverse Bias Switching Safe Operating Area

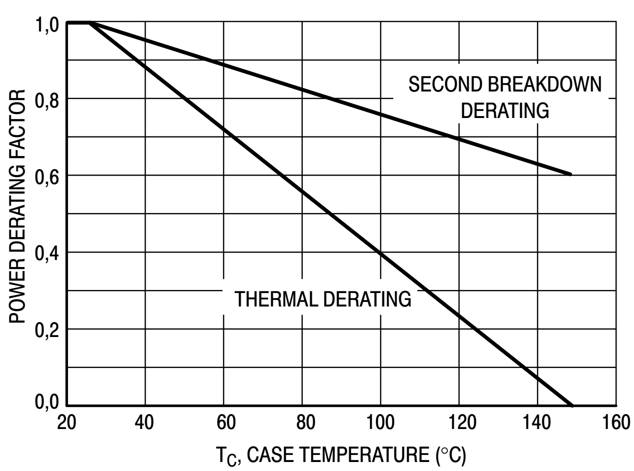


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figure 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base−to−emitter junction reverse−biased. The safe level is specified as a reverse−biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

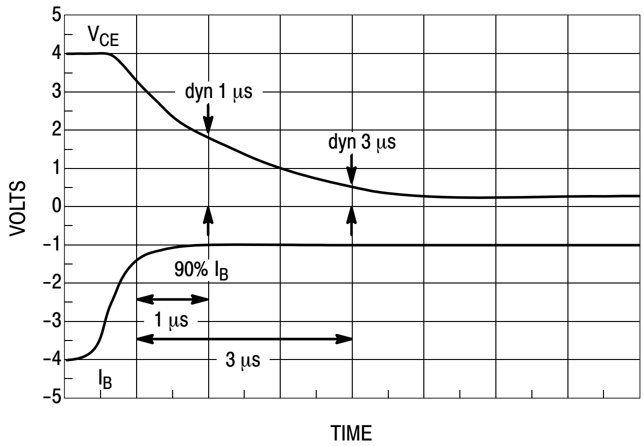


Figure 18. Dynamic Saturation Voltage Measurements

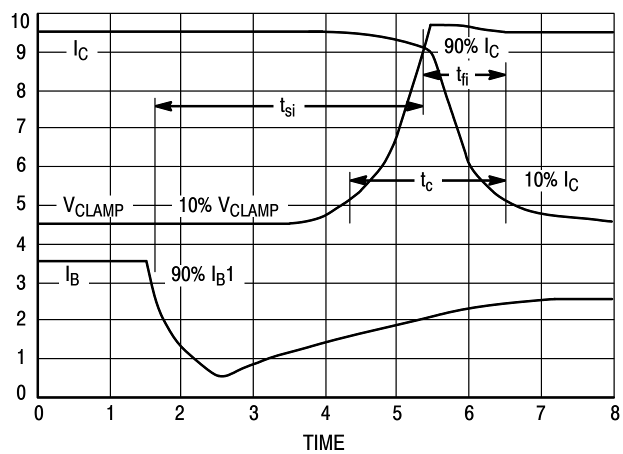


Figure 19. Inductive Switching Measurements

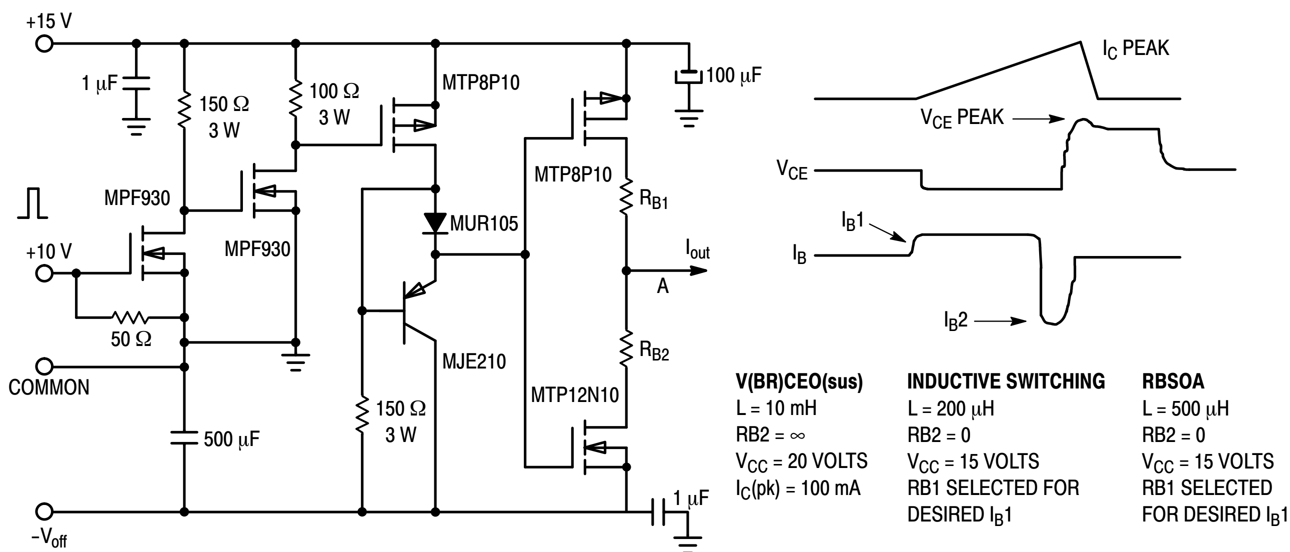


Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

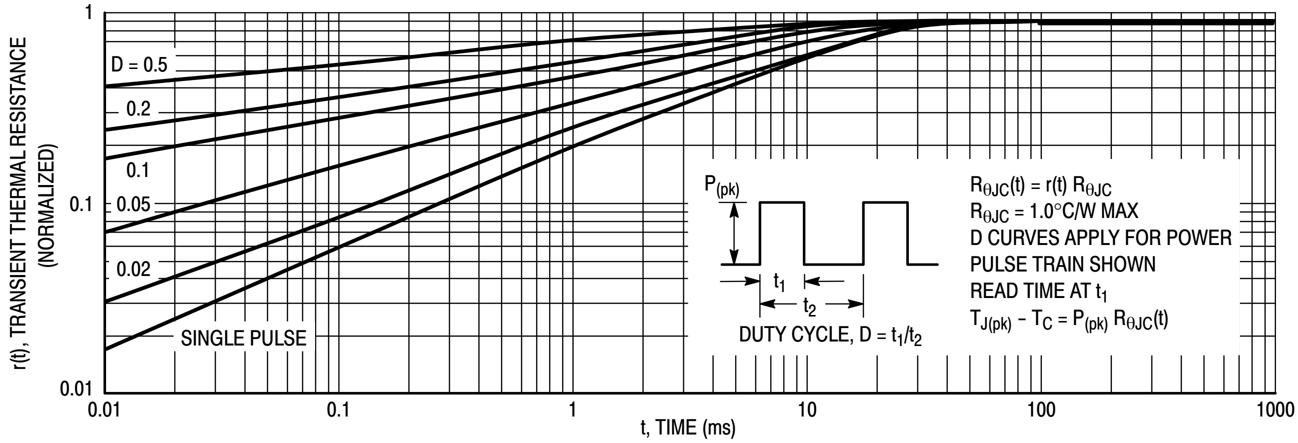


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18008

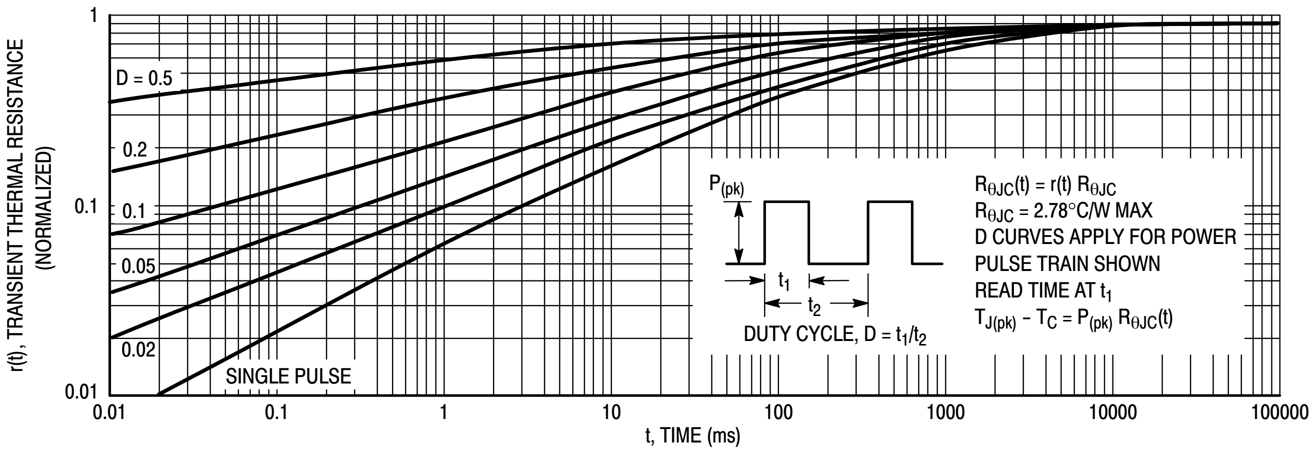


Figure 21. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJF18008

ORDERING INFORMATION

Device	Package	Shipping
MJE18008G	TO−220AB (Pb−Free)	50 Units / Rail
MJF18008G	TO−220 (Fullpack) (Pb−Free)	50 Units / Rail

TEST CONDITIONS FOR ISOLATION TESTS*

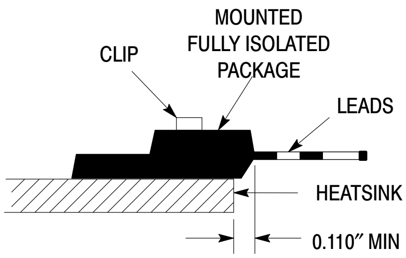


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

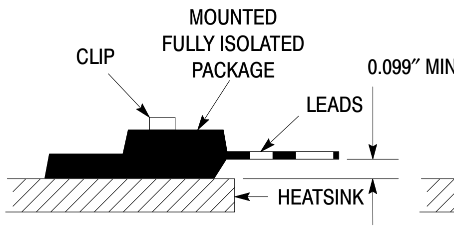


Figure 22b. Clip Mounting Position for Isolation Test Number 2

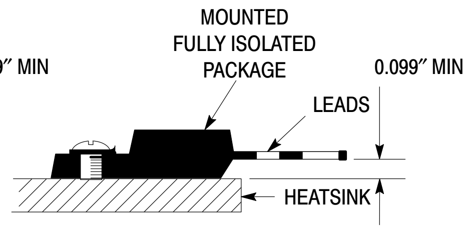


Figure 22c. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

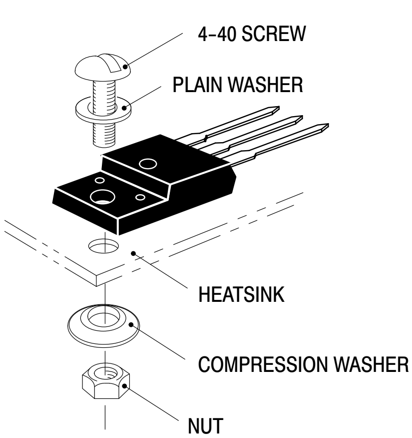


Figure 23a. Screw−Mounted

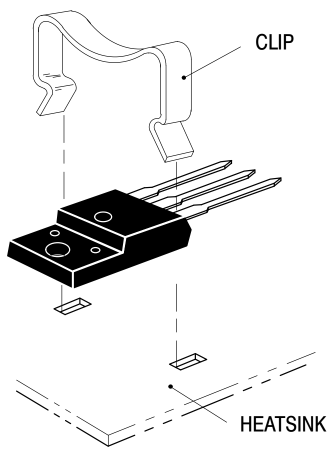


Figure 23b. Clip−Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

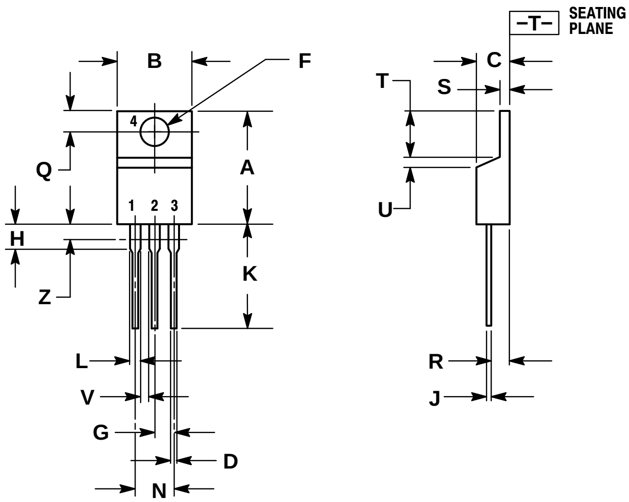
Destructive laboratory tests show that using a hex head 4−40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4−40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AH

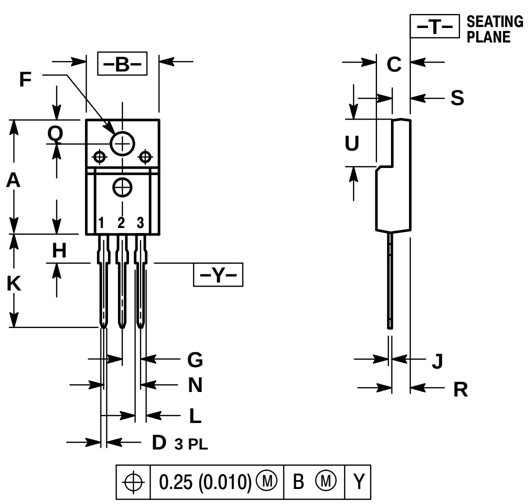


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

TO−220 FULLPAK
CASE 221D−03
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

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