D44VH10 (NPN), D45VH10 (PNP)

Complementary Silicon Power Transistors

These complementary silicon power transistors are designed for high−speed switching applications, such as switching regulators and high frequency inverters. The devices are also well−suited for drivers for high power switching circuits.

Features

- Fast Switching
- Key Parameters Specified @ 100°C
- Low Collector−Emitter Saturation Voltage
- Complementary Pairs Simplify Circuit Designs
- These Devices are Pb−Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Collector−Emitter Voltage	V_{CEV}	100	Vdc
Emitter Base Voltage	V_{EB}	7.0	Vdc
Collector Current − Continuous	I_C	15	Adc
Collector Current − Peak (Note 1)	I_{CM}	20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 83 0.67	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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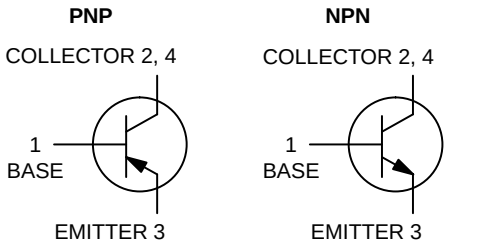
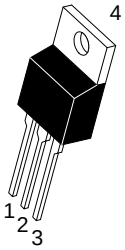
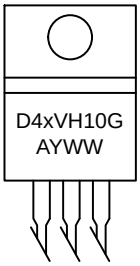
15 A
COMPLEMENTARY SILICON POWER TRANSISTORS
80 V, 83 W





TO−220
CASE 221A
STYLE 1

MARKING DIAGRAM



x = 4 or 5
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
D44VH10G	TO−220 (Pb−Free)	50 Units/Rail
D45VH10G	TO−220 (Pb−Free)	50 Units/Rail

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 2) (I_C = 25 mAdc, I_B = 0)	$V_{CEO(sus)}$	80	–	–	Vdc
Collector−Emitter Cutoff Current (V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc) (V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc, T_C = 100°C)	I_{CEV}	– –	– –	10 100	μAdc
Emitter Base Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	–	10	μAdc
ON CHARACTERISTICS (Note 2)					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	35 20	– –	– –	–
Collector−Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.4 Adc) D44VH10 (I_C = 8.0 Adc, I_B = 0.8 Adc) D45VH10 (I_C = 15 Adc, I_B = 3.0 Adc, T_C = 100°C) D44VH10 D45VH10	$V_{CE(sat)}$	 – – – –	 – – – –	 0.4 1.0 0.8 1.5	Vdc
Base−Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.4 Adc) D44VH10 (I_C = 8.0 Adc, I_B = 0.8 Adc) D45VH10 (I_C = 8.0 Adc, I_B = 0.4 Adc, T_C = 100°C) D44VH10 (I_C = 8.0 Adc, I_B = 0.8 Adc, T_C = 100°C) D45VH10	$V_{BE(sat)}$	 – – – –	 – – – –	 1.2 1.0 1.1 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	–	50	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_C = 0, f_{test} = 1.0 MHz) D44VH10 D45VH10	C_{ob}	 – –	 120 275	 – –	pF
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 20 Vdc, I_C = 8.0 Adc, I_{B1} = I_{B2} = 0.8 Adc)	t_d	–	–	50	ns
Rise Time		t_r	–	–	250	
Storage Time		t_s	–	–	700	
Fall Time		t_f	–	–	90	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

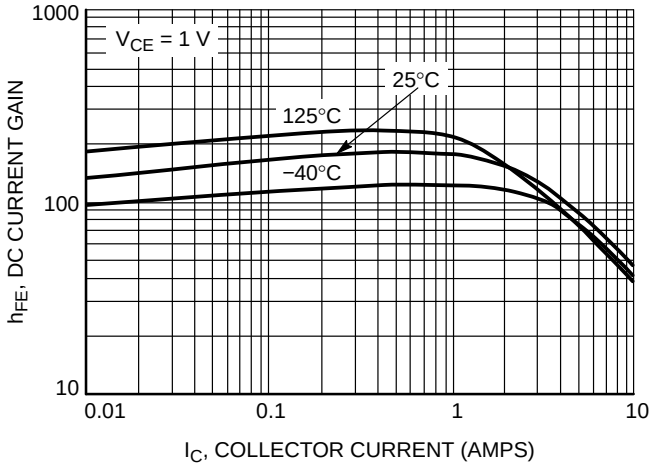


Figure 1. D44VH10 DC Current Gain

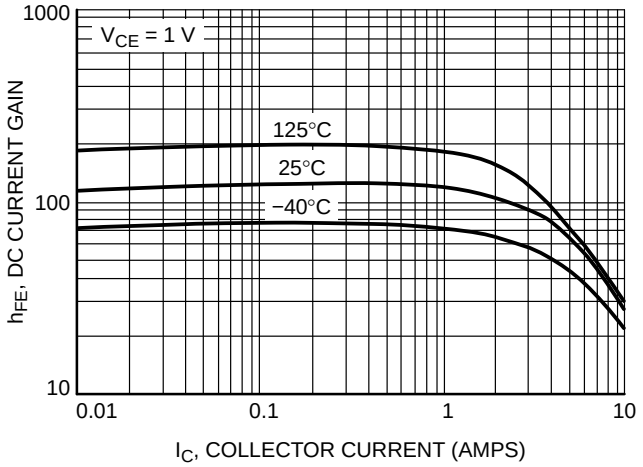


Figure 2. D45VH10 DC Current Gain

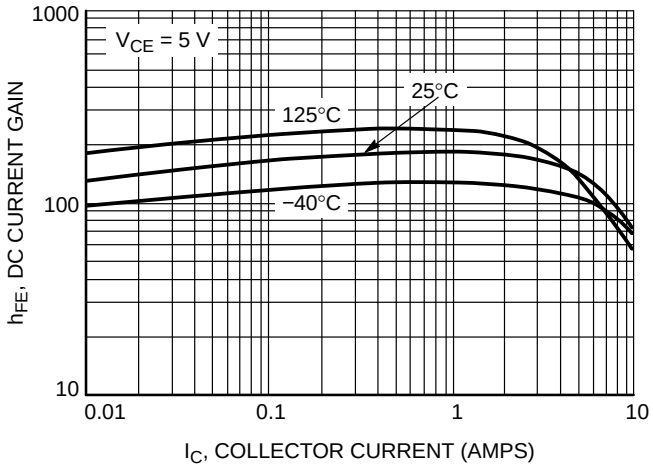


Figure 3. D44VH10 DC Current Gain

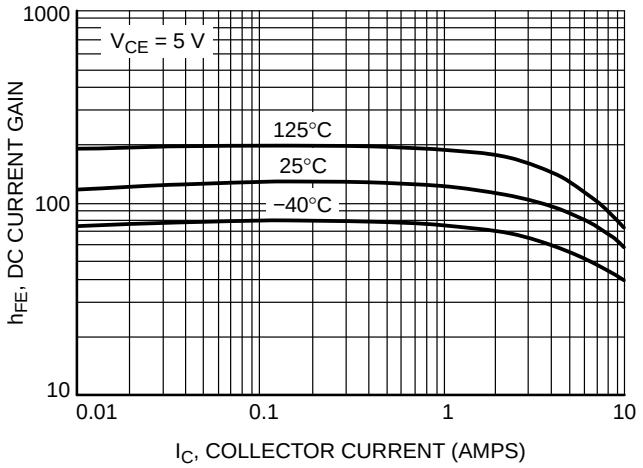


Figure 4. D45VH10 DC Current Gain

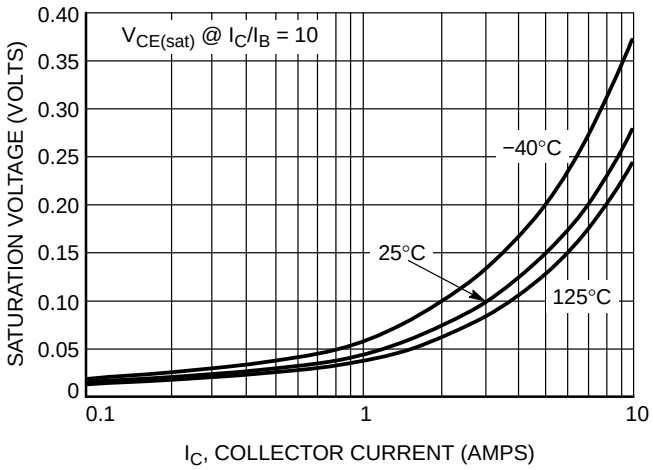


Figure 5. D44VH10 ON−Voltage

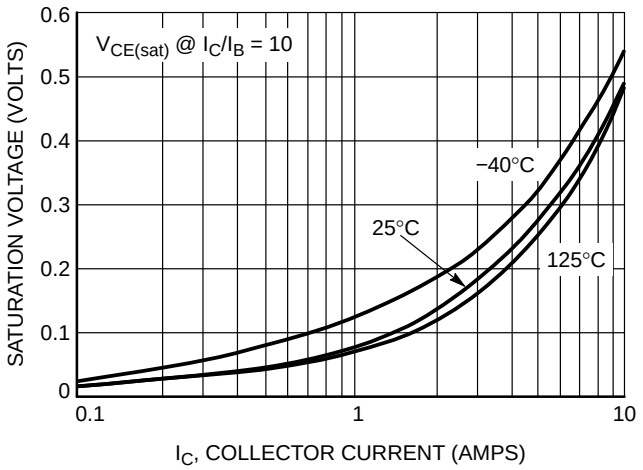


Figure 6. D45VH10 ON−Voltage

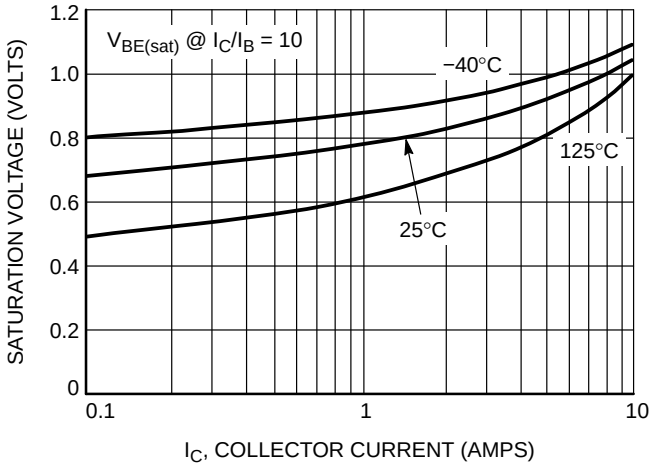


Figure 7. D44VH10 ON−Voltage

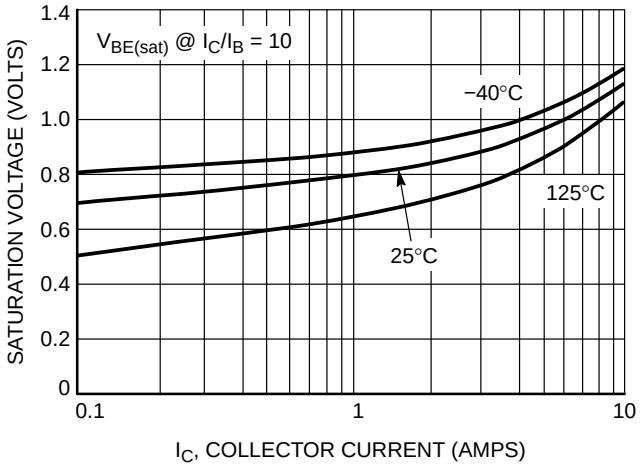


Figure 8. D45VH10 ON−Voltage

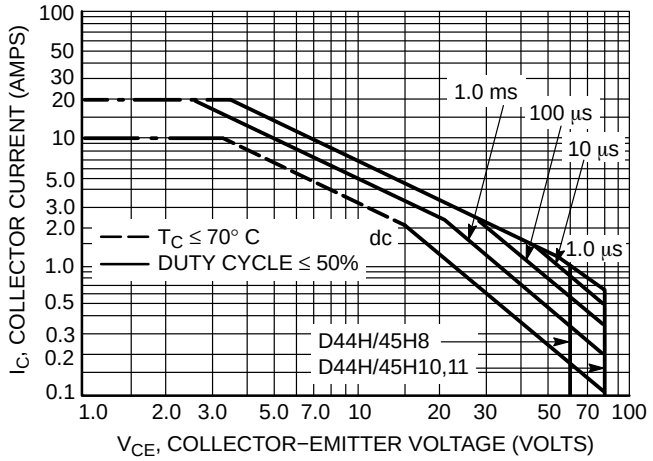


Figure 9. Maximum Rated Forward Bias Safe Operating Area

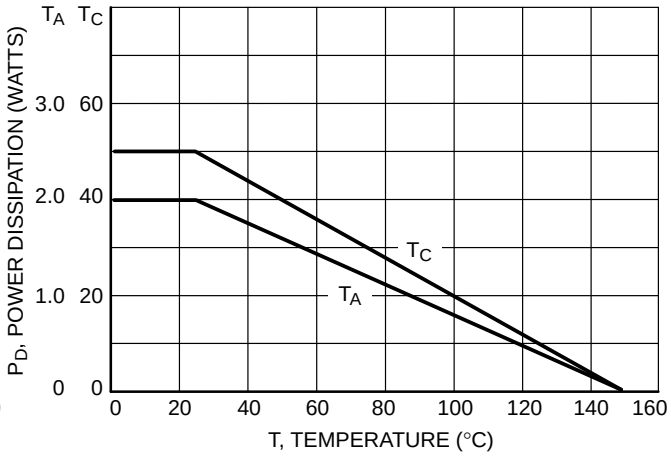


Figure 10. Power Derating

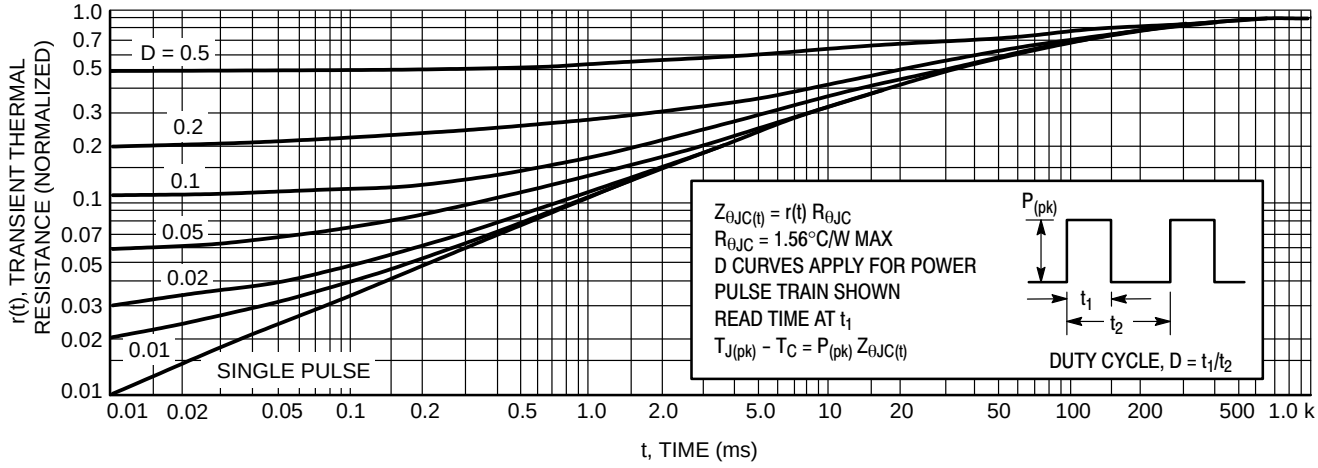
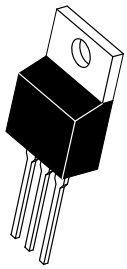


Figure 11. Thermal Response

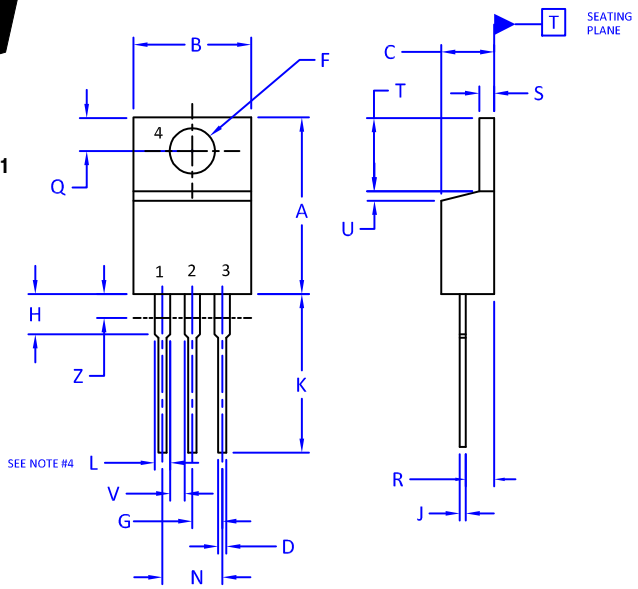
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TO−220
CASE 221A
ISSUE AK

DATE 13 JAN 2022



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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